TEXAS INSTRUMENTS

High-Performance FIFO Memories

Designer's Handbook

1996

Advanced System Logic Products

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5 Mechanical and Thermal Information
6 Device Models
7 Quality and Reliability Assurance

High-Performance FIFO Memories Designer's Handbook

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INTRODUCTION

The Texas Instruments (TI) High-Performance FIFO Memories Designer's Handbook has been created to provide users and potential users of TI's FIFOs with a comprehensive collection of information and data used as a reference guide during the design-in process. In a much broader sense, the designer's handbook also is a means to further the overall understanding and awareness of TI's FIFOs and their many applications.

The contents of the handbook complement the information contained in the 1996 High-Performance FIFO Memories Data Book, literature number SCAD003C. In addition to an expanded series of FIFO application notes, the handbook also contains information that is useful to the designer, such as sample power-dissipation calculations, mechanical packaging data, thermal-resistance data, and quality/reliability assurance information. Section 6, *Device Models*, includes lists of available VHDL [VHSIC (very high-speed integrated circuits) hardware-description language] models and logic-modeling behavior models.

This designer's handbook is organized into seven major sections: *General Information* (section 1), *Product Overview* (section 2), *Specific Application Reports* (section 3), *Power Considerations* (section 4), *Mechanical and Thermal Information* (section 5), *Device Models* (section 6), and *Quality and Reliability Assurance* (section 7).

Section 1 contains a glossary of symbols, terms, and definitions that are used throughout the handbook. These symbols, terms, and definitions are presented in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association.

Section 2 provides an overview of TI's FIFO products. The summary charts in this section allow quick reference of key FIFO parameters, such as architecture, organization, speed sort, maximum clock frequency, and available packaging options. The features associated with TI's advanced application-specific FIFOs are summarized in this section. Section 2 also includes a flow chart that can be used as an aid in selecting a FIFO architecture based on a known bus width.

Section 3 provides a comprehensive set of FIFO application reports. The application reports are organized into subsections based on the subject matter of each report. The subsections are *FIFO Performance and Reliability*, *FIFO Features*, and *FIFO Applications*.

Section 4 provides typical power characteristics in the form of active supply current versus frequency for each of TI's advanced FIFOs. Plots of idle supply current versus frequency also are given for a select number of FIFOs. In addition to this data, sample power-dissipation calculations are performed for a representative set of FIFOs. The application report in this section is used as a guideline for these calculations. Calculations and equations are provided for CMOS FIFOs and Advanced BiCMOS Technology (ABT) FIFOs.

Section 5 contains mechanical drawings for each FIFO packaging option. The official JEDEC descriptor is used to identify each package type. These drawings typically include the following dimensions: lead pitch (tip to tip), body width and length, shoulder-to-shoulder insertion width, lead width, thickness, and angles, and package maximum height, and stand-off clearances from seating plane to bottom of the package. Included with the mechanical data is thermal data for each FIFO packaging option. Thermal resistance values for varying conditions and power-dissipation derating curves for varying air flows are

presented for each package type. Several application reports and papers also are included in this section to provide further detail regarding overall thermal considerations and thermal-resistance measurements, including the design and development of the thermally enhanced thin quad flat package (TQFP).

Section 6 contains a list of the behavioral models currently available from TI. All speed sorts of the devices under consideration are included in the models. VHDL models of FIFO devices included in this section may be obtained by calling the Advanced System Logic hotline at 903-868-5202.

Section 7 addresses the issue of quality and reliability assurance for TI's FIFO products. Concepts such as the qualification of products and processes, quality and reliability assurance in integrated-circuit design, and quality and reliability monitoring are discussed.

For further information on TI's FIFO products or applications, please contact the Advanced System Logic hotline at 903-868-5202. For information on TI's military FIFO devices, contact military Advanced System Logic marketing at 915-561-7289.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i — Input capacitance

The internal capacitance at an input of the device

C_o — Output capacitance

The internal capacitance at an output of the device

C_{pd} — Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} — Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

I_{CC} — Supply current

The current into* the V_{CC} supply terminal of an integrated circuit

ΔI_{CC} — Supply current change

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 or V_{CC}

I_{CEX} — Output high-leakage current

The maximum leakage current into the collector of the pulldown-output transistor when the output is high and the output forcing condition $V_O = 5.5$ V

$I_{I(hold)}$ — Input-hold current

Input current that holds the input at the previous state when the driving device goes to a high-impedance state

I_{IH} — High-level input current

The current into* an input when a high-level voltage is applied to that input

I_{IL} — Low-level input current

The current into* an input when a low-level voltage is applied to that input

I_{off} — Input/output power-off leakage current

The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and $V_{CC} = 0$

I_{OH} — High-level output current

The current into* an output with input conditions applied that, according to the product specification, establishes a high level at the output

I_{OL} — Low-level output current

The current into* an output with input conditions applied that, according to the product specification, establishes a low level at the output

*Current out of a terminal is given as a negative value.

GLOSSARY
SYMBOLS, TERMS, AND DEFINITIONS

I_{OZ} **Off-state (high-impedance-state) output current (of a 3-state output)**

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, establishes the high-impedance state at the output

$R_{\Theta JA}$ **Junction-to-ambient thermal resistance**

The thermal resistance from the semiconductor junction(s) to the ambient

$R_{\Theta JC}$ **Junction-to-case thermal resistance**

The thermal resistance from the semiconductor junction(s) to a stated location on the case

t_a **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output

t_c **Clock cycle time**

Clock cycle time is $1/f_{max}$.

t_{dis} **Disable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low)

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

t_h **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value, in which case, the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

t_{pd} **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH})

t_{PHL} **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} **Disable time (of a 3-state output) from high level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

*Current out of a terminal is given as a negative value.

t_{PLH} **Propagation delay time, low-to-high level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

t_{PLZ} **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

t_{PZH} **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

t_{PZL} **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

t_{su} **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The setup time may have a negative value, in which case, the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is to be expected.

t_w **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

V_{IH} **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{IL} **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output

V_{OL} **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output

V_{IT+} **Positive-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element, according to specification, as the input voltage rises from a level below the negative-going threshold voltage, V_{IT-}

V_{IT-} Negative-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element, according to specification, as the input voltage falls from a level above the positive-going threshold voltage, V_{IT+}

V_{OHV} High-level output voltage change during simultaneous switching

The minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs

V_{OLP} Low-level output voltage change during simultaneous switching

The maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs

definitions

asynchronous FIFO

Data writes are initiated by a low-level pulse on the write-enable input when the full flag is not asserted. Likewise, data reads are initiated by a low-level pulse on the read-enable input when the empty flag is not asserted. The empty and full flags are not synchronized to a particular clock and reflect the instantaneous comparison of the read and write pointers.

clocked FIFO

Data is written by a low-to-high transition of a write clock when write-enable inputs are asserted and the input-ready flag is not asserted. Likewise, data is read by a low-to-high transition of a read clock when read-enable inputs are asserted and the output-ready flag is asserted. The input-ready flag is multistaged synchronized to the write clock and the ouput-ready flag is multistaged synchronized to the read clock, improving metastability.

strobed FIFO

Data is written on a low-to-high transition on the load-clock input when the full flag is not asserted. Likewise, data is read on a low-to-high transition on the unload-clock input when the empty-flag is not asserted. The empty and full flags are not synchronized to a particular clock and reflect the instantaneous comparison of the read and write pointers.

synchronous FIFO

The term synchronous refers to a port-control method and does not imply that data writes and reads must be synchronous to one another. Data is written by a low-to-high transition of a write clock when write-enable inputs are asserted and the full flag is not asserted. Likewise, data is read by a low-to-high transition of a read clock when read-enable inputs are asserted and the empty flag is not asserted. The empty flag is single-staged synchronized to the read clock and the full flag is single-staged synchronized to the write clock.

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2 Product Overview

FIFO Product Offerings

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FIFO PRODUCT OFFERINGS

Advanced Clocked FIFOs

DEVICE	ORGANIZATION	SPEED SORT t_c (ns)	MAXIMUM FREQUENCY (MHz)	ACCESS TIME (ns)	I_{OH}/I_{OL} (mA)	PACKAGE	PITCH (mm)	AREA (mm^2)
SN74ACT7884 SN74ACT7882 SN74ACT7881	4K × 18 2K × 18 1K × 18	−15, −20,−30	67, 50, 33	11, 13, 18	8/16	80-pin TQFP (PN) 68-pin PLCC (FN)	0.5 1.27	196 310
SN74ACT7811	1K × 18	−15, −18, −20, −25	40, 35, 29, 17	15, 18, 20, 25	8/16	80-pin TQFP (PN) 68-pin PLCC (FN)	0.5 1.27	196 310
SN74ACT7803 SN74ACT7805 SN74ACT7813	512 × 18 256 × 18 64 × 18	−15, −20, −25, −40	67, 50, 40, 30	12, 13, 15, 20	8/16	56-pin SSOP (DL)	0.635	191
SN74ACT7807	2K × 9	−15, −20, −25, −40	67, 50, 40, 25	12, 13, 18, 25	8/16	64-pin TQFP (PM/PAG) 44-pin PLCC (FN)	0.5 1.27	144 310
SN74ABT7819	512 × 18 × 2	−12, −15, −20, −30	80, 67, 50, 33	9, 10, 12, 14	12/24	80-pin TQFP (PN) 80-pin PQFP (PH)	0.5 0.8	196 432
SN74ALVC7803 SN74ALVC7805 SN74ALVC7813	512 × 18 256 × 18 64 × 18	−20, −25,−40	25, 40, 50	13, 15, 20	8/16	56-pin SSOP (DL)	0.635	191

Advanced Strobed FIFOs

DEVICE	ORGANIZATION	SPEED SORT t_c (ns)	MAXIMUM FREQUENCY (MHz)	ACCESS TIME (ns)	I_{OH}/I_{OL} (mA)	PACKAGE	PITCH (mm)	AREA (mm^2)
SN74ACT7802	1K × 18	−25, −40, −60	40, 25, 17	30, 35, 45	8/16	80-pin TQFP (PN) 68-pin PLCC (FN)	0.5 1.27	196 635
SN74ACT2235 SN74ACT2236	1K × 9 × 2	−20, −30, −40, −60	50, 33, 25, 17	25, 25, 35, 45	8/16	64-pin TQFP (PM/PAG) 44-pin PLCC (FN)	0.5 1.27	144 310
SN74ACT7804 SN74ACT7806 SN74ACT7814	512 × 18 256 × 18 64 × 18	−20, −25, −40	50, 40, 25	15, 18, 20	8/16	56-pin SSOP (DL)	0.635	191
SN74ACT7808	2K × 9	−20, −25, −30, −40	50, 40, 33, 25	15, 18, 20, 22	8/16	64-pin TQFP (PM/PAG) 44-pin PLCC (FN)	0.5 1.27	196 635
SN74ABT7820	512 × 18 × 2	−15, −20, −25, −40	67, 50, 40, 33	12, 14, 15, 17	12/24	80-pin TQFP (PN) 80-pin PQFP (PH)	0.5 0.8	196 432
SN74ALVC7804 SN74ALVC7806 SN74ALVC7814	512 × 18 256 × 18 64 × 18	−20, −25,−40	25, 40, 50	13, 15, 20	8/16	56-pin SSOP (DL)	0.635	191

FIFO PRODUCT OFFERINGS

Advanced Application-Specific Clocked FIFOs

DEVICE	ORGANIZATION	SPEED SORT t_c (ns)	MAXIMUM FREQUENCY (MHz)	ACCESS TIME (ns)	I_{OH}/I_{OL} (mA)	PACKAGE	PITCH (mm)	AREA (mm^2)
SN74ACT2226 SN74ACT2228	64 × 1 256 × 1		22	20	8/16	24-pin SOIC (DW)	1.27	165
SN74ACT2227 SN74ACT2229	64 × 1 256 × 1		60	9	8/16	28-pin SOIC (DW)	1.27	192
SN74ACT3638	512 × 32 × 2	–15, –20, –30	67, 50, 33	11, 13, 15	4/8	120-pin TQFP (PCB) 132-pin PQFP (PQ)	0.4 0.635	256 781
SN74ACT3622 SN74ACT3632 SN74ACT3642	256 × 36 × 2 512 × 36 × 2 1K × 36 × 2	–15, –20, –30	67, 50, 33	11, 13, 15	4/8	120-pin TQFP (PCB) 132-pin PQFP (PQ)	0.4 0.635	256 781
SN74ACT3631 SN74ACT3641 SN74ACT3651	512 × 36 1K × 36 2K × 36	–15, –20, –30	67, 50, 33	11, 13, 15	4/8	120-pin TQFP (PCB) 132-pin PQFP (PQ)	0.4 0.635	256 781
SN74ABT3611 SN74ABT3613	64 × 36 64 × 36	–15, –20, –30	67, 50, 33	10, 12, 15	4/8	120-pin TQFP (PCB) 132-pin PQFP (PQ)	0.4 0.635	256 781
SN74ABT3612 SN74ABT3614	64 × 36 × 2 64 × 36 × 2	–15, –20, –30	67, 50, 33	10, 12, 15	4/8	120-pin TQFP (PCB) 132-pin PQFP (PQ)	0.4 0.635	256 781

Advanced Application-Specific FIFO Features

TELECOMMUNICATIONS FIFOs	
SN74ACT2226 SN74ACT2228 SN74ACT2227 SN74ACT2229	Dual independent FIFO with separate output enables, separate I /O, separate resets, characterized to industrial temperature specification: –40°C to 85°C
DIGITAL-SIGNAL-PROCESSING FIFOs	
SN74ACT3638 SN74ACT3631 SN74ACT3641 SN74ACT3651	Microprocessor interface-control logic, synchronous retransmit capability, mailbox-bypass registers for each FIFO
SN74ACT3622 SN74ACT3632 SN74ACT3642	Microprocessor interface-control logic, mailbox-bypass registers for each FIFO
HIGH-BANDWIDTH COMPUTING FIFOs	
SN74ABT3611 SN74ABT3612	Microprocessor interface-control logic, parity generation and parity check, mailbox-bypass registers for each FIFO
INTERNETWORKING FIFOs	
SN74ABT3613 SN74ABT3614	Microprocessor interface-control logic, parity generation and parity check, bus matching and byte swapping, mailbox-bypass registers for each FIFO

Synchronous Mature FIFOs

DEVICE	ORGANIZATION	SPEED SORT t_c (ns)	MAXIMUM FREQUENCY (MHz)	ACCESS TIME (ns)	PACKAGE
SN74ACT72211L SN74ACT72221L SN74ACT72231L SN74ACT72241L	512 × 9 1K × 9 2K × 9 4K × 9	–15, –20, –25, –50	67, 50, 40, 20	10, 12, 15, 25	32-pin PLCC (RJ)

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FIFO PRODUCT OFFERINGS

Asynchronous Mature FIFOs

DEVICE	ORGANIZATION	SPEED SORT t_c (ns)	MAXIMUM FREQUENCY (MHz)	ACCESS TIME (ns)	PACKAGE
SN74ACT7200L SN74ACT7201LA SN74ACT7202LA SN74ACT7203L SN74ACT7204L	256 × 9	−15, −25, −50	67, 40, 20	10, 12, 20	28-pin DIP (NP) 28-pin SOIC (DV) 32-pin PLCC (RJ)
	512 × 9, 1K × 9	−15, −25, −35, −50	67, 50, 40, 20	10, 12, 15, 25	
	2K × 9	−15, −25, −50	67, 40, 20	10, 12, 20	
	4K × 9				
SN74ACT7205L	8K × 9	−15, −25, −50	67, 40, 20	10, 12, 20	28-pin DIP (NP)
SN74ACT7206	16K × 9	−15, −25, −50	67, 40, 20	10, 12, 20	32-pin PLCC (RJ)
SN74ALS2238	32 × 9 × 2		40		40-pin DIP (N) 44-pin PLCC (FN)
SN74ALS2233A	64 × 9		40		28-pin DIP (N) 44-pin PLCC (FN)
SN74ALS2232A	64 × 8		40		24-pin DIP (NT) 28-pin PLCC (FN)
SN74ALS235	64 × 5		25		20-pin DIP (N) 20-pin SOIC (DW)
SN74ALS233	16 × 5		30		20-pin DIP (N) 20-pin SOIC (DW)
SN74ALS232B	16 × 4		30		16-pin DIP (N) 16-pin SOIC (DW) 20-pin PLCC (FN)
SN74ALS229B	16 × 5		30		20-pin PLCC (FN) 20-pin DIP (N) 20-pin SOIC (DW)
SN74S225	16 × 5		10		20-pin DIP (N)

FIFO Functionality

DEVICE	Depth (bits)	Width (bits)	Access Time (ns)	High Sink Capability ($I_{OL} \geq 16$ mA)	3-State Outputs	Cascade for Memory Depth	Bidirectional	Dual Independent FIFO	5-V/3.3-V Counterparts	Flag Programming	Serial Flag Programming	Microprocessor Interface-Control Logic	Mailbox Bypass	Parity Generate	Parity Check	Read Retransmit	Synchronous Read Retransmit	Byte Swapping	Bus Matching	Programmable Depth	Multiple Queues
SN74ACT2226	64	1	20	✔		✔		✔													
SN74ACT2227	64	1	9	✔	✔	✔		✔													
SN74ACT2228	256	1	20	✔		✔		✔													
SN74ACT2229	256	1	9	✔	✔	✔		✔													
SN74ALS232	16	4	23	✔	✔																
SN74ALS234	64	4	17	✔	✔	✔															
SN74ALS236	64	4	17	✔	✔	✔															
SN74ALS229	16	5	30	✔	✔																
SN74ALS233	16	5	30	✔	✔																
SN74S225	16	5	75	✔	✔	✔															
SN74ALS235	64	5	17	✔	✔	✔															
SN74ALS2232	64	8	26	✔	✔																
SN74ALS2238	32	9	33	✔	✔		✔													✔	
SN74ALS2233	64	9	26	✔	✔																
SN74ACT7200	256	9	15		✔	✔										✔					
SN74ACT72211	512	9	10		✔					✔											
SN74ACT7201	512	9	15		✔	✔										✔					
SN74ACT72221	1K	9	10		✔					✔											
SN74ACT2235	1K	9	25	✔	✔		✔			✔											
SN74ACT2236	1K	9	25	✔	✔		✔			✔											
SN74ACT7202	1K	9	15		✔	✔										✔					
SN74ACT7807	2K	9	12	✔	✔	✔				✔											
SN74ACT72231	2K	9	10		✔					✔											
SN74ACT7808	2K	9	15	✔	✔	✔				✔											
SN74ACT7203	2K	9	15		✔	✔										✔					
SN74ACT72241	4K	9	10		✔					✔											
SN74ACT7204	4K	9	15		✔	✔										✔					
SN74ACT7205	8K	9	15		✔	✔										✔					
SN74ACT7206	16K	9	15		✔	✔										✔					
SN74ACT7813	64	18	12	✔	✔	✔	*		✔	✔											

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FIFO Functionality (Continued)

DEVICE	Depth (bits)	Width (bits)	Access Time (ns)	High Sink Capability (I_{OL} ≥ 16 mA)	3-State Outputs	Cascade for Memory Depth	Bidirectional	Dual Independent FIFO	5-V/3.3-V Counterparts	Flag Programming	Serial Flag Programming	Microprocessor Interface-Control Logic	Mailbox Bypass	Parity Generate	Parity Check	Read Retransmit	Synchronous Read Retransmit	Byte Swapping	Bus Matching	Programmable Depth	Multiple Queues
SN74ALVC7813	64	18	13	✓	✓	✓	*		✓	✓											
SN74ACT7814	64	18	15	✓	✓				✓	✓											
SN74ALVC7814	64	18	18	✓	✓				✓	✓											
SN74ACT7805	256	18	12	✓	✓	✓	*		✓	✓											
SN74ALVC7805	256	18	13	✓	✓	✓	*		✓	✓											
SN74ACT7806	256	18	15	✓	✓				✓	✓											
SN74ALVC7806	256	18	18	✓	✓				✓	✓											
SN74ACT7803	512	18	12	✓	✓	✓	*		✓	✓											
SN74ALVC7803	512	18	13	✓	✓	✓	*		✓	✓											
SN74ACT7804	512	18	15	✓	✓				✓	✓											
SN74ALVC7804	512	18	18	✓	✓				✓	✓											
SN74ABT7819	512	18	9	✓	✓	✓	✓			✓		✓									
SN74ABT7820	512	18	12	✓	✓		✓			✓											
SN74ACT7881	1K	18	11	✓	✓	✓				✓											
SN74ACT7811	1K	18	15	✓	✓	✓				✓											
SN74ACT7802	1K	18	30	✓	✓					✓											
SN74ACT7882	2K	18	11	✓	✓	✓				✓											
SN74ACT7884	4K	18	11	✓	✓	✓				✓											
SN74ACT53861	4K	18	11	✓	✓	✓				✓										✓	✓
SN74ACT3638	512	32	11		✓	✓	✓			✓		✓	✓				✓				
SN74ABT3611	64	36	10		✓	✓				✓		✓	✓	✓	✓						
SN74ABT3613	64	36	10		✓	✓				✓		✓	✓	✓	✓			✓	✓		
SN74ABT3612	64	36	10		✓	✓	✓			✓		✓	✓	✓	✓						
SN74ABT3614	64	36	10		✓		✓			✓		✓	✓	✓	✓			✓	✓		
SN74ACT3622	256	36	11		✓	✓	✓			✓		✓	✓								
SN74ACT3631	512	36	11		✓	✓				✓	✓	✓	✓				✓				
SN74ACT3632	512	36	11		✓	✓	✓			✓		✓	✓								
SN74ACT3641	1K	36	11		✓	✓				✓	✓	✓	✓				✓				
SN74ACT3642	1K	36	11		✓	✓	✓			✓		✓	✓								
SN74ACT3651	2K	36	11		✓	✓				✓	✓	✓	✓				✓				

* Bidirectional configurable without additional logic

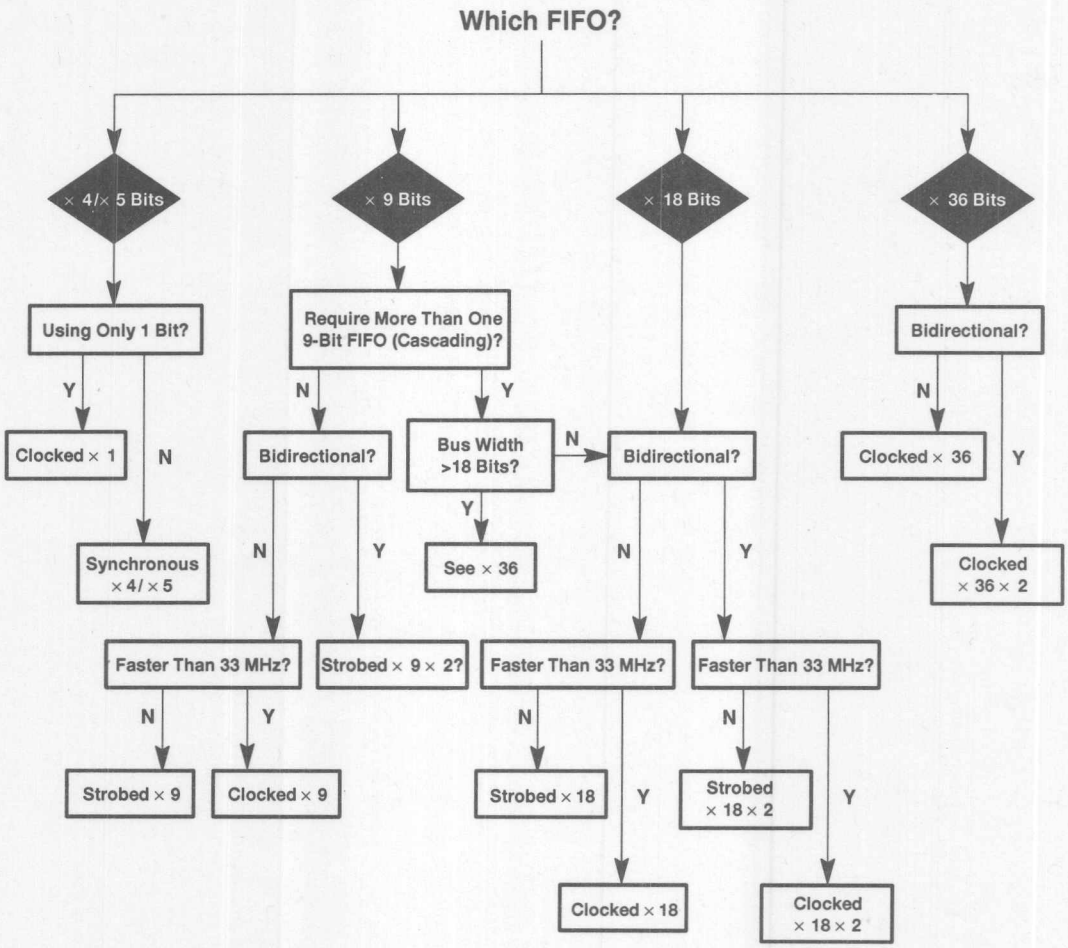
DEVICE	CPU	ROM (KB)	RAM (B)	Watchdog timer	Memory protection	Code security	Clock source	Max CPU frequency (MHz)	Wake-up from standby mode (µs)	Brownout detector	Supply voltage supervisor	Number of channels	Configurable delay	Sample and hold	Auto-scan	Window comparator	Differential inputs	Gain programmable	Offset programmable	Internal temperature sensor	Hardware multiply	Number of I/O pins	Number of timers	Number of UART serial ports	Number of SPI serial ports	Number of I²C serial ports	Hardware real-time clock	Number of comparators	Number of USCI modules	Number of hardware UARTs	Number of hardware SPIs	Number of hardware I²C	Number of ADC channels	Number of DAC channels	Number of DMA channels	LCD driver	Segment LCD	Embedded emulation	Package type
MSP430G2001	16	1	128	1			1	16	6													10	1																RHB20, TSSOP20
MSP430G2101	16	1	128	1			1	16	6													10	1																RHB20, TSSOP20
MSP430G2111	16	1	128	1			1	16	6													10	1																RHB20, TSSOP20
MSP430G2121	16	1	128	1			1	16	6													10	1																RHB20, TSSOP20
MSP430G2131	16	1	128	1			1	16	6													10	1																RHB20, TSSOP20
MSP430G2201	16	2	128	1			1	16	6													10	1																RHB20, TSSOP20
MSP430G2211	16	2	128	1			1	16	6													10	1																RHB20, TSSOP20
MSP430G2221	16	2	128	1			1	16	6													10	1																RHB20, TSSOP20
MSP430G2231	16	2	128	1			1	16	6													10	1																RHB20, TSSOP20
MSP430G2201	16	2	128	1			1	16	6													14	1																RGE24, TSSOP24
MSP430G2211	16	2	128	1			1	16	6													14	1																RGE24, TSSOP24
MSP430G2221	16	2	128	1			1	16	6													14	1																RGE24, TSSOP24
MSP430G2231	16	2	128	1			1	16	6													14	1																RGE24, TSSOP24
MSP430G2201	16	2	128	1			1	16	6													16	1																RSA16, QFN16
MSP430G2211	16	2	128	1			1	16	6													16	1																RSA16, QFN16
MSP430G2221	16	2	128	1			1	16	6													16	1																RSA16, QFN16
MSP430G2231	16	2	128	1			1	16	6													16	1																RSA16, QFN16
MSP430G2201	16	2	128	1			1	16	6													20	1																RHB20, TSSOP20
MSP430G2211	16	2	128	1			1	16	6													20	1																RHB20, TSSOP20
MSP430G2221	16	2	128	1			1	16	6													20	1																RHB20, TSSOP20
MSP430G2231	16	2	128	1			1	16	6													20	1																RHB20, TSSOP20
MSP430G2201	16	2	128	1			1	16	6													20	1																RSA16, QFN16
MSP430G2211	16	2	128	1			1	16	6													20	1																RSA16, QFN16
MSP430G2221	16	2	128	1			1	16	6													20	1																RSA16, QFN16
MSP430G2231	16	2	128	1			1	16	6													20	1																RSA16, QFN16
MSP430G2201	16	2	128	1			1	16	6													24	1																RGE24, TSSOP24
MSP430G2211	16	2	128	1			1	16	6													24	1																RGE24, TSSOP24
MSP430G2221	16	2	128	1			1	16	6													24	1																RGE24, TSSOP24
MSP430G2231	16	2	128	1			1	16	6													24	1																RGE24, TSSOP24
MSP430G2201	16	2	128	1			1	16	6													28	1																DA28, TSSOP28
MSP430G2211	16	2	128	1			1	16	6													28	1																DA28, TSSOP28
MSP430G2221	16	2	128	1			1	16	6													28	1																DA28, TSSOP28
MSP430G2231	16	2	128	1			1	16	6													28	1																DA28, TSSOP28
MSP430G2201	16	2	128	1			1	16	6													32	1																RHA32, QFN32
MSP430G2211	16	2	128	1			1	16	6													32	1																RHA32, QFN32
MSP430G2221	16	2	128	1			1	16	6													32	1																RHA32, QFN32
MSP430G2231	16	2	128	1			1	16	6													32	1																RHA32, QFN32
MSP430G2201	16	2	128	1			1	16	6													32	1																RSA32, QFN32
MSP430G2211	16	2	128	1			1	16	6													32	1																RSA32, QFN32
MSP430G2221	16	2	128	1			1	16	6													32	1																RSA32, QFN32
MSP430G2231	16	2	128	1			1	16	6													32	1																RSA32, QFN32
MSP430G2201	16	2	128	1			1	16	6													38	1																DL38, TSSOP38
MSP430G2211	16	2	128	1			1	16	6													38	1																DL38, TSSOP38
MSP430G2221	16	2	128	1			1	16	6													38	1																DL38, TSSOP38
MSP430G2231	16	2	128	1			1	16	6													38	1																DL38, TSSOP38
MSP430G2201	16	2	128	1			1	16	6													48	1																RGZ48, TSSOP48
MSP430G2211	16	2	128	1			1	16	6													48	1																RGZ48, TSSOP48
MSP430G2221	16	2	128	1			1	16	6													48	1																RGZ48, TSSOP48
MSP430G2231	16	2	128	1			1	16	6													48	1																RGZ48, TSSOP48
MSP430G2201	16	2	128	1			1	16	6													56	1																RSK56, QFN56
MSP430G2211	16	2	128	1			1	16	6													56	1																RSK56, QFN56
MSP430G2221	16	2	128	1			1	16	6													56	1																RSK56, QFN56
MSP430G2231	16	2	128	1			1	16	6													56	1																RSK56, QFN56
MSP430G2201	16	2	128	1			1	16	6													64	1																PM64, LQFP64
MSP430G2211	16	2	128	1			1	16	6													64	1																PM64, LQFP64
MSP430G2221	16	2	128	1			1	16	6													64	1																PM64, LQFP64
MSP430G2231	16	2	128	1			1	16	6													64	1																PM64, LQFP64

* Preliminary (product advisory applies)

FIFO Selection Flow Chart

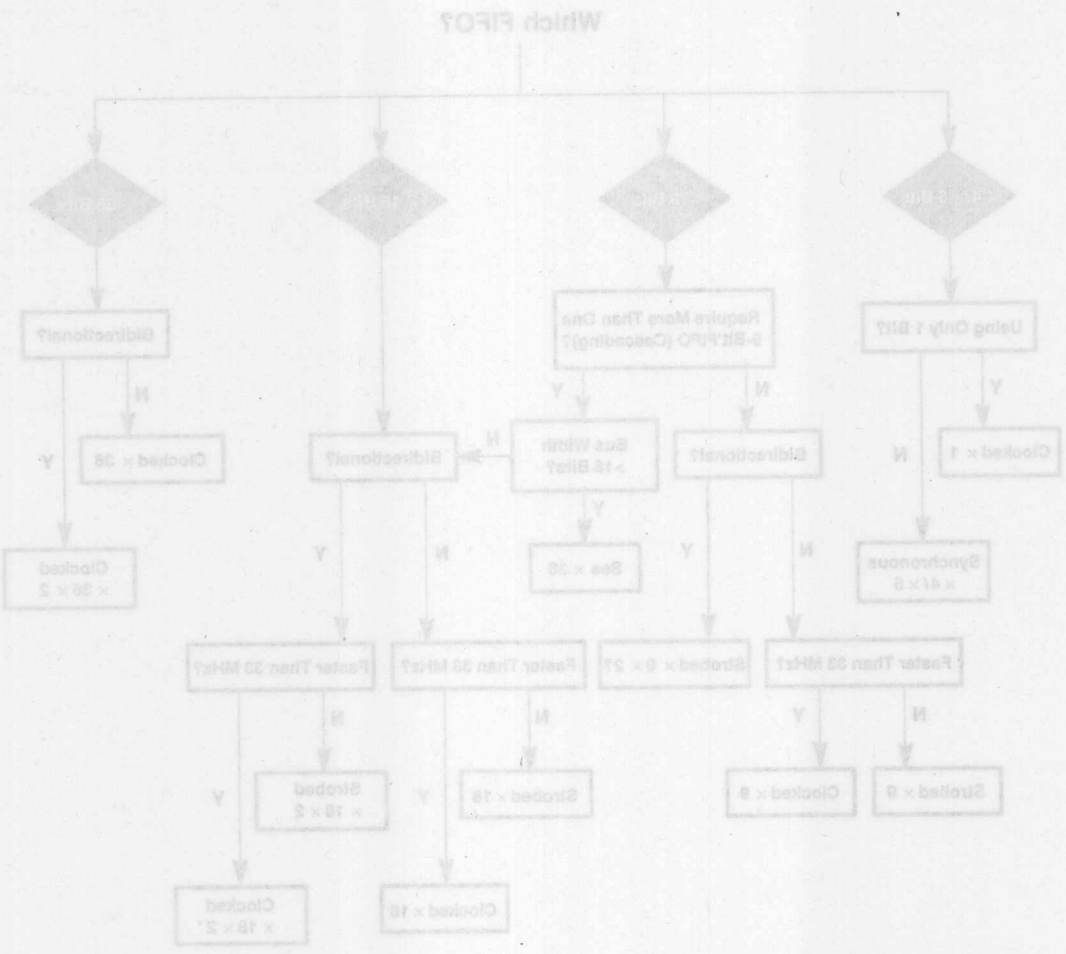
FIFO SELECTION FLOW CHART

This chart can be used to select the appropriate strobed or clocked FIFO for the application based on the desired FIFO width.



FIFO SELECTION FLOW CHART

This chart can be used to select the appropriate strobed or clocked FIFO for the application based on the desired FIFO width.



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FIFO Performance and Reliability

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Metastability Performance of Clocked FIFOs

First-In, First-Out Technology

Chris Wellheuser
Advanced System Logic – Semiconductor Group



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Introduction

This report is intended to help the user understand more clearly the issues relating to the metastable performance of Texas Instruments (TI) clocked FIFOs in asynchronous-system applications. It discusses basic metastable-operation theory, shows the equations used to calculate metastable failure rates for one and two stages of synchronization, and describes the approach TI has used for synchronizing the status flags on its series of clocked FIFOs. Additionally, a test setup for measuring the failure rate of a device to determine its metastability parameters is shown and results are given for both an advanced BiCMOS (ABT) FIFO and an advanced CMOS (ACT) FIFO. Using these parameters, calculations of MTBF under varying conditions are performed.

Metastability

Metastability in digital systems occurs when two asynchronous signals combine in such a way that their resulting output goes to an indeterminate state. A common example is the case of data violating the setup and hold specifications of a latch or a flip-flop. In a synchronous system, the data always has a fixed relationship with respect to the clock. When that relationship obeys the setup and hold requirements for the device, the output goes to a valid state within its specified propagation delay time. However, in an asynchronous system, the relationship between data and clock is not fixed; therefore, occasional violations of setup and hold times can occur. When this happens, the output may go to an intermediate level between its two valid states and remain there for an indefinite amount of time before resolving itself or it may simply be delayed before making a normal transition[1]. In either case, a metastable event has occurred.

Metastable events can occur in a system without causing a problem, so it is necessary to define what constitutes a failure before attempting to calculate a failure rate. For a simple CMOS latch, as shown in Figure 1, valid data must be present on the input for a specified period of time before the clock signal arrives (setup time) and must remain valid for a specified period of time after the clock transition (hold time) to assure that the output functions predictably. This leaves a small window of time with respect to the clock (t_0) during which the data is not allowed to change. If a data edge occurs within this aperture, the output may go to an intermediate level and remain there for an indefinite amount of time before resolving itself either high or low, as illustrated in Figure 2. This metastable event can cause a failure only if the output has not resolved itself by the time that it must be valid for use (for example, as an input to another stage); therefore, the amount of resolve time allowed a device plays a large role in calculating its failure rate.

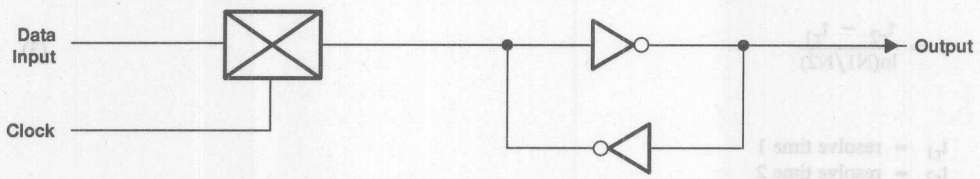


Figure 1. A Simple CMOS Latch

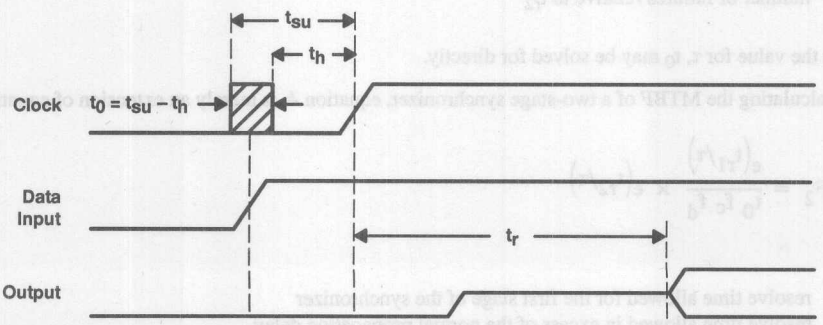


Figure 2. Output at Intermediate Level Due to Data Edge Within t_0 Aperture

The probability of a metastable state persisting longer than a time, t_r, decreases exponentially as t_r increases[2]. This relationship can be characterized by equation 1:

$$f_{(r)} = e^{(-t_r/\tau)} \tag{1}$$

where the function f(r) is the probability of nonresolution as a function of resolve time allowed, t_r, and the circuit time constant τ (which has also been shown to be inversely proportional to the gain-bandwidth product of the circuit)[3,4].

For a single-stage synchronizer with a given clock frequency and an asynchronous data edge that has a uniform probability density within the clock period, the rate of generation of metastable events can be calculated by taking the ratio of the setup and hold time window previously described to the time between clock edges and multiplying by the data edge frequency. This generation rate of metastable events coupled with the probability of nonresolution of an event as a function of the time allowed for resolution gives the failure rate for that set of conditions. The inverse of the failure rate is the mean time between failure (MTBF) of the device and is calculated with the formula shown in equation 2:

$$\frac{1}{\text{failure rate}} = \text{MTBF}_1 = \frac{e^{(t_r/\tau)}}{t_0\, f_c\, f_d} \tag{2}$$

Where:

t_r = resolve time allowed in excess of the normal propagation delay time of the device
t = metastability time constant for a flip-flop
t_0 = a constant related to the width of the time window or aperture wherein a data edge triggers a metastable event
f_c = clock frequency
f_d = asynchronous data edge frequency

The parameters t_0 and t are constants that are related to the electrical characteristics of the device in question. The simplest way to determine their values is to measure the failure rate of the device under specified conditions and solve for them directly. If the failure rate of a device is measured at different resolve times and plotted, the result is an exponentially decaying curve. When plotted on a semilogarithmic scale, this becomes a straight line the slope of which is equal to τ; therefore, two data points on the line are sufficient to calculate the value of τ using equation 3:

$$\tau = \frac{t_{r2} - t_{r1}}{\ln(N1/N2)} \tag{3}$$

Where:

t_{r1} = resolve time 1
t_{r2} = resolve time 2
N1 = number of failures relative to t_{r1}
N2 = number of failures relative to t_{r2}

After determining the value for τ, t_0 may be solved for directly.

The formula for calculating the MTBF of a two-stage synchronizer, equation 4, is merely an extension of equation 2:

$$\text{MTBF}_2 = \frac{e^{(t_{r1}/\tau)}}{t_0\, f_c\, f_d} \times e^{(t_{r2}/\tau)} \tag{4}$$

Where:

t_{r1} = resolve time allowed for the first stage of the synchronizer
t_{r2} = resolve time allowed in excess of the normal propagation delay
f_c, f_d, t, and t_0 are as previously defined, with t and t_0 assumed to be the same for both stages.

The first term calculates the MTBF of the first stage of the synchronizer, which in effect becomes the generation rate of metastable events for the next stage. The second term then calculates the probability that the metastable event will be resolved based on the value of t_{r2}, the resolve time allowed external to the synchronizer. The product of the two terms gives the overall MTBF for the two-stage synchronizer.

TI Clocked FIFOs

The TI clocked FIFOs are designed to reduce the occurrence of metastable errors due to asynchronous operation. This is achieved through the use of two- and three-stage synchronizing circuits that generate the status-flag outputs input ready (IR) and output ready (OR). In a typical application, words may be written to and then read from the FIFO at varying rates independent of one another, resulting in asynchronous flag-signal generation (internally) at the boundary conditions of full and empty; for example, the operation when the FIFO is at the full boundary condition with writes taking place faster than and asynchronous to reads. The IR flag is low, signifying that the FIFO is full and can accept no more words. When a read occurs, the FIFO is no longer completely full. This causes an internal flag signal to go high, allowing another write to take place. Since the exit from the full state happens asynchronously to the write clock (WRTCLK) of the FIFO, this flag is not useful as a system write-enable signal. The solution is to synchronize this internal flag to the write clock through two D-type flip-flop stages and output this synchronized signal as the IR flag (see Figure 3). The OR status flag is generated in a similar manner at the empty boundary condition and is synchronized to the read clock through a three-stage synchronizing circuit.

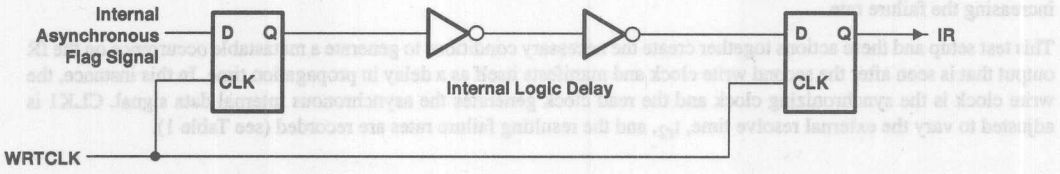


Figure 3. IR-Flag Synchronizer

The remainder of this report pertains to the metastability performance of the two-stage IR synchronizer, which is the limiting case of the two in terms of MTBF characteristics. The internal flag signal that goes high on a read and low on a write is synchronized to the write clock through two D-type flip-flop stages. Since this results in the IR flag status of the FIFO being delayed for two clock cycles, a predictive circuit is used to clock the status into the synchronizer at (full minus two) words so that the action of the IR flag going low coincides with the actual full status of the FIFO. However, once the FIFO is full and IR is low, a read that causes the internal flag to go high is not reflected in the status of the IR flag until two write clocks occur.

With the FIFO full and the IR flag low, a read causes the internal flag signal to go high. This signal is clocked into the first stage of the two-stage synchronizer on the next write clock. Because these two signals are asynchronous to one another, the potential for the output of the first stage of the synchronizer to go to a metastable state exists. If this condition persists until the next write clock rising edge, a metastable condition could be generated in the second stage and reflected on the IR flag output. This metastable condition manifests itself as a delay in propagation time and is considered a failure only if it exceeds the maximum delay allowed in a design.

The effectiveness of the two-stage synchronizer becomes apparent when attempting to generate failures at a rate high enough to count in a reasonable period of time. A metastable event generated in the first stage must persist until the next write clock, i.e., when that data is transferred to the second stage. The resolve time for the first stage is governed by the frequency or period of the write clock. At slower frequencies, the failure rate of the first stage is very low, resulting in a low metastable generation rate to the second stage. The second stage of the synchronizer further reduces the probability of a metastable failure based on the resolve time allowed at the output. The overall failure rate of the device may be affected by increasing the initial asynchronous data generation rate (adding jitter to the data centered about the setup and hold window), by decreasing the resolve time of the first stage (increasing the write clock frequency), and by reducing the external resolve time at the output.

Test Setup for Measuring FIFO Flag Metastability

The failure rate of a device is measured on a test fixture as shown in Figure 4. The input waveforms used on this setup are also shown in Figure 4. Rising data is jittered asynchronously about the setup and hold aperture of the device under test (DUT) in a ±400-ps window with respect to the device clock (CLK). The output of the DUT is then clocked into two separate flip-flops, FF1 and FF2, by two different clock signals, CLK1 and CLK2. The resolve time, t_r, is set by the relationship between CLK1 and CLK and is measured as the delta between the normal output transition time and the rising edge of CLK1 minus the setup time required for FF1. CLK2 occurs long enough after CLK1 to allow sufficient time for the DUT to have resolved itself to a valid state. The outputs of FF1 and FF2 are compared by the exclusive OR gate, the output state of which is latched into FF3 by CLK3. When a metastable failure occurs, the output of the exclusive OR gate goes high caused by FF1 and FF2 having opposite data due to the DUT not having resolved itself by time t_r. On the next cycle, low data is clocked into the DUT and FF1 and FF2 in order to reset the status latch, FF3. Failures are counted for different resolve times, and τ is then calculated using equation 3.

Using the test setup in Figure 4, failure rates are measured for both an SN74ABT7819, 512 × 18 × 2 clocked FIFO, and an SN74ACT7807, 2K × 9 clocked FIFO. The device is initially written full to set IR low at the boundary condition. A read clock is generated to send the internal flag high, and a jitter signal is superimposed on it to sweep asynchronously with respect to the write clock in an 800-ps-wide envelope and centered such that the IR flag goes high alternately on the second and third write clocks. The nominal write-clock frequency of the test setup is 40 MHz, but to increase the failure rate to an observable level, a pulse is injected into the write-clock stream just after the read clock occurs such that the first and second write clocks (the ones that clock the status through the synchronizer) are only 5.24 ns apart. This increases the effective write clock frequency to 191 MHz, reducing the resolve time allowed in the first stage and increasing the failure rate.

This test setup and these actions together create the necessary conditions to generate a metastable occurrence on the IR output that is seen after the second write clock and manifests itself as a delay in propagation time. In this instance, the write clock is the synchronizing clock and the read clock generates the asynchronous internal data signal. CLK1 is adjusted to vary the external resolve time, t_{r2}, and the resulting failure rates are recorded (see Table 1).

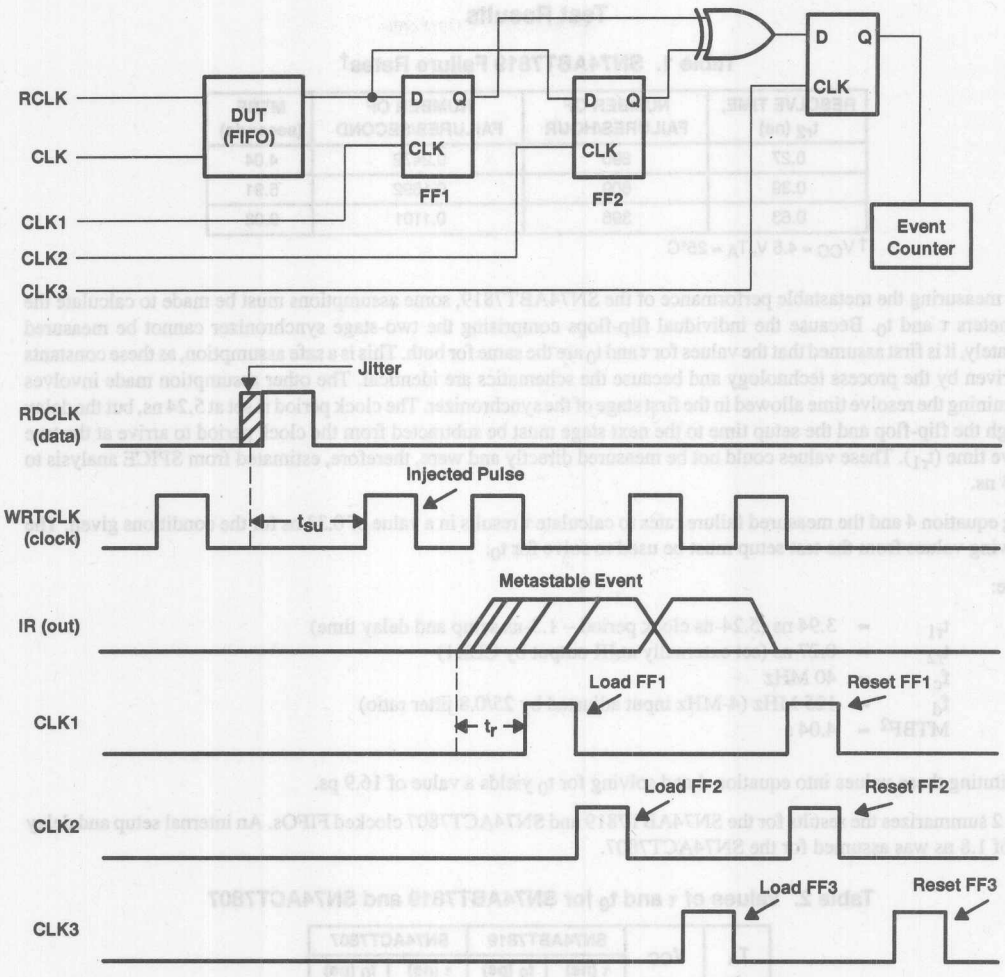


Figure 4. Metastable Event Counter and Input Waveforms

Test Results

Table 1. SN74ABT7819 Failure Rates†

RESOLVE TIME, t_{r2} (ns)	NUMBER OF FAILURES/HOUR	NUMBER OF FAILURES/SECOND	MTBF (seconds)
0.27	890	0.2472	4.04
0.39	609	0.1692	5.91
0.53	396	0.1101	9.08

† V_{CC} = 4.5 V, T_A = 25°C

After measuring the metastable performance of the SN74ABT7819, some assumptions must be made to calculate the parameters τ and t_0. Because the individual flip-flops comprising the two-stage synchronizer cannot be measured separately, it is first assumed that the values for τ and t_0 are the same for both. This is a safe assumption, as these constants are driven by the process technology and because the schematics are identical. The other assumption made involves determining the resolve time allowed in the first stage of the synchronizer. The clock period is set at 5.24 ns, but the delay through the flip-flop and the setup time to the next stage must be subtracted from the clock period to arrive at the true resolve time (t_{r1}). These values could not be measured directly and were, therefore, estimated from SPICE analysis to be 1.3 ns.

Using equation 4 and the measured failure rates to calculate τ results in a value of 0.33 ns for the conditions given. The following values from the test setup must be used to solve for t_0:

Where:

t_{r1} = 3.94 ns (5.24-ns clock period – 1.3-ns setup and delay time)
t_{r2} = 0.27 ns (set externally at IR output by CLK1)
f_c = 40 MHz
f_d = 125 MHz (4-MHz input adjusted by 25/0.8 jitter ratio)
$MTBF^2$ = 4.04 s

Substituting these values into equation 4 and solving for t_0 yields a value of 16.9 ps.

Table 2 summarizes the results for the SN74ABT7819 and SN74ACT7807 clocked FIFOs. An internal setup and delay time of 1.8 ns was assumed for the SN74ACT7807.

Table 2. Values of τ and t_0 for SN74ABT7819 and SN74ACT7807

T_A	V_{CC}	SN74ABT7819		SN74ACT7807	
		τ (ns)	t_0 (ps)	τ (ns)	t_0 (ps)
25°C	4.5 V	0.33	16.9	0.50	1.13
	5 V	0.30	7	0.40	2.05
	5.5 V	0.23	28.8	0.30	9.40

These numbers indicate the performance of only a few devices and are not intended to represent a fully characterized parameter. However, they should be valid for the purpose of relative performance comparisons, and the values do fall within the expected range given the circuit configuration and process technology in which the devices are fabricated.

MTBF Comparisons

With the constants τ and t_0 now known, calculations of the MTBF of the device under different operating conditions may be performed. First, however, consider an example of the metastability performance of a single-stage synchronizer using equation 1 and the circuit constants τ and t_0 from Table 2. Assume an application running with a 33-MHz write clock, an 8-MHz read clock, a 9-ns maximum propagation delay time for the IR path, and a 5-ns setup time for IR to the next device. Therefore:

t_r = 16 ns (30-ns clock period – 9-ns propagation delay – 5-ns t_{su})
f_c = 33 MHz
f_d = 8 MHz

Using equation 2 to calculate the MTBF gives 2.55 y 10^{17} seconds or a little bit more than 8 billion years.

The reliability of a one-stage synchronizer degrades as operating frequency increases. With a 50-MHz write clock, a 12-MHz read clock, a 9-ns maximum delay, and a 5-ns setup time:

t_r = 6 ns (20-ns clock period – 9-ns propagation delay – 5-ns t_{su})
f_c = 50 MHz
f_d = 12 MHz

Substituting these values into equation 2 yields an MTBF of about 2 hours. This performance is unacceptable, even with a device fabricated in the 0.8-mm BiCMOS process, which is more resistant to metastability than other processes.

The benefits of two-stage synchronization become evident with the next example. Using the conditions stated in the last example:

t_{r1} = 18.7 ns (20-ns clock period – 1.3-ns setup and delay time)
t_{r2} = 6 ns (20-ns clock period – 9-ns propagation delay – 5-ns t_{su})
f_c = 50 MHz
f_d = 12 MHz

Using equation 4 to calculate the MTBF gives 3.16 y 10^{28} seconds or 1.00 y 10^{21} years.

Table 3 gives a performance summary of both one- and two-stage synchronizing solutions under different conditions.

Table 3. MTBF Comparisons†

CONDITIONS	ACT 1 STAGE	ABT 1 STAGE	ACT 2 STAGE	ABT 2 STAGE
f_c = 33 MHz, f_d = 8 MHz	8400 years	8.1×10^9 years	2.62×10^{28} years	4.77×10^{47} years
f_c = 40 MHz, f_d = 10 MHz	92 days	1400 years	3.56×10^{19} years	2.18×10^{34} years
f_c = 50 MHz, f_d = 12 MHz		2 hours	4.90×10^{10} years	1.00×10^{21} years
f_c = 67 MHz, f_d = 16 MHz			417 years	1.28×10^9 years
f_c = 80 MHz, f_d = 20 MHz				2900 years

† Assumptions for the MTBF comparisons:
– The values for t_0 and τ are those given previously for both the ABT and ACT devices with V_{CC}= 4.5 V, T_A = 25°C.
– Flag propagation delay time (IR or OR) is assumed to be 9 ns.
– Setup times to the next device are 5 ns (up to 50-MHz operation), 4 ns (up to 67-MHz operation), and 3 ns (up to 80-MHz operation).

Conclusion

Metastability failures must be accounted for in the design of asynchronous digital circuits. These failures become increasingly prevalent at higher operating frequencies. When higher frequencies are used, extreme care must be taken to ensure that system reliability is not adversely affected due to inadequate synchronization methods.

Clocked FIFOs from TI provide a solution to this problem by synchronizing the boundary flags with at least two flip-flop stages to improve the metastable MTBF over one-stage synchronization. This architecture allows designers to utilize the high-throughput performance of the memory without endangering the reliability of their end products.

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FIFO Memories: Solution to Reduce FIFO Metastability

First-In, First-Out Technology

Tom Jackson
Advanced System Logic – Semiconductor Group

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As system operating frequencies continue to increase in excess of 33 MHz, designers must begin to address the issues of overall system reliability due to increased chance of a metastable event occurring. A metastable event is defined as the time period when the output of a logic device is neither at a logic high nor at a logic low but rather in an indeterminate level. The chance of a metastable occurrence is exponentially increased if single-stage synchronization is employed, as in the case of the '722xx synchronous-style devices versus the two-stage synchronization that is implemented by Texas Instruments (TI) (see Figure 1). The following information assists designers in understanding and improving upon the metastable characteristics of '722xx synchronous-style devices and their reliability.

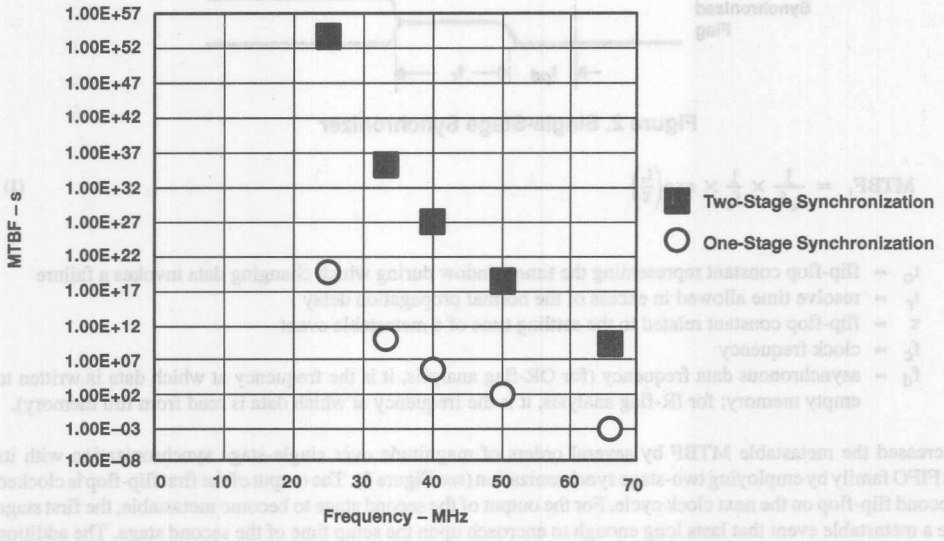


Figure 1. MTBF for Metastability as a Function of Frequency

Metastability may occur when using a FIFO to synchronize two digital signals operating at different frequencies. This type of application is a familiar one to many design engineers. Triggering a metastable event is common in single-stage (single flip-flop) synchronized FIFOs that are used to synchronize different clock signals (see Figure 2). With this method, the asynchronous input might change states too close to the clock transition, violating the flip-flop's setup and hold times. This causes an increase in resolve time (t_r) which then results in an overall increase in propagation delay (t_{pd}). Once a metastable event is triggered, the probability of the output recovering to a high or low level increases exponentially with the increased resolve time. The expected time until the output of a single flip-flop with asynchronous data has a metastable event is described by the mean time between failure (MTBF) equation (see equation 1). The first term of the equation is the probability that the asynchronous data will trigger a metastable event. The second term is the data rate. The third and final term is the probability of the metastable event recovering given the resolve time. A linear increase in resolve time exponentially increases the MTBF of a metastable event.

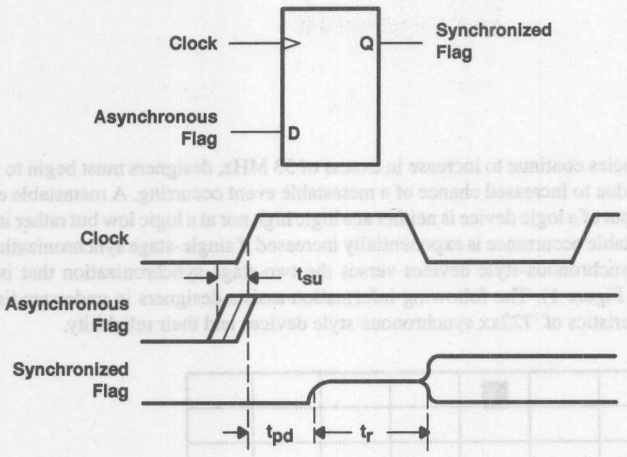


Figure 2. Single-Stage Synchronizer

$$MTBF_1 = \frac{1}{t_o f_c} \times \frac{1}{f_d} \times \exp\left(\frac{t_r}{\tau}\right) \quad (1)$$

Where:

t_o = flip-flop constant representing the time window during which changing data invokes a failure
t_r = resolve time allowed in excess of the normal propagation delay
τ = flip-flop constant related to the settling time of a metastable event
f_c = clock frequency
f_d = asynchronous data frequency (for OR-flag analysis, it is the frequency at which data is written to empty memory; for IR-flag analysis, it is the frequency at which data is read from full memory).

TI has increased the metastable MTBF by several orders of magnitude over single-stage synchronization with its advanced FIFO family by employing two-stage synchronization (see Figure 3). The output of the first flip-flop is clocked into the second flip-flop on the next clock cycle. For the output of the second stage to become metastable, the first stage must have a metastable event that lasts long enough to encroach upon the setup time of the second stage. The addition of the second flip-flop to the single-stage synchronizer allows the flip-flops more time to resolve any metastable output. This is statistically equivalent to increasing its resolve time by the clock period minus its propagation delay. MTBF for a two-stage synchronizer is given in equation 2. All terms, except for the third one, are the same as in equation 1. The third term represents the additional propagation delay through the added flip-flop.

$$MTBF_2 = \frac{1}{t_o f_c} \times \frac{1}{f_d} \times \exp\left[\frac{\frac{1}{f_c} - t_{pd}}{\tau}\right] \times \exp\left(\frac{t_r}{\tau}\right) \quad (2)$$

t_{pd} = propagation delay through the first flip-flop
$MTBF_2 = MTBF_1$

Where:

$t_r = t_r + (1/f_c - t_{pd})$

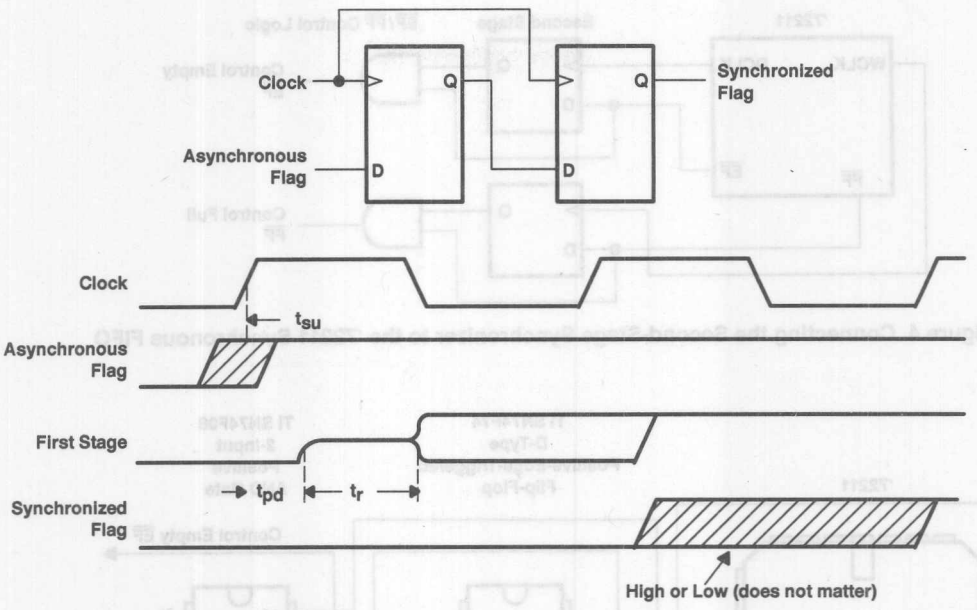


Figure 3. Two-Stage Synchronizer

The functional block diagram in Figure 4 illustrates the connections necessary to add the second-stage synchronization to the '72211 synchronous FIFO. A quick and inexpensive schematic to resolve metastability of a synchronous FIFO is shown in Figure 5. In this case, the FIFO is the '72211LJ and, by implementing a single TI SN74F74 D-type positive-edge-triggered flip-flop and a TI SN74F08 two-input positive AND gate, the metastability characteristics of this circuit can be dramatically improved. The TI SN74F74 acts as the second stage for this circuit, increasing the resolve time as described in the previous paragraphs. The TI SN74F08 is implemented to act as the control-empty and control-full flags to the receiving device. These control lines of the first-stage and second-stage synchronized flags are then ANDed together to create the control flags (control empty and control full). The control lines are essentially read enables that ensure the synchronization of the device. As is shown in the logic diagram and truth table, synchronization is complete only when the empty flags ($\overline{EF}$) of both the second stage (truth table input A) and the device (truth table input B) are high. The empty flag is used for read control and the full flag ($\overline{FF}$) is used for write control. If either flag from the synchronizer or the device is held low or becomes metastable, a read is not permitted (truth table output Y) until the write flag is synchronized.

As can be seen in today's digital systems, synchronous and asynchronous operations can and will produce random errors due to metastability in single-stage FIFO designs like those of the '722xx synchronous FIFO family. The described method of implementing a second stage for flag synchronization is extremely useful for clock speeds that are either approaching or exceeding 33 MHz. Metastability can be virtually eliminated in the '722xx synchronous FIFO family by the simple addition of a second flip-flop. The second-stage synchronizer greatly reduces metastability, thereby increasing the MTBF and allowing designers to use faster microprocessors and higher data-transfer rates for greater overall system performance and reliability.

To reduce metastability and improve system reliability, TI offers a complete line of high-performance FIFO memory devices. TI's FIFOs have dual-stage synchronization designed onto each chip. This eliminates the need for any external discrete solution and reduces critical board space by fully utilizing TI's family of fine-pitch surface-mount packaging.

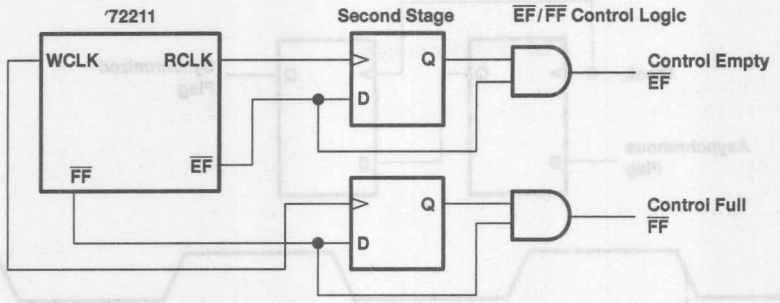
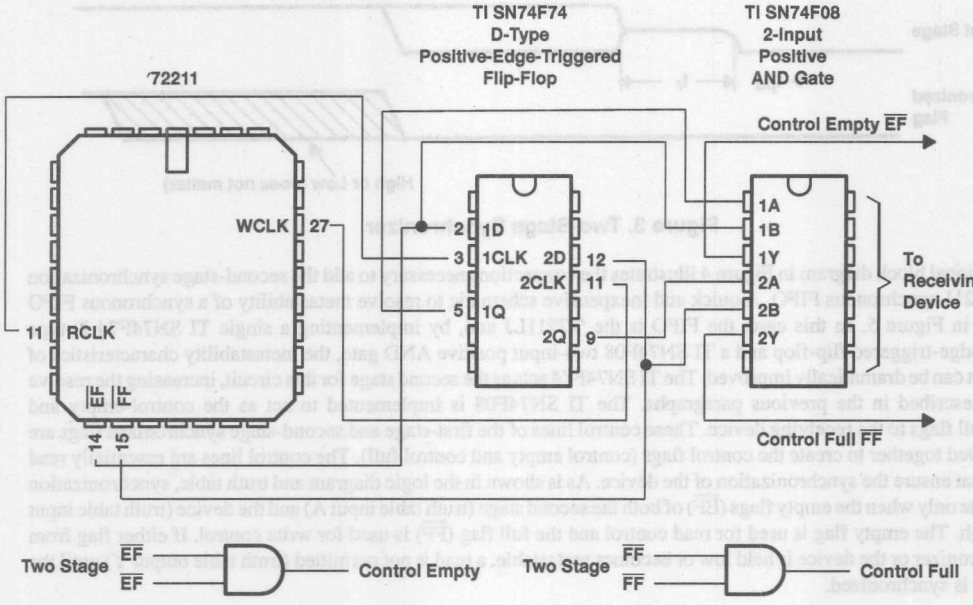


Figure 4. Connecting the Second-Stage Synchronizer to the '72211 Synchronous FIFO



INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

Figure 5. Resolving Metastability of a Synchronous FIFO

Simultaneous-Switching Noise Analysis for Texas Instruments FIFO Products

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Abstract

Analysis of circuit-noise immunity during simultaneous switching of multiple outputs is crucial in the high-speed advanced logic families including ACT and ABT FIFO products. Consequently, reduction of simultaneous-switching noise is of the utmost concern to the FIFO design team at Texas Instruments (TI). TI offers reliable FIFO products that meet the fast-speed requirement of today's technology. In this application report, a thorough explanation of noise-reduction techniques for TI's FIFO devices is provided. This report assists component and system design engineers in their evaluations of simultaneous-switching noise for TI's ACT and ABT FIFO products.

Introduction

One concern in advanced integrated circuit (IC) design is the challenge of minimizing simultaneous-switching noise while increasing switching speed of the device. This application report presents the achievements TI has made in providing very high-speed FIFO products with minimum simultaneous-switching noise.

This report provides an introduction to advanced CMOS simultaneous-switching noise and the approaches taken by the FIFO design group to effectively reduce the noise. Test procedures for measuring noise during simultaneous switching of multiple outputs are also presented. Test results provide the data necessary to ensure proper operation of the FIFO during simultaneous switching of multiple outputs.

In high-speed, high-density CMOS VLSI devices, many output drivers may switch simultaneously. During the transition, the excessive current drawn from the power supply can produce a significant amount of power/ground noise called simultaneous-switching noise (SS noise). The noise may be generated in the package V_{DD}/V_{SS} planes and also in the internal (on-chip) V_{DD}/V_{SS} buses. Figure 1 shows the power/ground noise coupling through a dc-on driver to external circuitry.

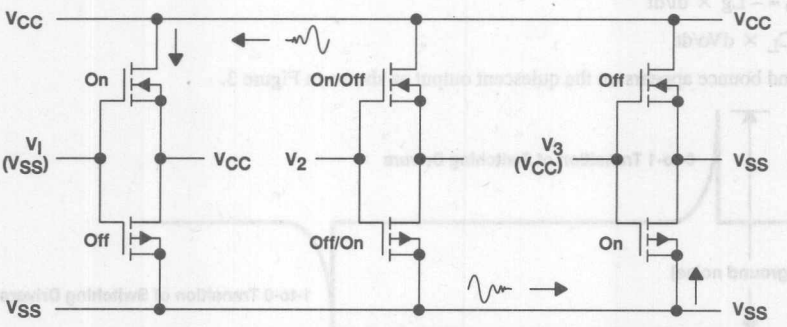


Figure 1. Power/Ground Noise Coupling Through a dc-on Driver to External Circuitry[1]

A simultaneous-switching scenario where several drivers switch at the same time is shown in Figure 2. The electrical path from the ground/power IC pads to the package terminals is inductive as shown in Figure 2. The IC pads are connected through bonding wires to the package pads that are connected through a multilayer package to the package terminals, which, in turn, are connected to ground/power planes on the printed circuit board (PCB). All of these different elements in the packaging of the IC behave as inductances with negligible resistive components. [2]

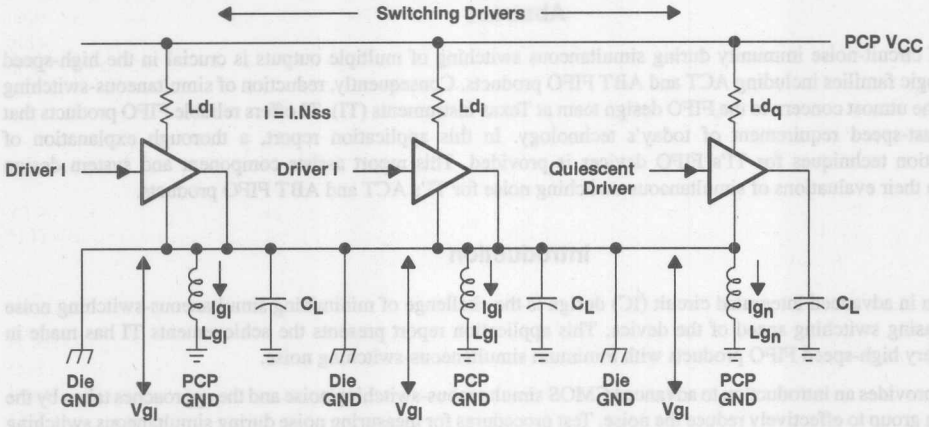


Figure 2. Simultaneous Switching[2]

The physics of the device package plays a fundamental role in the voltage-noise spike. The major effect on a high-speed device is the induced voltage on the GND and V_{CC} terminals caused by the transient currents from switching capacitive loads.[3] If only one output is switched, the ground noise is calculated by equation 1 where Lg is the inductance of the ground terminal due to the bond wire, lead, and via, and di/dt is the time rate of change in transient current driving the capacitive load. Equation 2 illustrates transient current where dVo/dt is the change of output voltage in time.

$$V_{GND} = -Lg \times di/dt \quad (1)$$

$$i(t) = C_L \times dVo/dt \quad (2)$$

The induced ground bounce appears on the quiescent output as shown in Figure 3.

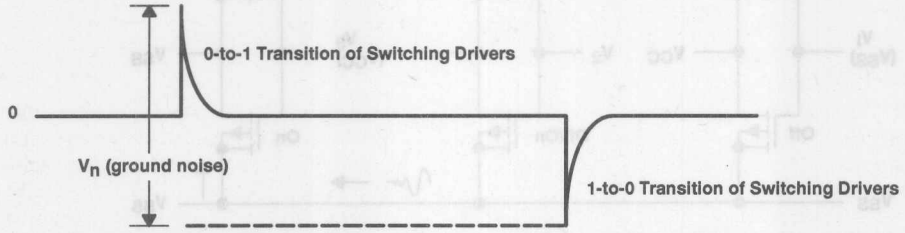


Figure 3. Example of Ground-Bounce Waveform[2]

When the number of simultaneously switching outputs increases, ground noise increases. For large ICs, the relationship between ground-bounce amplitude and the number of switching drivers is no longer linear. [1, 2, 4]

Unless these power/ground noise fluctuations are controlled, simultaneous-switching noise can degrade or even limit system performance. Uncontrolled noise spikes can lead to loss of stored data, severe speed degradation, output glitches, and reduction in system-noise immunity.[3] From a functional perspective, ground bounce reduces noise margins of the gate and may cause false switching of quiet gates. Noise margins for the low state are usually smaller than noise margins for the high state; therefore, noise of the ground bus in the IC concerns designers the most. [2, 5]

Several techniques have been proposed for reducing simultaneous-switching noise. At the package level, one approach is to reduce the inductance by improved packaging techniques, such as decreasing the various inductive contributions

to ground bounce.[2] Surface-mount packages, such as PQFPs, are a better package option than through-hole packages, such as DIP or PGA, because the former have shortened pins or a lower-profile package. Another approach is to decrease the inductance of the ground pins by placing as many ground/power pins in the package as possible.[1, 2] At the design level, some designers have proposed output edge control (OEC™) as a solution to reduce noise.[4]

At the circuit level, simultaneous-switching noise can be reduced by skewing the output drivers and/or by damping out power and ground noise with additional damping resistors at the source end of both p- and n-channel transistors of output drivers,[3] and/or by adding bypass capacitors that reduce the current noise associated with output buffers driving off-chip loads.[4] This application report concentrates only on TI's approaches to reduce the simultaneous-switching noise in high-performance advanced FIFO products.

TI Solution for Simultaneous-Switching Noise

TI's solutions to minimize noise caused by simultaneous switching of outputs include reducing package inductance by using multiple ground pins, controlling the output edge, and separating the ground pins. Measurements used by TI in evaluating the chip's performance are included in the following discussion.

Reducing Package Inductance

To reduce voltage spikes, the value of lead inductance (Lg) in equation 1 should be lowered. Lead inductance is dependent upon lead lengths as well as the location of GND/V_{CC} pins in the package. Decreasing the overall size of the FIFO package lowers the package inductance. The inductance value per pin for most of the package types used for FIFO products is shown in Table 1. TI's current technology has provided high-performance 9-, 18-, and 36-bit FIFO products with less inductance per pin, giving TI a performance edge in the FIFO market. More information on TI package types is provided in Appendix B.

Table 1. Inductance Value per Pin for Most Package Types Used for FIFO Products

PITCH	PACKAGE TYPE	FIFO TYPE	INDUCTANCE PER PIN (nH)
Standard-Pitch Option	24-pin DIP	4-, 5-, 8-, and 9-bit FIFO	3–15
	28-pin DIP	9-bit (IDT) FIFO	2–15
	44-pin PLCC	9-bit FIFO	6–8
	28-pin SOIC	1-bit FIFO	3–8
Fine-Pitch Option	120-pin TQFP	36-bit FIFO	4–5
	80-pin TQFP	18-bit FIFO	5
	64-pin TQFP	9-bit FIFO	3–4

Multiple GND and V_{CC} Pins

By adding more GND and V_{CC} pins on a chip, TI offers advanced FIFO products with lower noise compared to other products with only one GND and one V_{CC} corner pin. The previous section discussed simultaneous-switching noise being directly proportional to the inductance of the ground/power leads. Multiple ground/power pins improve the noise immunity of the chip by reducing the total ground/power lead inductance because the total inductance is a parallel combination of the lead inductances of the ground/power pins. For example, SN74ACT7814 FIFO memory in Figure 4 has four GND pins distributed among the outputs. The total ground-lead inductance of this chip is approximately one-fourth of that of a similar chip with only one GND pin. Assuming L_1, L_2, L_3, and L_4 are the lead inductances of the four ground pins on the chip, and assuming these inductances are equal, the combination of the parallel inductances is 1/4 of the inductance when only one GND pin is on the chip (see equation 3).

$$L_T = \frac{1}{\frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} + \frac{1}{L_4}} = \frac{L_1}{4} \quad (3)$$

OEC is a trademark of Texas Instruments Incorporated.

Multiple ground/power pins are used on all TI FIFO products. Table 2 shows the number of data output pins per ground pin for different FIFO products.

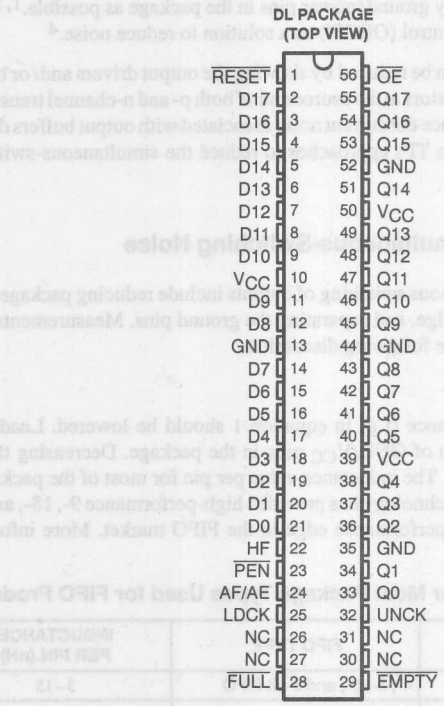


Figure 4. SN74ACT7814 FIFO With Multiple GND Pins

Table 2. Number of Data Output Pins per Ground Pin for Different FIFO Products

FIFO	FIFO PRODUCT	SIZE	PACKAGE TYPE	GND PINS	DATA OUTPUTS PER GND PIN
9 Bits	SN74ACT2335	102492	44-pin PLCC (FN)	4	4.5
			64-pin TQFP (PM)	12	1.5
	SN74ACT2236	102492	44-pin PLCC (FN)	4	4.5
	SN74ACT7807	20489	44-pin PLCC (FN)	6	1.5
			64-pin TQFP (PM)	12	0.75
18 Bits	SN74ACT7803	51218	(DL)	4	4.5
	SN74ACT7811	102418	68-pin PLCC (FN)	10	1.8
			80-pin TQFP (PN)	14	1.3
	SN74ABT7819	512182	80-pin QFP (PH)	14	2.6
			80-pin TQFP (PN)	14	2.6
32 Bits	SN74ACT3638	512322	120-pinTQFP (PCB)	14	4.6
			132-pin PQFP (PQ)	15	4.3
36 Bits	SN74ABT3614	64362	120-pin TQFP (PCB)	10	7.2
			132-pin PQFP (PQ)	18	4.0
	SN74ACT3632	512362	120-pin TQFP (PCB)	14	5.1
			132-pin PQFP (PQ)	14	5.1
	SN74ACT3641	102436	120-pin TQFP (PQ)	15	2.4
			132-pin PQFP (PCB)	15	2.4

Output Edge Control (OEC™) Method

OEC™ is another method for controlling simultaneous-switching noise. This is a circuit method that reduces the di/dt portion of equation 1. The output transistor is split into many small subtransistors with sequential turnon of each subtransistor. By splitting the total current into a series of smaller currents distributed over time, the effective di/dt is reduced. The delay in turnon of the successive subtransistors reduces the maximum peak di/dt for the entire output transistor.

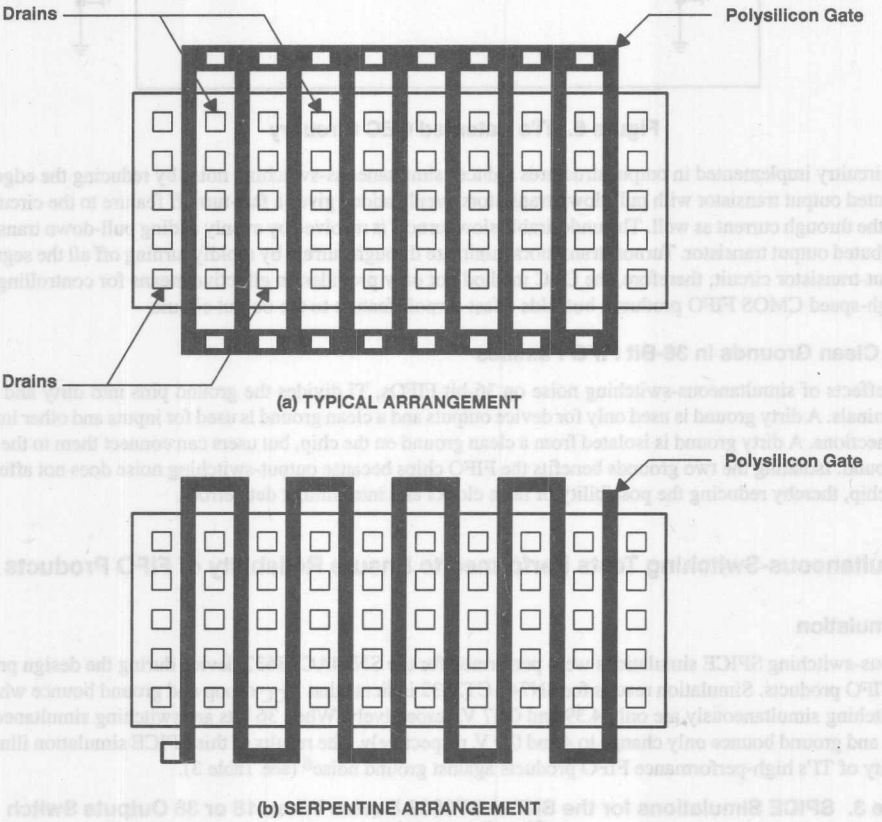


Figure 5. CMOS-Transistor-Gate Layout

At the output, the structure of the polysilicon gate is modified to grade the turnon by removing portions of the polysilicon gate to form a serpentine arrangement and by driving the gate from one end (see Figure 5). The resistance of the polysilicon and the capacitance of each gate segment form a distributed RC network that slows the turnon of each succeeding segment. Figure 6 shows the equivalent-circuit schematic for the distributed output transistor.[4]

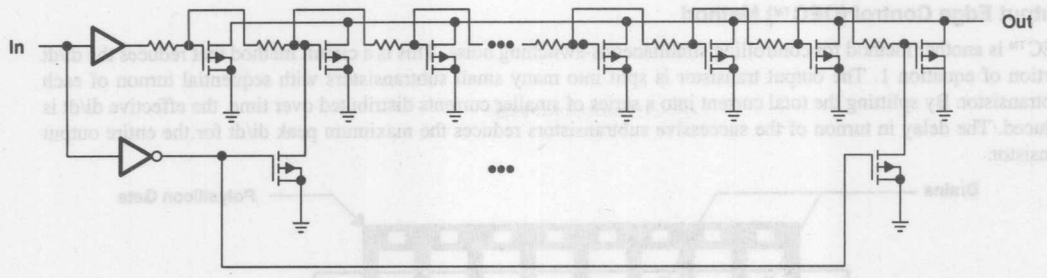


Figure 6. TI's Patented OEC Circuitry

The OEC circuitry implemented in output structures reduces simultaneous-switching noise by reducing the edge rate. The distributed output transistor with pull-down transistors evenly added gives a fast-turnoff feature to the circuit and minimizes the through current as well. The undesirable slow turnoff is resolved by evenly adding pull-down transistors to the distributed output transistor. Turnoff transistors minimize through current by rapidly turning off all the segments of the output-transistor circuit; therefore, the OEC method not only provides an effective means for controlling di/dt noise in high-speed CMOS FIFO products, but adds a fast-turnoff feature to the output circuit.

Dirty and Clean Grounds in 36-Bit FIFO Families

To reduce effects of simultaneous-switching noise on 36-bit FIFOs, TI divides the ground pins into dirty and clean ground terminals. A dirty ground is used only for device outputs and a clean ground is used for inputs and other internal circuit connections. A dirty ground is isolated from a clean ground on the chip, but users can connect them to the same external ground. Isolating the two grounds benefits the FIFO chips because output-switching noise does not affect the rest of the chip, thereby reducing the possibility of false clocks and intermittent data errors.

Simultaneous-Switching Tests Performed to Ensure Reliability of FIFO Products

SPICE Simulation

Simultaneous-switching SPICE simulations were performed for the SN74ACT3632 device during the design process for 36-bit FIFO products. Simulation results for SN74ACT3632 indicate that V_{CC} droop and ground bounce when 18 bits are switching simultaneously are only 4.39 and 0.67 V, respectively. When 36 bits are switching simultaneously, V_{CC} droop and ground bounce only change to 4 and 0.9 V, respectively. The results of this SPICE simulation illustrate the reliability of TI's high-performance FIFO products against ground noise[6] (see Table 3).

Table 3. SPICE Simulations for the SN74ACT3632 Device When 18 or 36 Outputs Switch Simultaneously

SN74ACT3632 SWITCHING SIMULTANEOUSLY	V_{CC} DROOP (V)	GROUND BOUNCE (V)
18 bits	4.39	0.67
36 bits	4.0	0.9

Ground/Power-Noise Measurements (V_{OLP} and V_{OHV})

Noise measurements evaluate the performance of FIFO products while simultaneously switching the outputs. A typical simultaneous-switching test is performed to determine the magnitude of the disturbance on the output that is not being switched, as well as stored data integrity for devices with multiple outputs. The voltage induced on a quiescent output during simultaneous switching is referred to as V_{OLP} and V_{OHV}. For V_{OLP} (V_{OHV}) measurements, the output under test is held low (high) while the rest of the outputs are switching from high to low (low to high). V_{OLP}, the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs, is measured with respect to a ground reference near the output under test. V_{OHV} is the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. Table 4 summarizes the V_{OLP} and V_{OHV} results for 36-bit FIFO products. Data was taken on an automatic test machine (HP 82000) at room temperature (25°C).

Table 4. Sample V_{OLP} and V_{OHV} Test Results for 36-Bit FIFO Products

DEVICE	V_{OLP} (V)	V_{OHV} (V)	V_{CC} (V)
SN74ABT3614	0.75	0.2	5.5
SN74ACT3632	1.0	1.4	5.0

The results of V_{OLP} and V_{OHV} measurements performed on TI's 36-bit FIFO products indicate the reliability and noise immunity of TI's high-performance FIFO products. Sample waveforms for SN74ACT3638, SN74ACT3611, and SN74ACT3613 are presented in Appendix A.

Special Test Performed on 36-Bit FIFOs (V_{IH} and V_{IL} Testing)

V_{IH} and V_{IL} values for 36-bit FIFO families are tested while outputs are simultaneously switching. For example, the SN74ACT3632 continues to function properly with V_{IH} and V_{IL} values shown in Table 5. These results show that separating the output ground from the ground used for the rest of the chip results in excellent input-noise margins for the 36- and 32-bit-wide FIFOs.

Table 5. Test Required for the 36-Bit SN74ACT3632

V_{CC}	4.5 V	5.5 V
V_{IH}	1.8 V	1.9 V
V_{IL}	1.3 V	1.3 V

Summary

Fast switching speeds in today's technology require solutions to problems such as simultaneous-switching noise. The fast switching of drivers can cause uncontrolled noise spikes on the chip's ground bus, which lead to false clocks or incorrect data and control signals on the device. As more outputs of an IC switch simultaneously, noise effects increase and limit the usefulness of the device.

Better packaging options, multiple ground/power pins, output edge control, and separating the ground pins as clean and dirty ground pins reduce the simultaneous-switching noise. Finally, results obtained from simultaneous-switching tests are provided to illustrate the noise immunity of TI's high-performance FIFO devices.

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2. Lilianan Diaz-Olavarrieta, "Ground Bounce in ASIC's: Model and Test Results," IEEE International Symposium on Electromagnetic Compatibility, 1991, Cherry Hill, NJ.
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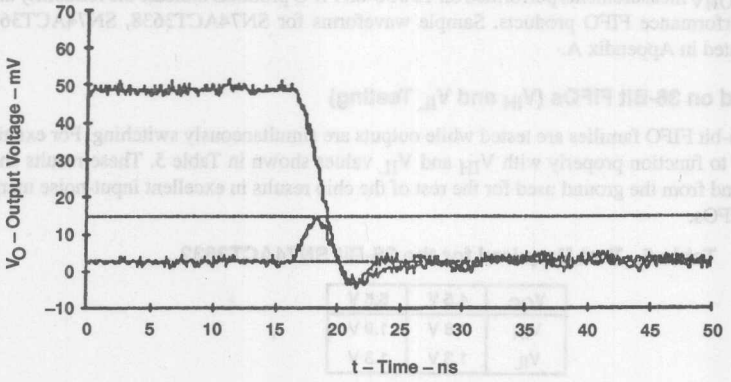
Acknowledgements

The V_{OLP} and V_{OHV} graphs in Appendix A are provided with the assistance of Al Sawyer.

Packaging information in Appendix B is provided by TI packaging engineers and organized by Tom Jackson.

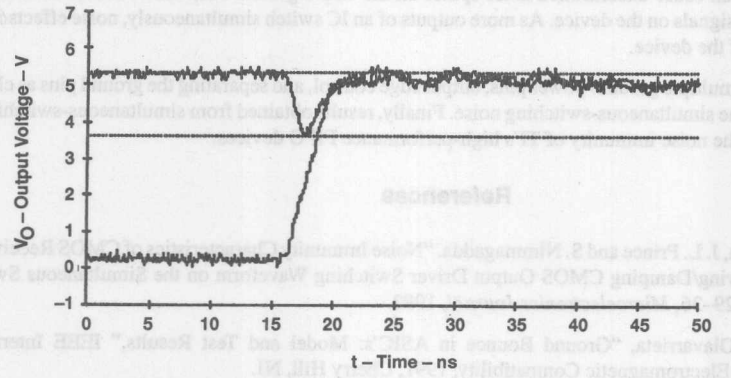
Appendix A

Appendix A shows V_{OLP} and V_{OHV} measurements during simultaneous switching. Measurements are made with respect to ground at 25°C with an HP8200 automatic test machine. V_1 is the quiescent voltage on the output being tested prior to switching other outputs. V_2 is the peak voltage on the output being tested while switching other outputs. V_D is the difference in V_1 and V_2.



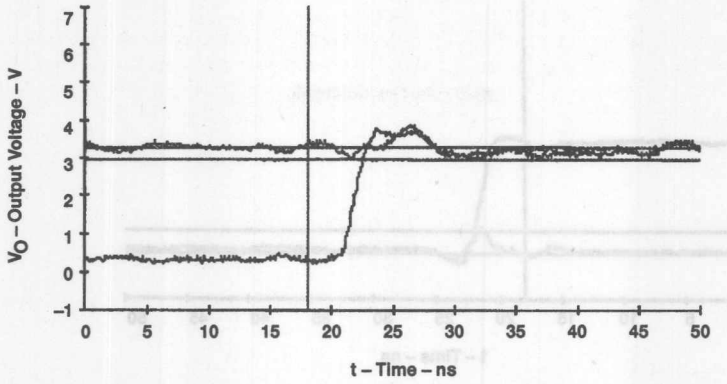
V_1 = 25 mV, V_2 = 14.7 mV, V_D = 12.2 mV

Figure A–1. SN74ACT3638 V_{OLP}, V_{CC} = 5.5 V



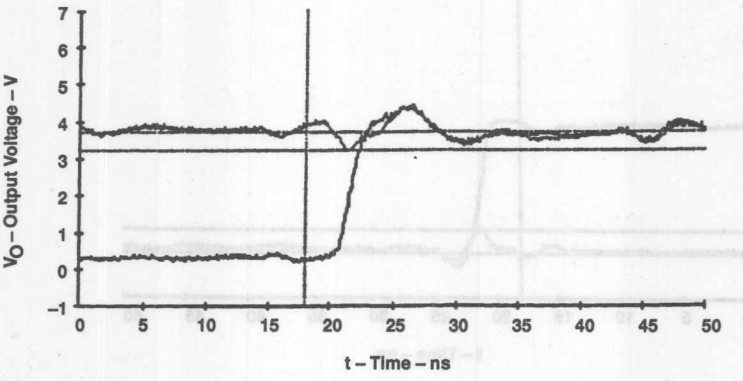
V_1 = 3.63 V, V_2 = 5.31 V, V_D = 1.69 V

Figure A–2. SN74ACT3638 V_{OHV}, V_{CC} = 5.5 V



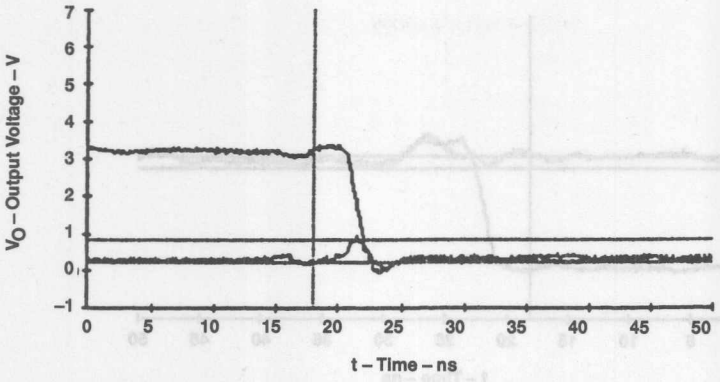
V_1 = 3.25 V, V_2 = 2.93 V, V_D = –312.5 mV

Figure A–3. SN74ABT3611 V_{OHV}, V_{CC} = 5 V



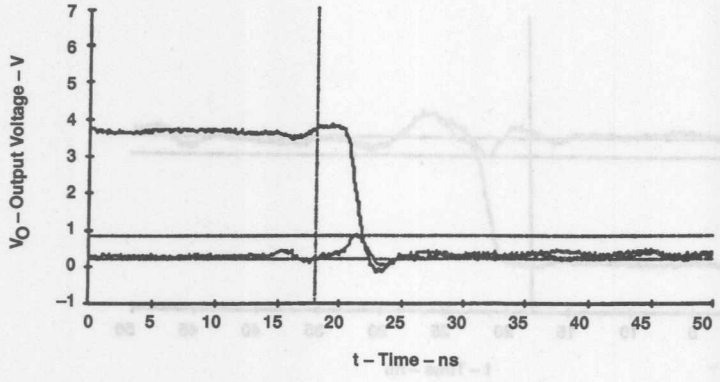
V_1 = 3.71 mV, V_2 = 3.21 mV, V_D = –500 mV

Figure A–4. SN74ABT3611 V_{OHV}, V_{CC} = 5.5 V



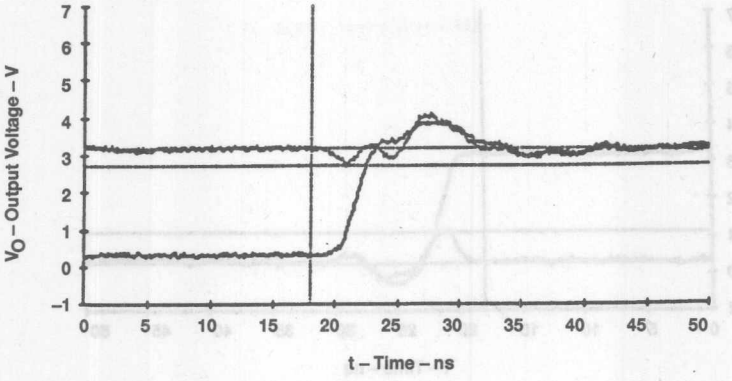
V_1 = 218.75 mV, V_2 = 843.75 mV, V_D = 625 mV

Figure A–5. SN74ABT3611 V_{OLP}, V_{CC} = 5 V



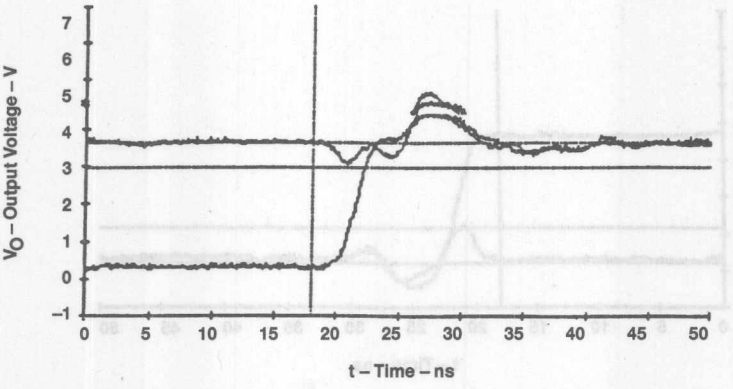
V_1 = 218.75 mV, V_2 = 843.75 mV, V_D = 625 mV

Figure A–6. SN74ABT3611 V_{OLP}, V_{CC} = 5 V



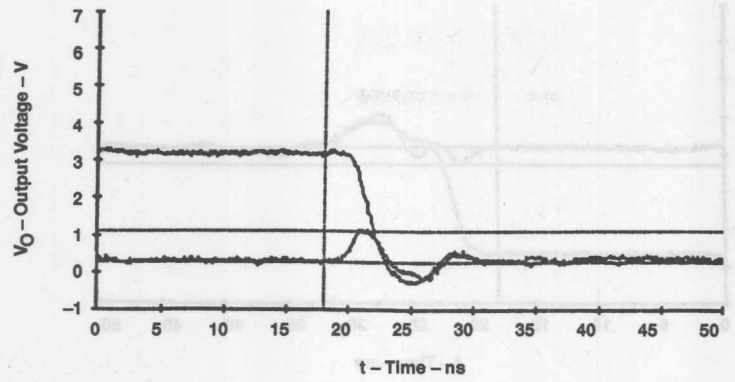
$V_1 = 3.18$ V, $V_2 = 2.71$ V, $V_D = -468.75$ mV

Figure A–7. SN74ABT3613 V_{OHV}, V_{CC} = 5 V



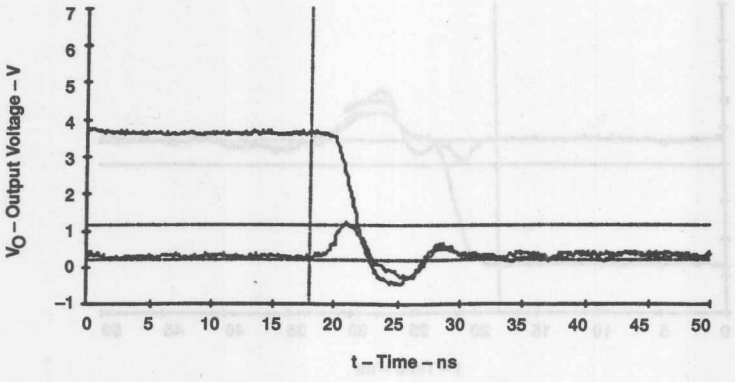
$V_1 = 3.18$ V, $V_2 = 2.71$ V, $V_D = -468.75$ mV

Figure A–8. SN74ABT3613 V_{OHV}, V_{CC} = 5.5 V



V_1 = 250 mV, V_2 = 1.12 V, V_D = 875 mV

Figure A–9. SN74ABT3613 V_{OLP}, V_{CC} = 5 V



V_1 = 218.75 mV, V_2 = 1.18 V, V_D = 968.75 mV

Figure A–10. SN74ABT3613 V_{OLP}, V_{CC} = 5.5 V

Appendix B

FIFO Package Types

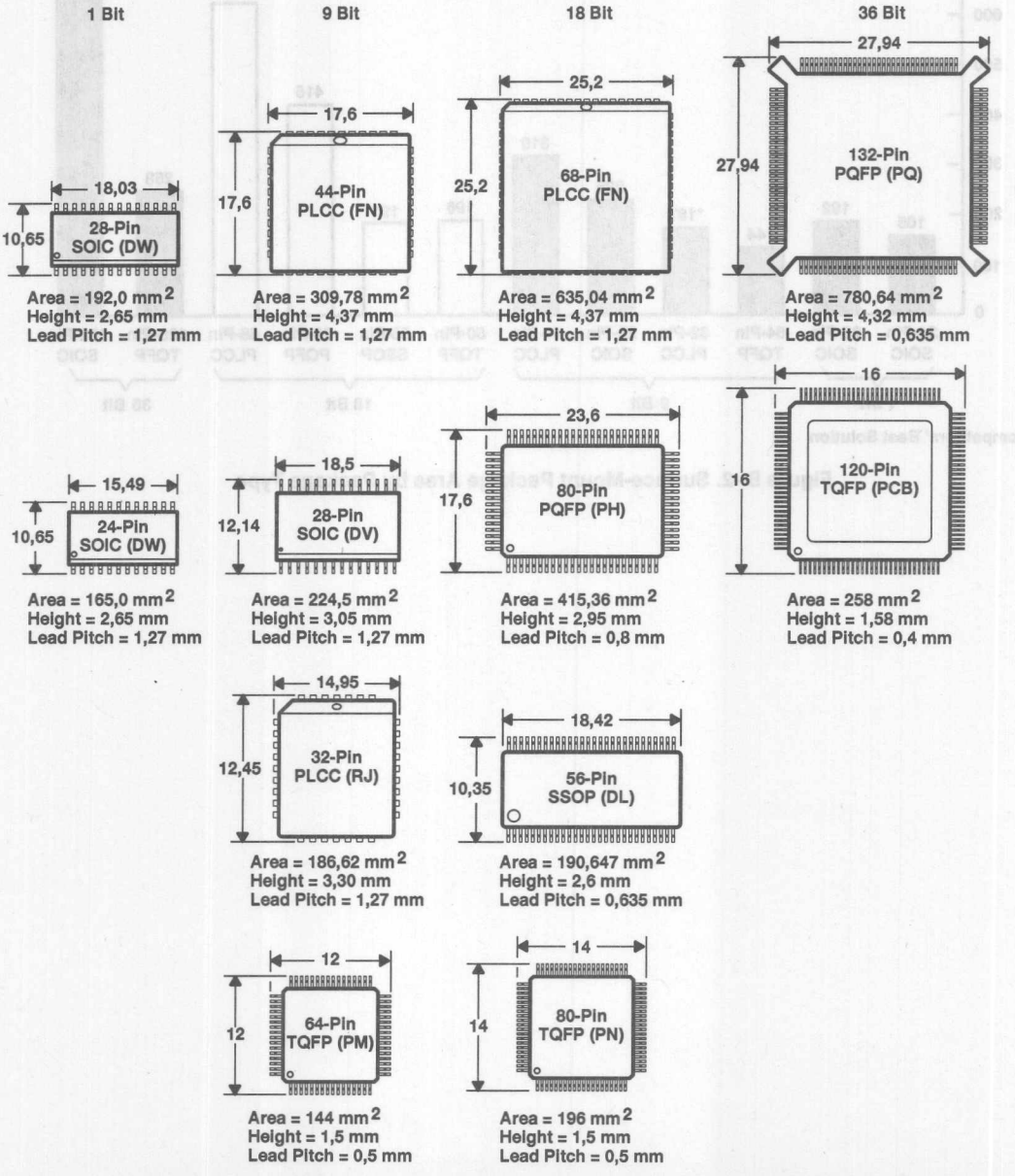


Figure B–1. Surface-Mount Package Options

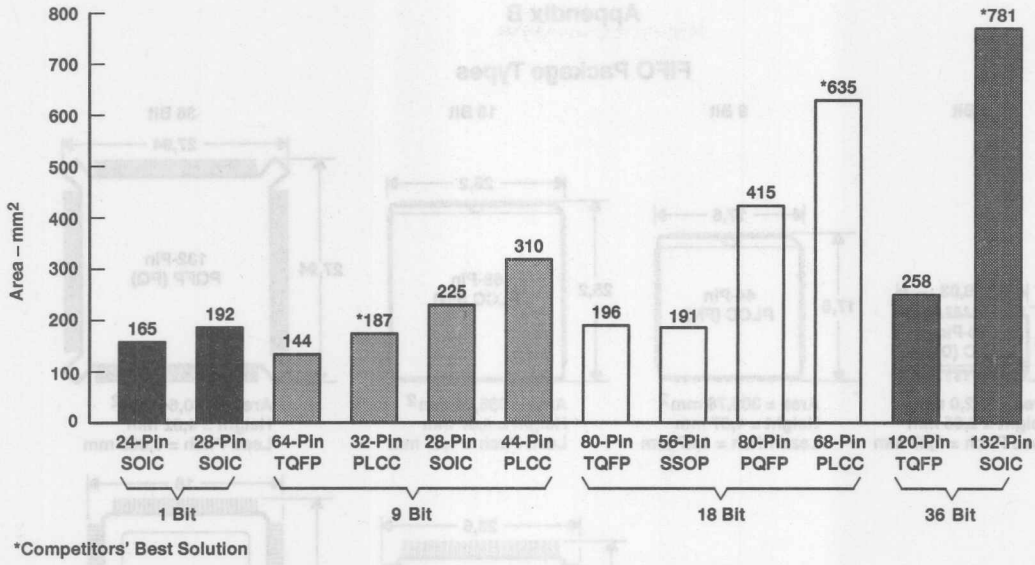


Figure B–2. Surface-Mount Package Area by Package Type

FIFO Solutions for Increasing Clock Rates and Data Widths

First-In, First-Out Technology

Kam Kittrell
Advanced System Logic – Semiconductor Group



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Introduction

Steady increases in microprocessor operating frequencies and bus widths over recent years have challenged system designers to find FIFO memories that meet their needs. To assist the designer, new FIFOs from Texas Instruments (TI) are available with features that complement these microprocessor trends.

Higher data-transfer rates have dictated the need for FIFOs to evolve into *clocked* architecture wherein data is moved in and out of the device with synchronous controls. Each synchronous control of the clocked FIFO uses enable signals that synchronize the data exchange to a *free-running* (continuous) clock.

Since the continuous clocks on each port of a clocked FIFO can operate asynchronously to each other, internal status signals indicating when the FIFO is empty or full can change with respect to either clock. To use a status signal for port control, it is synchronized to the port's clock on a clocked FIFO. Synchronization of these signals with flip-flops introduces metastability failures that increase with clock frequency. TI uses two-stage flag synchronization to greatly improve reliability.

Higher clock frequencies augment raw speed, but greater bandwidth is also achieved by increasing the data width. Wider datapaths can have the associated cost of large board area due to increased package sizes. New compact packages for TI's FIFOs reduce this cost.

Clocked FIFOs

Clocked FIFOs have become popular for relieving bottlenecks in high-speed data traffic. Data transfers for many systems are synchronized to a central clock with read and write enables. These free-running clocks can be input directly to a clocked FIFO with the same enables controlling its data transfer on the low-to-high transition of the clock.

Reducing the number of clocks keeps the interface simple and easy to manage. Extra logic is needed to produce a gated pulse when using a FIFO that accepts a clock only for a data transfer request. The generated clock signal is a derivative of the master clock with a margin of timing uncertainty. At high clock frequencies, this timing uncertainty is not tolerable and costly adjustments are needed.

Additional logic also is conserved by implementing flag synchronization on the clocked FIFO. Tracking is done to generate flags that indicate when the memory is empty or full. In many applications, the input and output to the FIFO are asynchronous and the flag signals must be synchronized for use as control. A read is not completed on the FIFO if no data is ready, so the $\overline{\text{EMPTY}}$ signal is synchronized to the read clock. This synchronous output-ready (OR) flag is useful for controlling read operations. Likewise, the $\overline{\text{FULL}}$ signal is synchronized to the write clock, producing the input-ready (IR) flag.

Flag Synchronization

As previously explained, one of the advantages of the clocked FIFO is the on-board synchronization of the $\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ status flags when the input and output are asynchronous. In one method of synchronization, a single flip-flop captures the asynchronous flag's value (see Figure 1). With this method, the rising transition of data can violate the flip-flop's setup time and produce a metastable event (metastability is a malfunction of a flip-flop wherein the latch hangs between high and low states for an indefinite period of time).

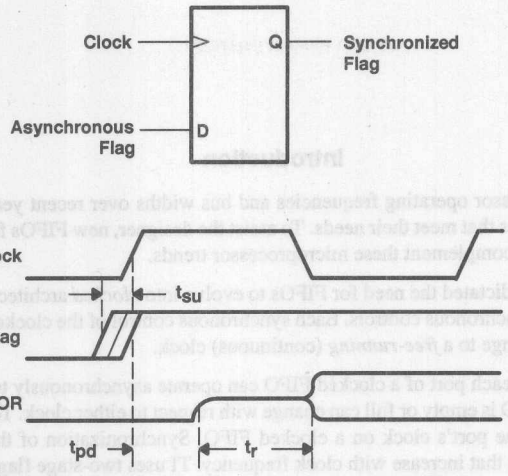


Figure 1. Triggering a Metastable Event With a One-Stage Synchronizer

Once a metastable event is triggered, the probability of the output recovering to a high or low level increases exponentially with increased resolve time (t_r). The expected time until the output of a single flip-flop with asynchronous data has a metastable event that lasts t_r or longer is characterized by the following mean time between failures (MTBF) equation:

$$MTBF_1 = \frac{\exp\left(\frac{t_r}{\tau}\right)}{t_o\ f_c\ f_d}$$

Where:

t_o = flip-flop constant representing the time window during which changing data invokes a failure
t_r = resolve time allowed in excess of the normal propagation delay
t = flip-flop constant related to the settling time of a metastable event
f_c = clock frequency
f_d = asynchronous data frequency. For OR-flag analysis, it is the frequency at which data is written to empty memory. For IR-flag analysis, it is the frequency at which data is read from full memory.

The MTBF decreases as clock and data frequency increase and as the time allowed for a metastable event to settle (t_r) decreases.

Metastability failures are a formidable issue for short-clock cycle times. Increasing the clock frequency linearly increases the number of metastable events triggered, but the shortened available resolve time exponentially increases the failure rate. It is impossible to eliminate the possibility of a metastable event under these conditions, but solutions exist to reliably increase the expected time between failures.

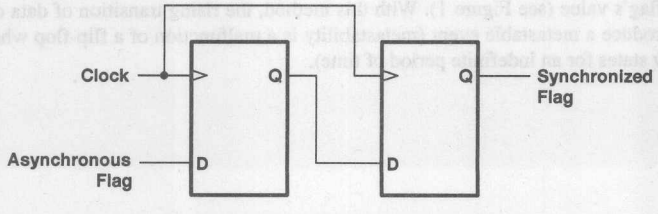


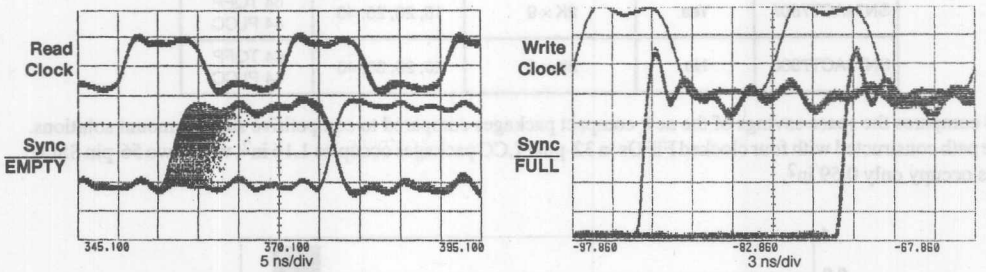
Figure 2. Two-Stage Synchronizer

TI increases the metastable MTBF by several orders of magnitude for IR and OR flags by employing two-stage synchronization (see Figure 2). For the output of the second stage to be metastable, the first stage must have a metastable event that lingers until it encroaches upon the setup time of the second stage. Adding another stage to a single flip-flop synchronizer is statistically equivalent to increasing its resolve time by the clock period minus its propagation delay. The mean time between failures for a two-stage synchronizer is given by:

$$MTBF_2 = \frac{\exp\left[\frac{t_r + \frac{1}{f_c} - t_p}{\tau}\right]}{t_o\, f_c\, f_d}$$

Where:

t_p = propagation delay of the first flip-flop



f_c = 50 MHz, f_d = 5 MHZ, V_{CC} = 5 V

(a) ONE-STAGE SYNCHRONIZATION

f_c = 66.7 MHz, f_d = 6.7 MHz, V_{CC} = 5 V

(b) TWO-STAGE SYNCHRONIZATION

Figure 3. Storage Oscilloscope Plots Taken Over a 15-Hour Duration

Figure 3 compares the two synchronization methods previously discussed. Both plots were taken at room temperature and nominal V_{CC} while each data transition violated setup time. Figure 3(a) shows the performance of an $\overline{\text{EMPTY}}$ flag synchronizer using only one flip-flop, while Figure 3(b) is the IR flag of an SN74ACT7807 with the write clock operating at maximum frequency.

Compact Packaging

Microprocessor bus widths have continuously doubled every few years to maximize their performance. Bus widths of 32 and 64 bits are commonplace today, whereas they were almost unheard of a few years ago. The downside to the increased bit count is that each subordinate device in the system must match this width with corresponding increases in board size.

New shrink packages for TI's clocked FIFOs provide a solution to this problem. Multiple-byte datapaths can be buffered while covering only a fraction of the area of conventional packages. These new FIFO packages are presently available in 56-, 64-, and 80-pin configurations. Dubbed shrink quad flat package (SQFP), the 64-pin package is used for 9-bit-wide FIFOs, and the 80-pin package is used for 18-bit-wide FIFOs. Both SQFP packages have a lead pitch of 0.5 mm. The 56-pin shrink small-outline package has a 0.025-inch lead pitch and also houses 18-bit-wide FIFOs. A variety of TI's FIFOs are offered in these new packages (see Table 1).

Table 1. FIFOs Available in Space-Efficient Packages

DEVICE	CLOCKED	ORGANIZATION	CLOCK CYCLE TIME (ns)	PACKAGES
SN74ACT2235	No	1K × 9 × 2	20, 30 40, 50	64 TQFP 44 PLCC
SN74ACT7802	No	1K × 18	25, 40, 60	80 TQFP 68 PLCC
SN74ACT7811	Yes	1K × 18	15, 18, 20, 25	80 TQFP 68 PLCC
SN74ACT7803 SN74ACT7805 SN74ACT7813	Yes	512 × 18 256 × 18 64 × 18	15, 20, 25, 40	56 SSOP
SN74ACT7804 SN74ACT7806 SN74ACT7814	No	512 × 18 256 × 18 64 × 18	20, 25, 40	56 SSOP
SN74ACT7807	Yes	2K × 9	15, 20, 25, 40	64 TQFP 44 PLCC
SN74ACT7808	No	2K × 9	20, 25, 30, 40	64 TQFP 44 PLCC

Figure 4 compares the space savings of the new compact packages compared to competitive surface-mount solutions. A 4-byte path constructed with four clocked FIFOs in 32-pin PLCC packages occupies 1.16 in^2, while two 56-pin SSOP packages occupy only 0.59 in^2.

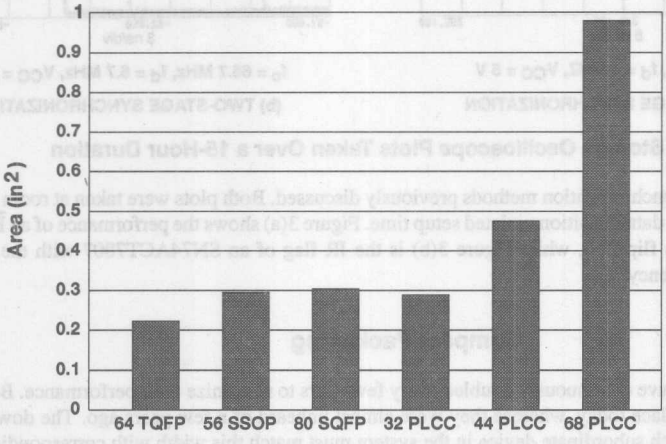


Figure 4. Surface-Mount Package Area Comparison

New Clocked FIFOs

Four new CMOS clocked FIFOs from TI offer a variety of memory depths. All four can match applications that require maximum clock frequencies of 67 MHz and access times of 12 ns. Suited for buffering long packets, the 2K × 9 SN74ACT7807 is the deepest of the four and is available in the 44-pin PLCC or 64-pin TQFP. The SN74ACT7803, SN74ACT7805, and SN74ACT7813 are organized as 512 × 18, 256 × 18, and 64 × 18, respectively, and have the same pin arrangement in the 56-pin SSOP. Every TI clocked FIFO is easily expanded in word width, and the SN74ACT7803/05/13 can also be arranged to form a bidirectional FIFO. With the two FIFOs connected as in Figure 5, no extra logic is needed for bidirectional operation.

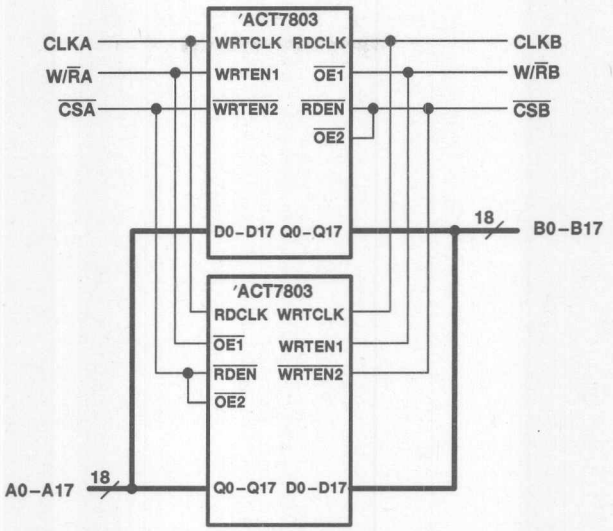


Figure 5. Bidirectional Configuration for the SN74ACT7803

Silicon is currently available for a bidirectional clocked FIFO fabricated in TI's Advanced BiCMOS (ABT) process. The SN74ABT7819 is organized as 512 × 18 × 2 with two internal independent FIFOs. Each port has a continuous free-running clock, a chip select ($\overline{CS}$), a read/write select ($\overline{R}/W$), and two separate read and write enables for control. It supports clock frequencies in excess of 80 MHz and a maximum access time below 10 ns. This device is packaged in the 80-pin QFP and 80-pin SQFP.

Conclusion

Several semiconductor manufacturers, including TI, have responded to customer needs by providing clocked FIFOs whose synchronous interfaces conform to the requirements of many high-performance systems. Capitalizing on the available continuous system clocks, this architecture limits the amount of necessary glue logic and the number of timing constraints.

Flag synchronization is important for clocked FIFOs buffering between asynchronous systems. Flip-flop synchronizers used for this task have a metastable failure rate that grows exponentially with clock frequency. TI employs two stages of synchronization that improve the flags' reliability significantly.

Finally, providing a FIFO buffer for wide buses has historically consumed large amounts of board area. Designers seeking relief from this problem can find it in the packaging options offered for TI's FIFOs. Used to house 9- and 18-bit devices, these packages require only about 50% of the space required for conventional surface-mount packages.

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FIFO Features

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FIFO Patented Synchronous Retransmit: Programmable DSP-Interface Application for FIR Filtering

Steve Strom and Kam Kittrell
Advanced System Logic – Semiconductor Group



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Introduction

This application report presents one example of the many uses of the synchronous-retransmit feature of Texas Instruments (TI) digital signal processing (DSP) application-specific FIFOs. This report describes TI's patented synchronous-retransmit feature and shows how this feature can be used in conjunction with a DSP for finite-length impulse-response (FIR) filtering. The TMS320C31 floating-point DSP and the SN74ACT3638 bidirectional clocked FIFO are the examples for this discussion.

Description of Synchronous Retransmit

An SN74ACT3638 functional block diagram with the synchronous-retransmit logic block highlighted is shown in Figure 1. The synchronous-retransmit feature of the SN74ACT3638 allows data stored within the FIFO to be reread starting at a selected position. FIFO1, one of two 512 × 32 dual-port SRAM FIFOs on board the SN74ACT3638 device, buffers data from port A to port B. FIFO1 is placed in the retransmit mode to select a beginning word and to prevent ongoing FIFO write operations from destroying data to be retransmitted. Data vectors with a minimum length of three words can be retransmitted repeatedly starting at the selected word. The FIFO can be taken out of the retransmit mode at any time, allowing normal operation to resume.

Figure 2 shows the FIFO1 retransmit timing and minimum retransmit length. FIFO1 is placed in the retransmit mode by a low-to-high transition on CLKB when the retransmit mode (RTM) input is high and the port-B output-ready (ORB) flag is high. This rising clock edge marks the data present in the FIFO1 output register as the first retransmit word. FIFO1 remains in the retransmit mode until a low-to-high transition of CLKB occurs while RTM is low.

When two or more reads have been performed past the initial retransmit word, a retransmit is initiated by a low-to-high transition on CLKB when the read-from-mark (RFM) input is high. This rising CLKB edge shifts the first retransmit word to the FIFO1 output register and subsequent reads begin immediately. While FIFO1 is in the retransmit mode, retransmit loops can be performed repeatedly with each pulse of the RFM terminal.

When FIFO1 is in the retransmit mode, it operates with two read pointers. The current-read pointer operates normally, incrementing each time a new word is shifted to the FIFO1 output register. This pointer is used as a reference by the ORB and port-B almost-empty ($\overline{\text{AEB}}$) flags. The shadow-read pointer stores the SRAM location at the time FIFO1 is placed in the retransmit mode and does not change until FIFO1 is taken out of the retransmit mode. This pointer is used as a reference by the port-A input-ready (IRA) and almost-full ($\overline{\text{AFA}}$) flags. While the FIFO is in the retransmit mode, data writes to the FIFO may continue. $\overline{\text{AFA}}$ is set low by the write that stores (512 – Y1) words after the first retransmit word, where 512 is the FIFO depth and Y1 is the almost-full-flag offset value. The IRA flag is set low following 512 writes after the first retransmit word.

When FIFO1 is in retransmit mode and RFM is high, a rising CLKB edge loads the current pointer with the shadow-read-pointer value. The ORB flag immediately reflects the new level of fill. If the retransmit changes the status of FIFO1 such that it is no longer within the almost-empty range, up to two CLKB rising edges after the retransmit cycle are required before the AEB flag is asserted. The rising CLKB edge that takes FIFO1 out of the retransmit mode shifts the read pointer used by the IRA and $\overline{\text{AFA}}$ flags from the shadow-read pointer to the current-read pointer.

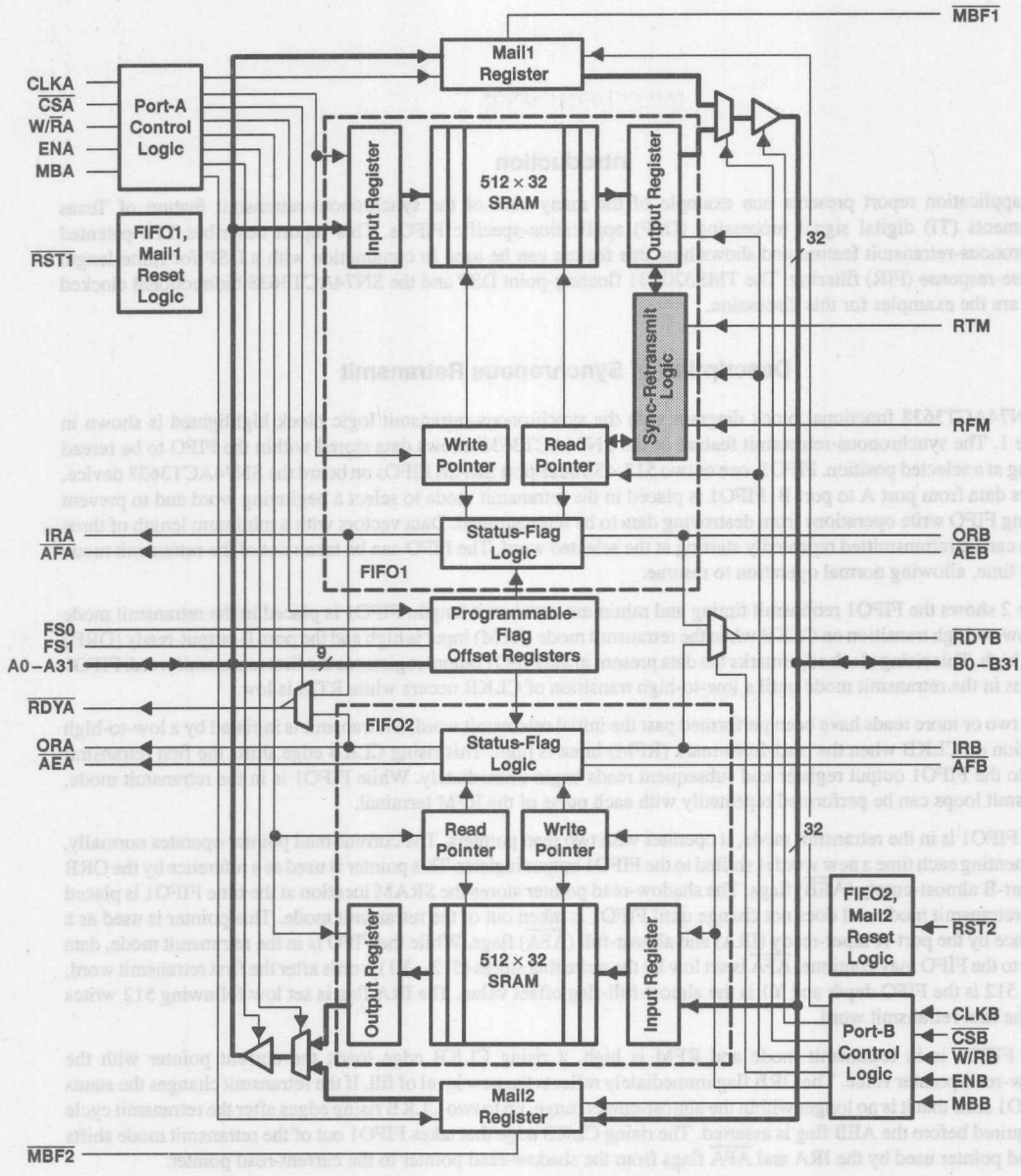
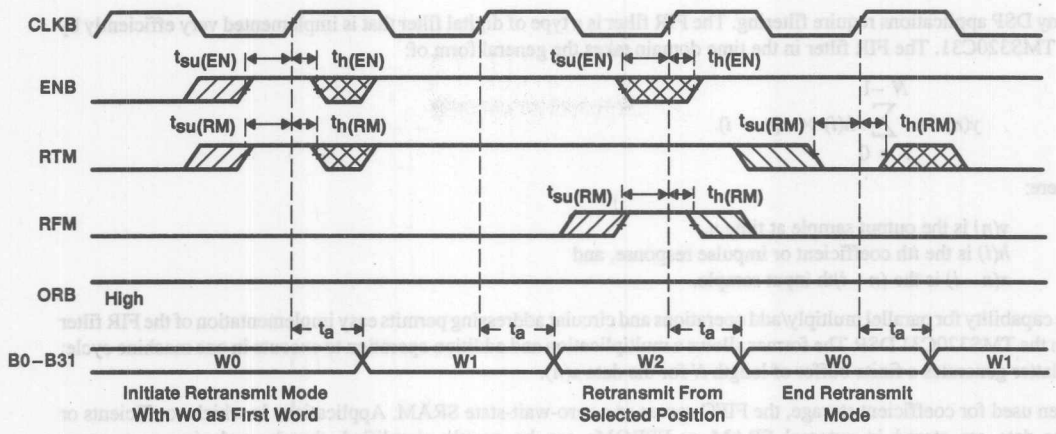


Figure 1. SN74ACT3638 Functional Block Diagram



$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, MBB, RTM, and RFM after CLKB↑
$t_{su(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, MBB, RTM, and RFM after CLKB↑
t_a	Access time, CLKA↑ to A0 – A31 and CLKB↑ to B0 – B31

Figure 2. FIFO1 Retransmit Timing Diagram Showing Minimum Retransmit Length

Example of Retransmit for FIR Filtering

In addition to the typical interface functions, such as rate matching and clock partitioning, FIFOs with retransmit capabilities can provide a repeated sequence of data to a processing element such as a DSP. This sequence of information may take the form of coefficients for use in a DSP multiply/accumulate operations as shown in Figure 3.

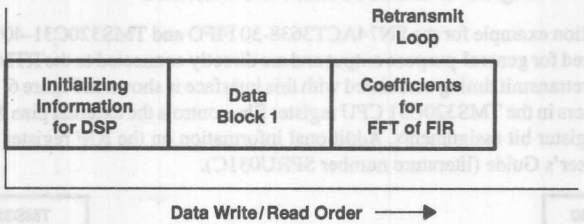


Figure 3. Using a FIFO for Coefficient Storage in Multiply/Accumulate Operations

Many DSP applications require filtering. The FIR filter is a type of digital filter that is implemented very efficiently by the TMS320C31. The FIR filter in the time domain takes the general form of:

$$y(n) = \sum_{i=0}^{N-1} h(i) \times x(n-i)$$

Where:

$y(n)$ is the output sample at time n,
$h(i)$ is the ith coefficient or impulse response, and
$x(n-i)$ is the $(n-i)$th input sample.

The capability for parallel multiply/add operations and circular addressing permits easy implementation of the FIR filter with the TMS320C31 DSP. The former allows a multiplication and addition operation to execute in one machine cycle; the latter generates a finite buffer of length N for the data $x(n)$.

When used for coefficient storage, the FIFO serves as a zero-wait-state SRAM. Applications in which coefficients or other data are stored in external SRAM or EPROMs can be greatly simplified, thereby reducing cost, space requirements, and overall device count. In other instances where DSP internal RAM is used to store the coefficients, a penalty is often paid in the form of overhead time for transferring the coefficients from the buffering FIFO to RAM. This overhead penalty and inefficient use of RAM can be eliminated by the use of the patented synchronous-retransmit feature of the TI FIFO.

Two TMS320C31 external input/output (I/O) flags (XF0 and XF1) can be configured as input or output terminals under software control. In the example of FIR filtering, I/O flags can be implemented to control the retransmit function of the FIFO, providing a programmable DSP interface. Figure 4 shows a block-diagram representation of the bidirectional interface to the programmable DSP.

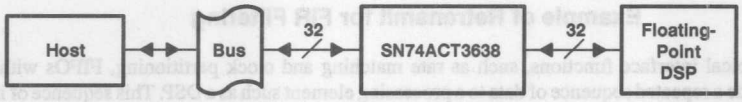


Figure 4. Bidirectional FIFO Interface

Figure 5 shows an interconnection example for the SN74ACT3638-30 FIFO and TMS320C31-40 DSP. The DSP XFO and XF1 terminals are configured for general-purpose output and are directly connected to the RTM and RFM terminals of the FIFO, respectively. The retransmit timing associated with this interface is shown in Figure 6. The I/O flag register (IOF), which is one of 28 registers in the TMS320C31 CPU register file, controls the external pins XF0 and XF1. Figure 7 shows a summary of IOF register bit assignments. Additional information on the IOF register may be obtained by consulting the TMS320C3x User's Guide (literature number SPRU031C).

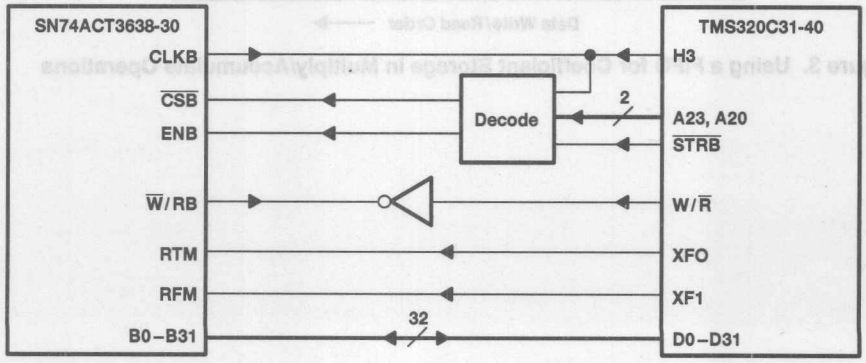


Figure 5. Interconnection Example

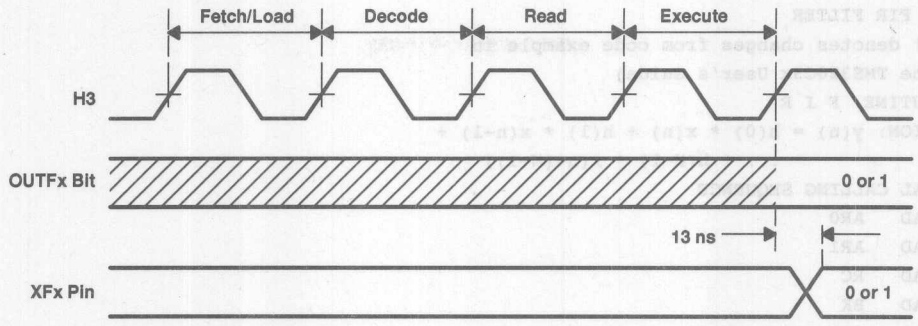


Figure 6. Retransmit Timing for Interconnection Example

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
xx	xx	xx	xx	xx	xx	xx	xx	INXF1	OUTXF1	T/OXF1	xx	INXF0	OUTXF0	T/OXF0	xx
								R	R/W	R/W		R	R/W	R/W	

NOTES: A. xx = reserved bit, read as 0
B. R = read, W = write

BIT	NAME	RESET VALUE	FUNCTION
0	Reserved	0	Read as 0
1	$\overline{I}$/OXF0	0	If $\overline{I}$/OXF0 = 0, XF0 is configured as a general-purpose input terminal. If $\overline{I}$/OXF0 = 1, XF0 is configured as a general-purpose output terminal.
2	OUTXF0	0	Data output on XF0
3	INXF0	0	Data input on XF0. A write has no effect.
4	Reserved	0	Read as 0
5	$\overline{I}$/OXF1	0	If $\overline{I}$/OXF1 = 0, XF1 is configured as a general-purpose input terminal. If $\overline{I}$/OXF1 = 1, XF1 is configured as a general-purpose output terminal.
6	OUTXF1	0	Data output on XF1
7	INXF1	0	Data input on XF1. A write has no effect.
31–8	Reserved	0–0	Read as 0

Figure 7. IOF Register Bit Summary

Modified Code for TMS320C3x FIR Filtering

The FIFO retransmit control for FIR filtering can be structured as in the following modified code fragment from the TMS320C3x User's Guide (see Figure 8). The values loaded into the IOF register are chosen to set and reset the RTM and RFM terminals of the FIFO as appropriate, providing retransmit control. Figure 9 shows the control timing associated with the FIFO retransmit for the FIR filter.

```
*    TITLE FIR FILTER
*       (!! denotes changes from code example in
*        the TMS320C3x User's Guide)
*    SUBROUTINE  F I R
*    EQUATION: y(n) = h(0) * x(n) + h(1) * x(n-1) +
*                     ... + h(N-1) * x(n-(N-1))
*    TYPICAL CALLING SEQUENCE
*       LOAD   AR0
*       LOAD   AR1
*       LOAD   RC
*       LOAD   BK
* !!    LOAD   IOF
*       CALL   FIR
*    ARGUMENT ASSIGNMENTS:
*     ARGUMENT| FUNCTION
*     --------+-------------------------------------------------
* !!  AR0     | ADDRESS OF FIFO where h vector is stored starting with
*             |   h(N-1)
*     AR1     | ADDRESS OF x(n-(N-1))
*     RC      | LENGTH OF FILTER - 2 (N-2)
*     BK      | LENGTH OF FILTER (N)
* !!  IOF     | XF0, XF1 configured as outputs.  XF0 is high, XF1 is low.
*             |   Initial register content is 026h. FIFO in retransmit mode.
* !! REGISTERS USED AS INPUT: AR1, RC, BK, IOF
* !! REGISTERS MODIFIED: R0, R2, AR0, AR1, RC, IOF
*    REGISTER CONTAINING RESULT: R0
       .global FIR
*                                      ; Initialize R0
FIR    MPYF3   *AR0,*AR1++(1)%,R0      ; !! AR0 not incremented
*                                      ; h(N-1) * x(n-(N-1)) -> R0
       LDF     0.0,R2                  ; Initialize R2
*    FILTER (1 <= i < N)
       RPTS    RC                      ; Setup the repeat cycle
*                                      ; !! AR0 not incremented
       MPYF3   *AR0,*AR1++(1)%,R0      ; h(N-1-i)*x(n-(N-1-i))->R0
||     ADDF3   R0,R2,R2                ; Multiply and add operation
*
       ADDF    R0,R2,R0                ; Add last product
*  !!
       LDI     066h,IOF                ; Retransmit FIFO data starting
*                                        with h(N-1) by asserting RFM
*                                        (XF1) high
*  !!
       LDI     026h,IOF               ; End RFM (XF1) high pulse to
*                                        begin normal data reads
*   RETURN SEQUENCE
       RETS                           ; Return
*  end
       .end
```

Figure 8. FIFO Retransmit Control for FIR Filtering

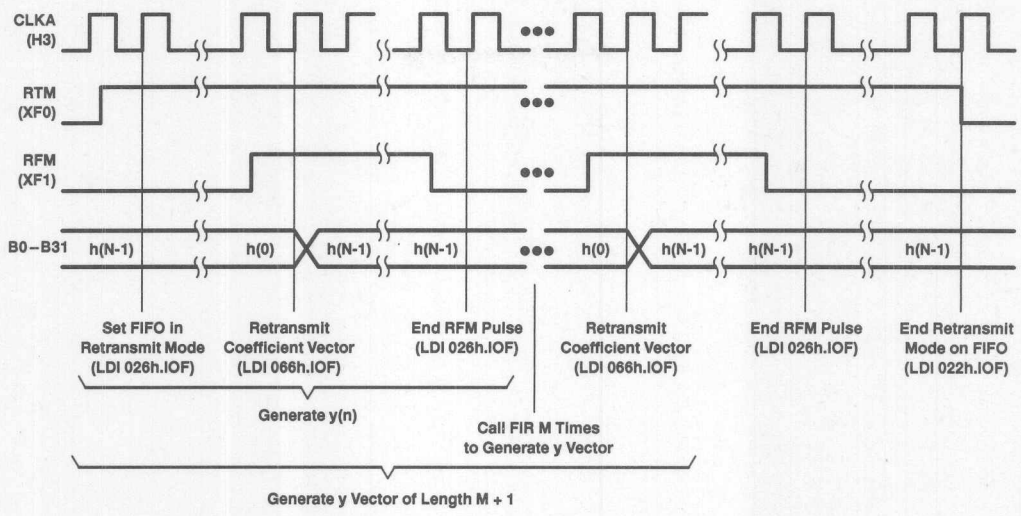


Figure 9. Control Timing for FIFO Retransmit for the FIR Filter

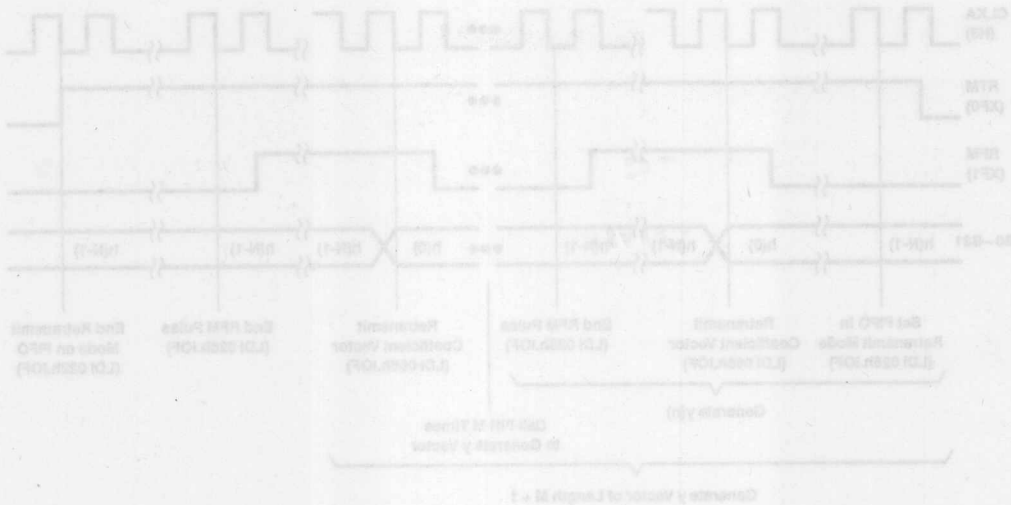
Conclusion

Unlike conventional retransmit, TI's patented synchronous-retransmit feature allows the user to select or mark the FIFO data to be retransmitted. Synchronous retransmit is easily controlled by two FIFO terminals: RTM and RFM. As previously discussed in this application report, synchronous retransmit provides a very efficient method for transferring a series of FIR filter coefficients to a DSP without storing the coefficients in a standard SRAM or EPROM. By interfacing the DSP external I/O terminals to the FIFO retransmit terminals, the DSP can effectively request the FIR filter coefficients on demand.

The following FIFOs belong to the DSP application-specific family featuring synchronous retransmit.

Table 1. DSP Application-Specific Family

DEVICE	ORGANIZATION	SPEED SORTS t_c (ns)	MAXIMUM FREQUENCY (MHz)	MAXIMUM ACCESS (ns)
SN74ACT3638	512 x 32 x 2	–15, –20, –30	67	11
SN74ACT3631	512 x 36	–15, –20, –30	67	11
SN74ACT3641	1K x 36	–15, –20, –30	67	11
SN74ACT3651	2K x 36	–15, –20, –30	67	11



FIFO Mailbox-Bypass Registers: Using Bypass Registers to Initialize DMA Control

Kam Kittrell and Steve Strom
Advanced System Logic – Semiconductor Group



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Introduction

This application report describes the operation of FIFO mailbox-bypass registers and shows their application in an example that implements the direct memory access (DMA) control of a digital signal processor (DSP). All Texas Instruments (TI) 32- and 36-bit FIFOs contain mailbox-bypass registers that transmit priority data from one FIFO port to the other, either from port A to port B or port B to port A, without storing the data in the FIFO SRAM buffer. The SN74ACT3641, a unidirectional, clocked-DSP, application-specific FIFO (1K x 36), is used as the example for our discussion. In the following scenario, this device connects to a DMA controller that may be viewed as an integral part of any generic processing element. This discussion focuses on the DMA controller that is resident on board the TMS320C31 DSP.

Mailbox-Bypass Register Operation

The operation of the FIFO mailbox-bypass register is straightforward. Each FIFO that features the mailbox option has two 32- or 36-bit bypass registers (Mail1 and Mail2) to pass command and control information between both ports without queuing the information in the FIFO SRAM buffer. The functional block diagram of the SN74ACT3641 is shown in Figure 1. The associated timing of the Mail1 register in the FIFO functional block diagram is shown in Figure 2.

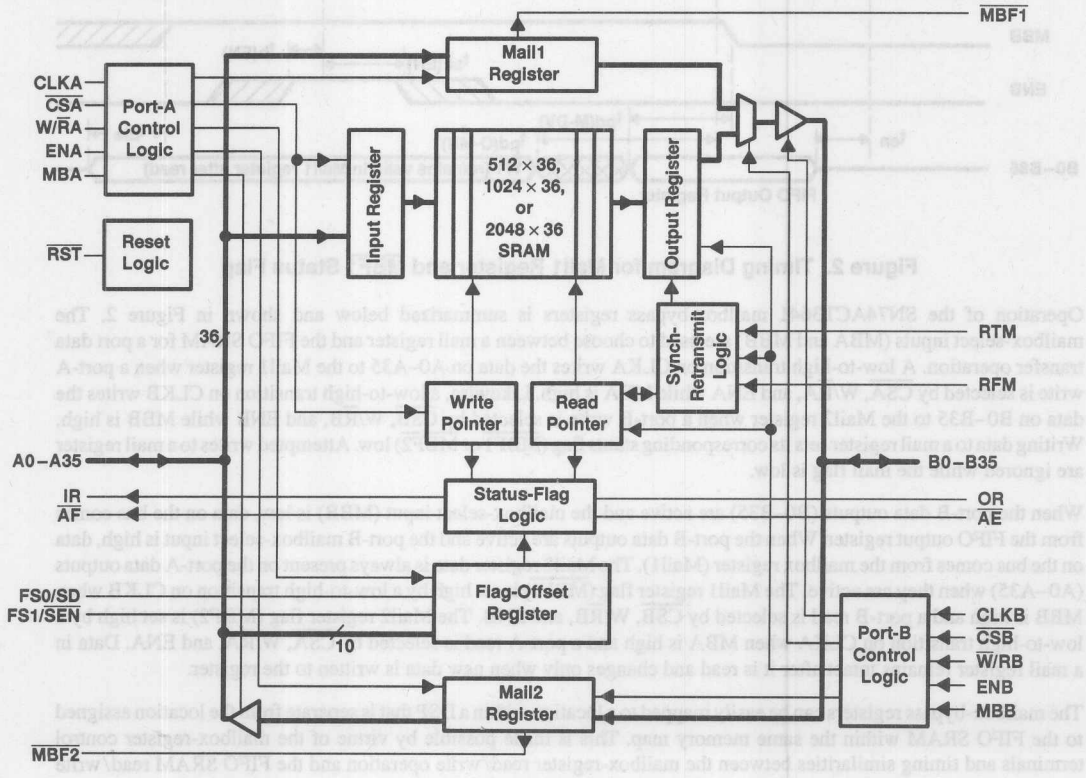


Figure 1. SN74ACT3641 FIFO Functional Block Diagram

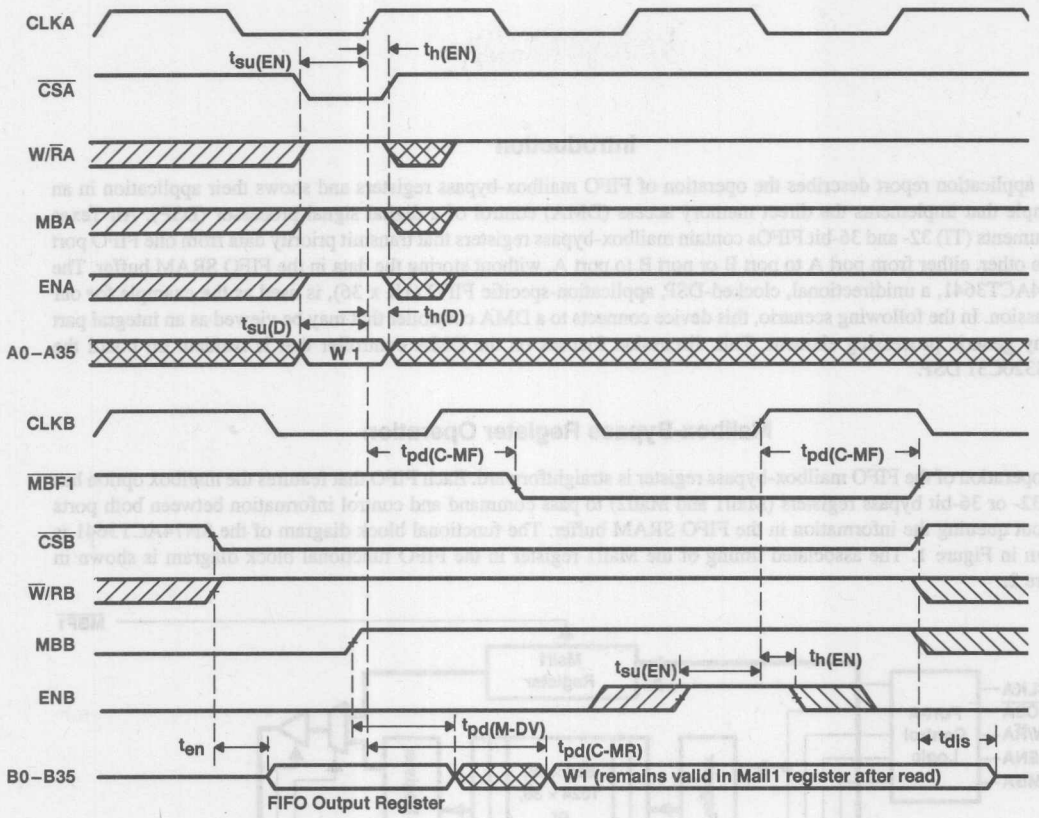


Figure 2. Timing Diagram for Mail1 Register and $\overline{\text{MBF1}}$ Status Flag

Operation of the SN74ACT3641 mailbox-bypass registers is summarized below and shown in Figure 2. The mailbox-select inputs (MBA and MBB) are used to choose between a mail register and the FIFO SRAM for a port data transfer operation. A low-to-high transition on CLKA writes the data on A0–A35 to the Mail1 register when a port-A write is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA while MBA is high. Likewise, a low-to-high transition on CLKB writes the data on B0–B35 to the Mail2 register when a port-B write is selected by $\overline{\text{CSB}}$, W/$\overline{\text{RB}}$, and ENB while MBB is high. Writing data to a mail register sets its corresponding status flag ($\overline{\text{MBF1}}$ or $\overline{\text{MBF2}}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When the port-B data outputs (B0–B35) are active and the mailbox-select input (MBB) is low, data on the bus comes from the FIFO output register. When the port-B data outputs are active and the port-B mailbox-select input is high, data on the bus comes from the mailbox register (Mail1). The Mail2 register data is always present on the port-A data outputs (A0–A35) when they are active. The Mail1 register flag ($\overline{\text{MBF1}}$) is set high by a low-to-high transition on CLKB when MBB is high and a port-B read is selected by $\overline{\text{CSB}}$, W/$\overline{\text{RB}}$, and ENB. The Mail2 register flag (MBF2) is set high by a low-to-high transition on CLKA when MBA is high and a port-A read is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA. Data in a mail register remains intact after it is read and changes only when new data is written to the register.

The mailbox-bypass registers can be easily mapped to a location within a DSP that is separate from the location assigned to the FIFO SRAM within the same memory map. This is made possible by virtue of the mailbox-register control terminals and timing similarities between the mailbox-register read/write operation and the FIFO SRAM read/write operation. An example of assigning the mailbox register and FIFO to the memory map of the TMS320C31 is shown in Figure 3.

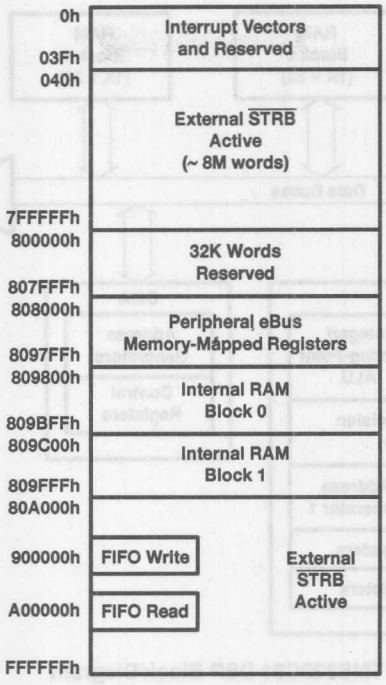


Figure 3. TMS320C31 Memory Map in Microprocessor Mode Showing Mailbox-Bypass Register and FIFO SRAM Addresses

DMA Controller Description

The TMS320C31 DSP contains an on-board direct-memory-access (DMA) controller that minimizes the requirement for the CPU to perform input/output operations. The TMS320C31 DSP block diagram is shown in Figure 4. Because of the DMA controller, the TMS320C31 can operate with slow external memories, peripherals, or analog-to-digital converters, for example, without slowing the computational throughput of the CPU.

Address and data buses are specifically dedicated to the DMA. As a result, there exists minimal conflict between the CPU and DMA controller. Using its address generators, source and destination registers, and transfer counter, the DMA controller can react to interrupts much like the CPU. Performing data transfers based upon interrupts received enables the DMA to execute input/output transfers that are typically the task of the CPU. While the DMA is receiving and transmitting data, the CPU is permitted to continue processing data.

A DMA transfer consists of two operations: reading from a memory location and writing to a memory location. These read and write operations can be as a block or a single word. The DMA controller can read from and write to any location in the TMS320C31 memory map, including all memory-mapped peripherals.

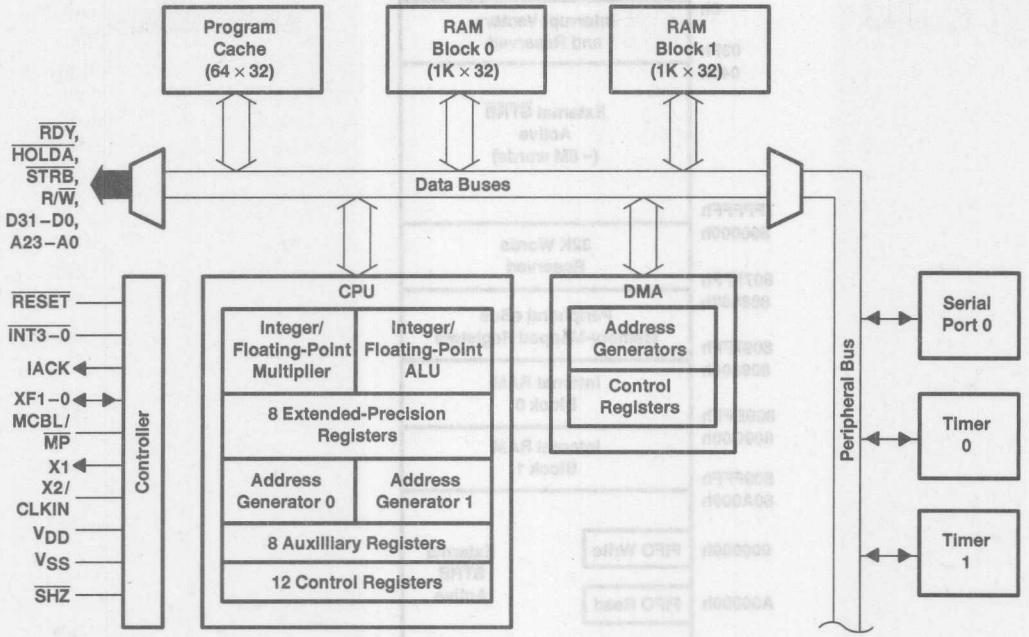


Figure 4. TMS320C31 DSP Block Diagram

Initializing DMA Controllers With Mailbox-Bypass Registers

FIFO memories, such as the SN74ACT3641, typically channel data between a generic local or backplane bus and a TMS320C31 DSP. The FIFO collects incoming information from the bus and develops packets or vectors of data for transfer to the DSP via the DMA controller (see Figure 5). The packet size of the stored data is easily defined by using the FIFO programmable almost-empty or almost-full flags and, if necessary, its empty and full flags. Data transfers via the DMA controller are performed block by block from the FIFO to the DSP or to off-chip memory such as RAM. The DMA-controlled transfer is preferred for moving large blocks of data. Instead of using the DSP's CPU for each single-word transfer, investing in a small amount of setup overhead allows the DMA to initialize the transfer of several words. In this case, the DMA controller becomes the bus master and performs the block transfer while the CPU is not using the external bus. The CPU is free to accomplish its primary task of performing mathematical operations.

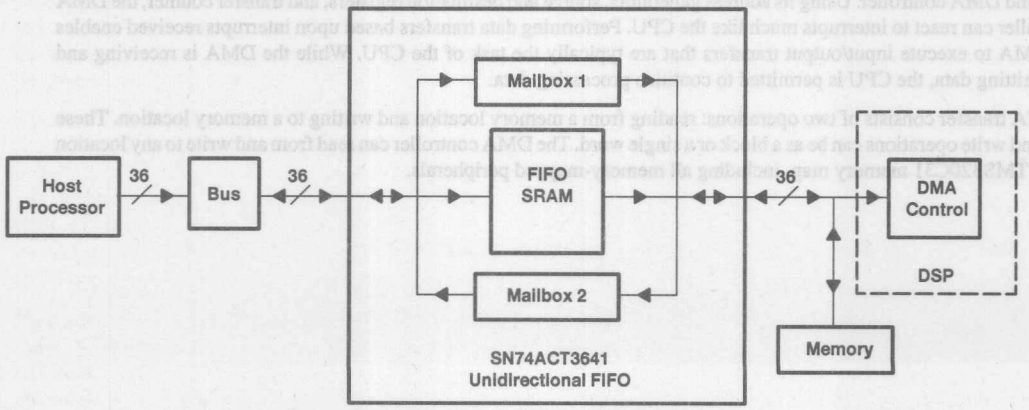
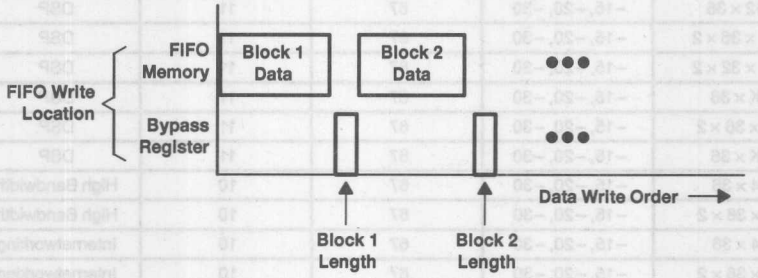


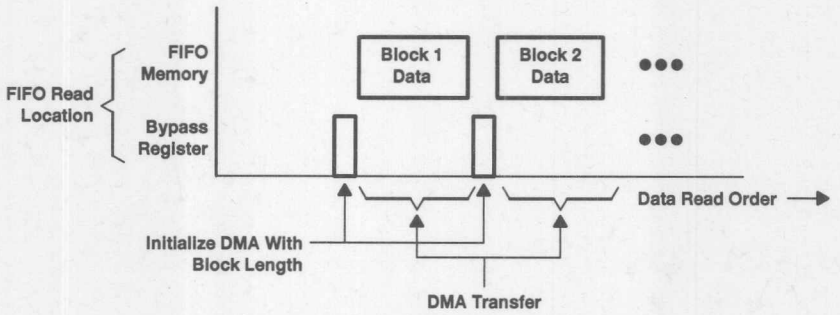
Figure 5. Using DMA Control to Transfer Large Data Blocks

Generally, the DMA controller requires the following information for data-block transfers: location of the data, destination of the data, and size of the data block to be transferred. The DMA controller is initialized by using the FIFO mailbox-bypass registers. This concept is shown in Figure 6. As previously, mailbox-bypass registers are useful in separating a control word from the data in a FIFO queue. In the example shown in Figure 6, the bypass registers of the SN74ACT3641 FIFO provide the DMA controller with the block-length initialization before performing the block transfer. At the same time, the mailbox-register status flags alert the DMA controller that the FIFO data is ready for transfer. In other instances, the mailbox register can also store a destination address in the DSP memory for incoming data.

In the earlier discussion, data flow through the mailbox register has been assumed to be in the bus-to-DSP direction. However, because of the bidirectional nature of the mailbox feature, the Mail2 register (see Figure 5) can also be used for transferring data in the DSP-to-bus direction. Many bus architectures support burst writes or have virtual addresses that can use the mailbox-bypass register for initialization.



(a) BUS-TO-FIFO DATA FLOW



(b) FIFO-TO-BUS DATA FLOW

Figure 6. Using Mailbox-Bypass Registers to Initialize DMA Control

Conclusion

Mailbox-bypass registers are very useful in performing block-data transfers from a bus to a processing element or vice versa. Integrating the 32- or 36-bit mailbox registers on board the FIFO chip significantly reduces the device count per system. Likewise, implementing on-board mailbox registers with access timing similar to the FIFO SRAM also reduces the requirement for control logic.

TI's DSP application-specific FIFOs, in addition to the other application-specific FIFOs with mailbox-bypass registers, are summarized in Table 1.

Table 1. FIFOs Featuring Mailbox-Bypass Registers

DEVICE	ORGANIZATION	SPEED SORTS	MAX FREQ	MAX ACCESS	APPLICATION
SN74ACT3622	256 × 36 × 2	−15, −20, −30	67	11	DSP
SN74ACT3621	512 × 36	−15, −20, −30	67	11	DSP
SN74ACT3632	512 × 36 × 2	−15, −20, −30	67	11	DSP
SN74ACT3638	512 × 32 × 2	−15, −20, −30	67	11	DSP
SN74ACT3641	1K × 36	−15, −20, −30	67	11	DSP
SN74ACT3642	1K × 36 × 2	−15, −20, −30	67	11	DSP
SN74ACT3651	2K × 36	−15, −20, −30	67	11	DSP
SN74ABT3611	64 × 36	−15, −20, −30	67	10	High Bandwidth
SN74ABT3612	64 × 36 × 2	−15, −20, −30	67	10	High Bandwidth
SN74ABT3613	64 × 36	−15, −20, −30	67	10	Internetworking
SN74ABT3614	64 × 36 × 2	−15, −20, −30	67	10	Internetworking

Advanced Bus-Matching/ Byte-Swapping Features for Internetworking FIFO Applications

Tom Jackson
Advanced System Logic – Semiconductor Group

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Introduction

Bus matching and byte swapping are features that Texas Instruments (TI) has added to their internetworking family of application-specific, first-in first-out memories (FIFOs). The first two FIFOs available are the SN74ABT3614 and SN74ABT3613. The bus-matching feature allows the user to dynamically select the desired bandwidth, either long-word format (36 bits), word format (18 bits), or byte format (9 bits) for mixed-bus systems. Byte swapping allows the user to reconfigure protocols for different microprocessor-based systems, such as big-endian format (i.e., RISC-based microprocessors such as the MC68000, IBM370) where the most significant bit (MSB) is 0 or little-endian format (i.e., CISC-based microprocessors such as iPAX, x86, DEC VAX) where the least significant bit (LSB) is 0 (see Figure 1). The bus-matching and byte-swapping features can be used independently or in conjunction with one another, which allows the user a wide range of possible solutions.

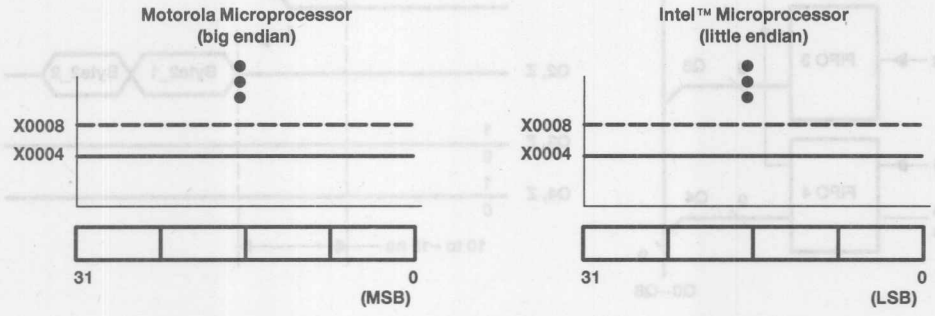


Figure 1. Big-Endian and Little-Endian Formats

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Conventional Bus-Matching Data Reads

With the evolution of 32-bit microprocessors and digital signal processors (DSPs), designers must add large complex discrete circuits to provide data continuity between mixed data-bus systems. A typical solution requires four 9-bit FIFOs and considerable board space (see Figure 2).

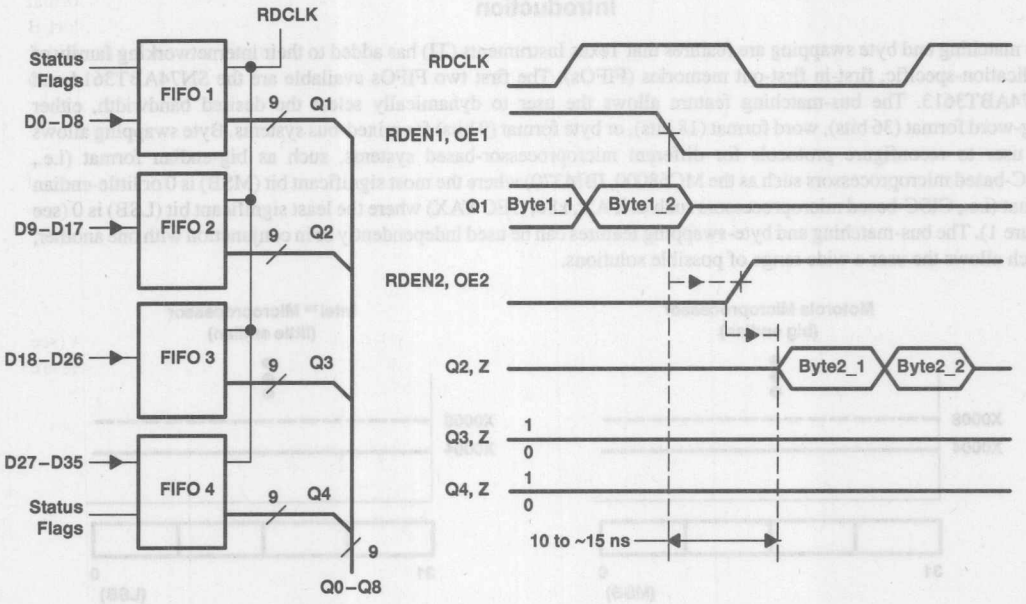


Figure 2. Data-Read Cycle for 36-Bit to 9-Bit Bus Matching

To provide bus matching from a 36-bit bus to a 9-bit bus, access time and flag synchronization are critical issues due to the combination of separate components. Figure 2 shows the required circuitry and associated timing diagram for a conventional bus-matching operation. The first byte of the long word is written into FIFO1 on D0–D8. On the rising edge of the read clock with read enable-1 (RDEN1) and output enable-1 (OE1) held high, the first byte of FIFO1 (byte 1_1) is read out. During that first read cycle, the remaining three FIFOs must be disabled. Before reading the second byte from FIFO2 (byte 2_1), the read enables and output enables of FIFO1 are asserted low, putting the FIFO outputs into 3-state, which prevents any bus-arbitration problems. FIFO1 must be disabled before FIFO2 is enabled.

In addition to the associated propagation delays of enabling and disabling the FIFOs, the typical access time of a single FIFO can range from 10 to 20 ns. To ensure proper device synchronization, the FIFO access time must be increased to allow for the propagation delays of the control signals. The increased propagation time for data reads can cause a bottleneck for data that is waiting to be written into the other FIFOs. This delay dramatically impacts system performance and data throughput. If the timing parameters are violated, the result is bus contention and lost data. To complete the long-word read, the cycle is repeated three more times. For subsequent long-word data reads, the process begins with the second byte of FIFO1 (byte 1_2). This data *ping-ponging* is prolonged and requires excessive access times and data setup and hold times to perform a single long-word read cycle. These factors contribute to reducing the effective maximum operating frequency of the system.

TI's Bus-Matching Data Reads

TI has designed the internetworking FIFOs to provide the user a single-chip solution for dynamic bus matching, in addition to fast data access times (t_a = 10 ns). The bus-matching feature offers a flow-through architecture that maintains port-to-port transparency and eliminates the need for any bus-arbitration control logic. Bus matching is performed with the FIFO on the port B bus and can be configured in long-word format (36 bits), word format (18 bits), or byte format (9 bits) for data reads from FIFO1 or written to FIFO2, in the case of the SN74ABT3614 bidirectional FIFO. Port-B bus size can be changed dynamically and synchronous to CLKB to communicate with peripherals of various bus widths. The bus-matching feature is implemented using the big-endian ($\overline{BE}$) format and the port-B bus size-select (SIZ0, SIZ1) terminals (see Table 1).

Table 1. Bus Size-Select Terminals

PACKAGE	TERMINAL NUMBER		
	$\overline{BE}$	SIZ1	SIZ0
120-pin TQFP (PCB)	47	50	51
132-pin PQFP (PQ)	132	129	128

The sizing function is performed on the output of port B after a long word has been written into the FIFO on port A (see Figure 3). If an output register is not used (e.g., 9- or 18-bit data reads), no line terminations such as pullup resistors are required due to the bipolar output structures of TI's advanced BiCMOS technology.

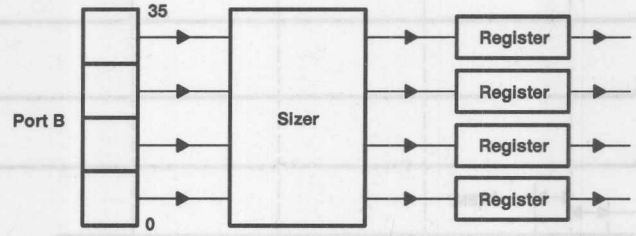


Figure 3. Bus Sizer

By varying the assertion levels of the three control terminals, five different bus-format configurations can be selected (see Table 2).

Table 2. Bus Configurations

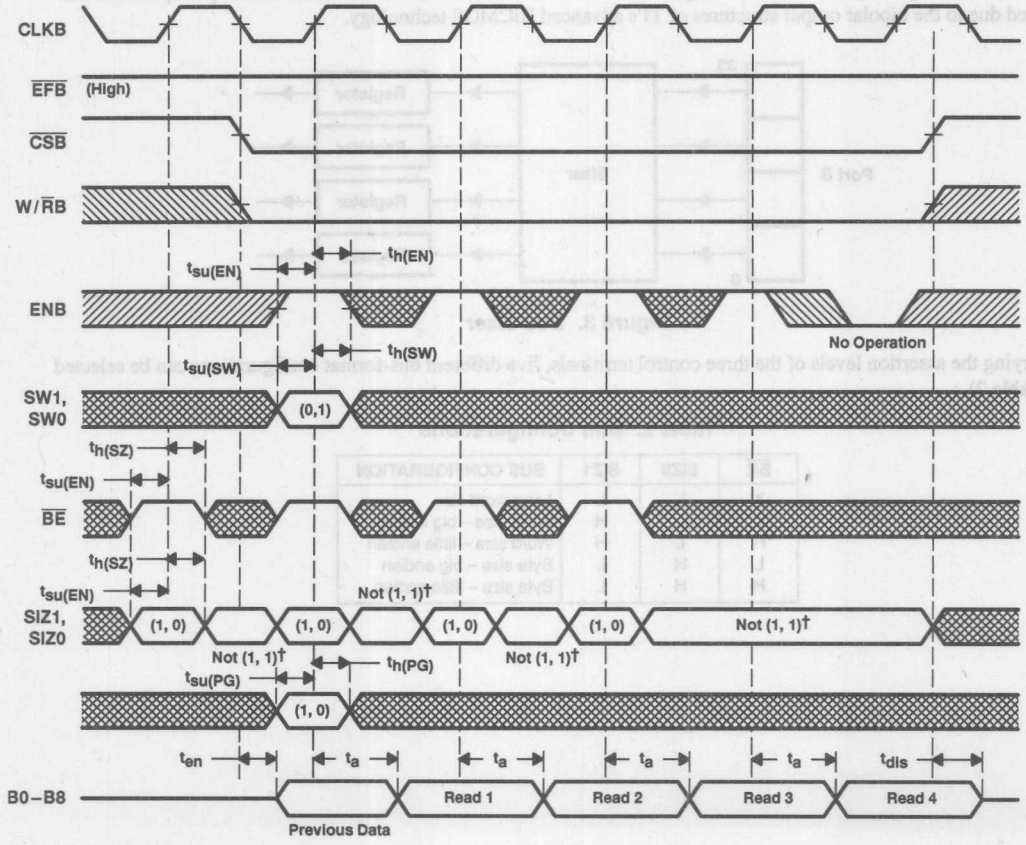
$\overline{BE}$	SIZ0	SIZ1	BUS CONFIGURATION
X	L	L	Long-word size
L	L	H	Word size – big endian
H	L	H	Word size – little endian
L	H	L	Byte size – big endian
H	H	L	Byte size – little endian

The byte-order arrangement of data that is read from or written to the FIFO can be changed synchronous to the clock. The bytes are rearranged within the long word, but the bit order within the bytes remains constant. The byte-swapping feature is implemented by asserting port-B byte-swap select (SW0, SW1) terminals (see Table 3).

Table 3. Byte-Swap Select Terminals

PACKAGE	TERMINAL NUMBER	
	SW1	SW0
120-pin TQFP (PCB)	48	49
132-pin PQFP (PQ)	131	130

The example as shown in Figure 4 takes the conventional 36-bit to 9-bit bus-matching example as shown in Figure 2 one step further by incorporating the byte-swapping feature. A timing diagram of a little-endian, byte-size, byte-swap data read from port B using the SN74ABT3613 unidirectional FIFO is shown in Figure 4. With a 36-bit-long word written into memory from port A, data read can be performed. On the rising edge of CLKB with the port-B chip select ($\overline{CSB}$) asserted low, the size and swap functions can be selected. The little-endian format is chosen by asserting $\overline{BE}$ high. Byte size is selected by asserting SIZ1 high and SIZ0 low. On the second clock cycle, the byte swap is performed by asserting SW1 low and SW0 high for one clock cycle.



† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.

Figure 4. Port-B Data-Read Cycle for 36-Bit to 9-Bit Bus Matching

During the second clock cycle, the first byte appears on the output bus B0–B8. After four successive read cycles are completed, the entire long word is parsed out onto the bus in four 9-bit data packets (see Figure 5). In byte-size or word-size data reads, the unused bytes hold the last FIFO output values. After the four bytes are read, the configuration can be dynamically changed.

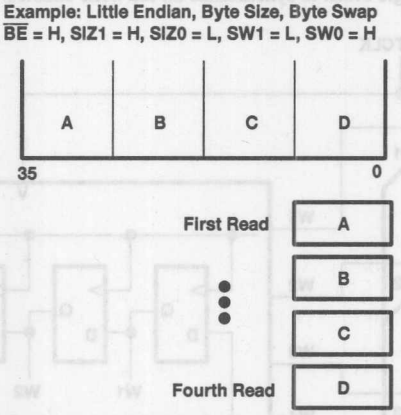


Figure 5. Little-Endian Data-Output Structure

If the example shown in Figure 4 is configured for big-endian format, the data is output on bus B27–B35 (see Figure 6 and Figure 7). No line termination is required for the unused data outputs. This is a dramatic improvement, not only in design ease, but in performance over the conventional data *ping-ponging* technique shown in Figure 2.

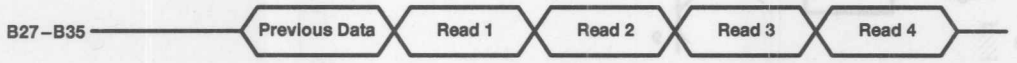


Figure 6. Big-Endian Data Output

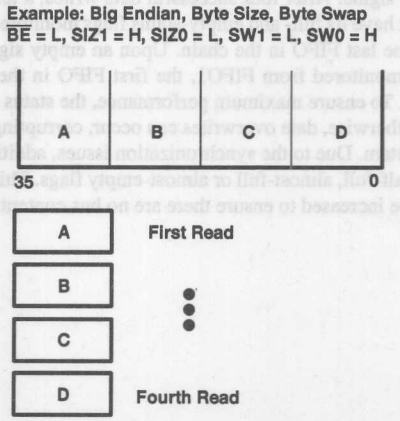


Figure 7. Big-Endian Data-Output Structure

Conventional Bus-Matching Data Writes

Conventional bus-matching data writes experience the same timing restrictions as data reads. The example in Figure 8 shows the circuitry required for 9-bit to 36-bit data writes. Just as in the example in Figure 2, four 9-bit FIFOs are required in addition to an extra control-logic block to synchronize all the write enables.

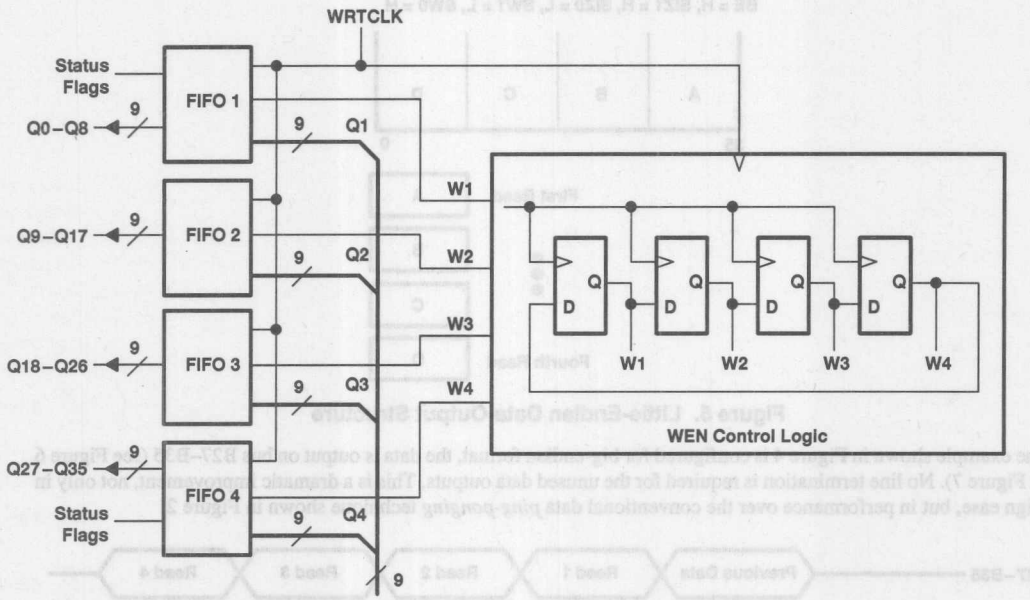
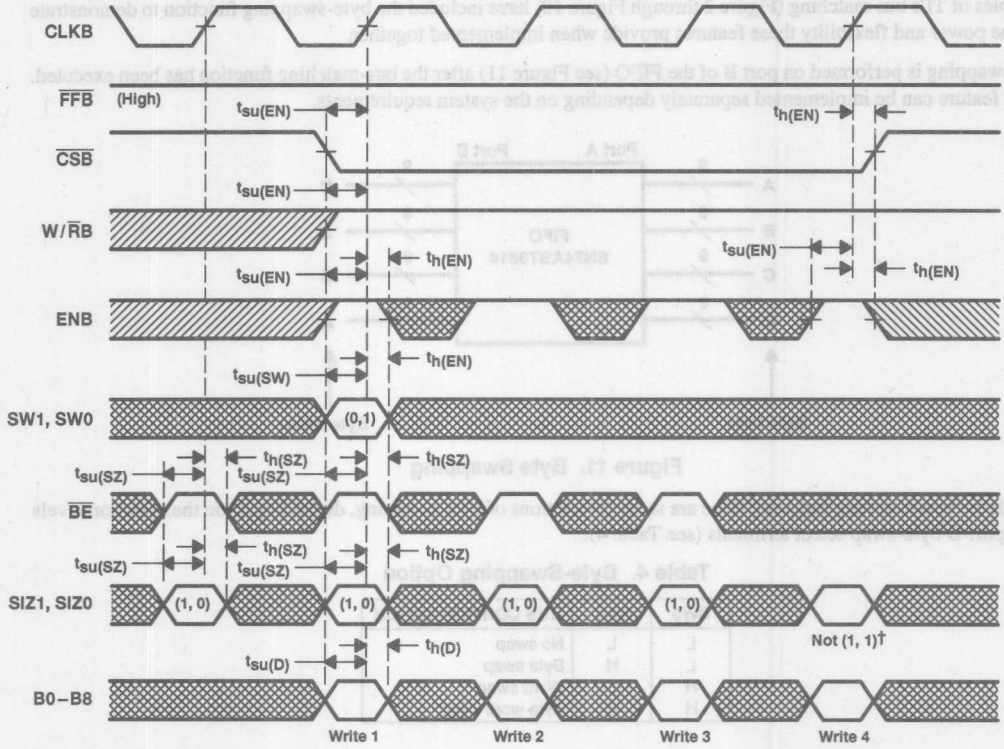


Figure 8. Data-Write Cycle for 9-Bit to 36-Bit Bus Matching

The write-control logic controls each data write in a round-robin style. The control logic consists of a bank of flip-flops that generate the appropriate write-enable signal. After four successful data writes, a long word can be read from the FIFO bank. However, the FIFO bank must have its full- and empty-status flags monitored to ensure data integrity. The empty status is monitored from FIFO4, the last FIFO in the chain. Upon an empty signal, additional data reads are immediately disabled. The full status is monitored from FIFO1, the first FIFO in the chain. When a full status is indicated, further data writes are disabled. To ensure maximum performance, the status flags require fast propagation delays for proper data synchronization. Otherwise, data overwrites can occur, corrupting the FIFO data, or additional wait states must be introduced into the system. Due to the synchronization issues, additional bus control or interrupts become extremely difficult by using the half-full, almost-full or almost-empty flags. This also limits FIFO operations. The data setup and hold times also must be increased to ensure there are no bus contentions during a write operation.

TI's Bus-Matching Data Writes

The timing diagram for performing a little-endian, byte-size, byte-swap data write to port B of FIFO2 using the SN74ABT3614 is shown in Figure 9. By implementing TI's SN74ABT3614 bidirectional FIFO in a design, bus matching can be performed in either direction without the need for additional glue logic or loss of system performance.



† SIZ0 = H and SIZ1 = H writes data to the mail2 register.

Figure 9. Port-B Data-Write Cycle for 9-Bit to 36-Bit Bus Matching

On the rising edge of CLKB with the port B selected ($\overline{CSB}$), the size and swap functions can be selected. The little-endian format is chosen by asserting $\overline{BE}$ high. Byte swap is selected by asserting SIZ0 high and SIZ1 low. These assertion levels are maintained for the entire write cycle. On the second clock cycle, the byte swap is performed by asserting SW1 low and SW0 high for one clock cycle. The data is then written into B0–B8, since the little-endian format has been selected.

If Figure 9 is configured for big-endian format, the data is written into B27–B35 (see Figure 10). No line termination in the form of pullup resistors is required for the unused data inputs.



Figure 10. Big-Endian Format of Byte Write

TI's Byte-Swapping Feature

TI has designed the internetworking FIFOs to provide designers maximum flexibility and ease of use. In addition to the bus-matching feature, a byte-swapping option has been added. The byte-swapping feature allows communication between systems with mixed bus protocols such as those using by RISC and CISC microprocessors. The previous examples of TI's bus matching (Figure 2 through Figure 10) have included the byte-swapping function to demonstrate the true power and flexibility these features provide when implemented together.

Byte swapping is performed on port B of the FIFO (see Figure 11) after the bus-matching function has been executed. Either feature can be implemented separately depending on the system requirements.

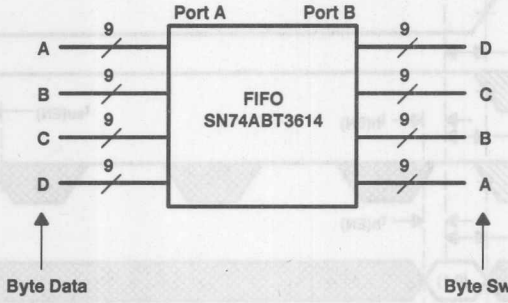


Figure 11. Byte Swapping

As with the bus-matching function, there are several variations of byte swapping, depending upon the assertion levels of the port-B byte-swap select terminals (see Table 4).

Table 4. Byte-Swapping Option

SW0	SW1	BUS CONFIGURATION
L	L	No swap
L	H	Byte swap
H	L	Word swap
H	H	Byte-word swap

Bus matching and byte swapping are performed in the following sequence for all data reads; the 36-bit word is first read, the swap is performed, followed by the bus-size function. The converse is true for data writes.

Conclusion

The ability to dynamically select the desired bus configuration and format is a very useful feature for today's designs. Many systems, such as network switches and routers, implement high-speed backplanes that are typically 32 to 36 bits to ensure maximum bandwidth for data; however, there are many 8-bit and 16-bit controllers and buses in existence. TI's bus-matching feature ensures a flow-through, high-speed architecture that permits multiple logical permutations. There is no longer the need for rerouting bytes on buses and manually controlling bus arbitration through a large and costly discrete solution. The SN74ABT3613 FIFO provides a unidirectional datapath with bus matching and byte swapping on port B. The SN74ABT3614 provides a full bidirectional datapath and supports bus matching and byte swapping in either direction. Both of these FIFOs feature TI advanced-clocked architecture in a space-saving single-chip solution that offers a maximum clock speed of 67 MHz with 10-ns access time.

Parity-Generate and Parity-Check Features for High-Bandwidth-Computing FIFO Applications

Tom Jackson
Advanced System Logic – Semiconductor Group

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Introduction

Parity-generate and parity-check features are available in both the internetworking family of first-in, first-out memories (FIFOs), SN74ABT3614 and SN74ABT3613, and the high-bandwidth-computing family, SN74ABT3612 and SN74ABT3611. Parity generate and parity check are needed in high-bandwidth and high-speed computing applications where demanding data integrity levels are required. All of TI's 36-bit FIFOs have bidirectional mailbox registers that allow quick access to data by bypassing the FIFO static random-access memory (SRAM) core. The same input/output (I/O) is shared between the mailbox registers and the FIFO data registers that allow parity generate and parity check on both the FIFO memory data and the mailbox-register data. The parity-generate and parity-check features are designed for fault-tolerant systems, such as those in computing and telecom that require error-detection techniques, in addition to many of today's microprocessors that have provisions for parity detection.

Parity-Generate Feature

The parity-generate feature enables the user to generate odd or even parity in the most significant bit (MSB) of each byte on either port A or port B of the FIFO. Odd and even parity are defined as follows:

Odd parity: The parity bit is set to one for an even number of ones, including the parity bit.

Even parity: The parity bit is set to zero for an odd number of ones, including the parity bit.

Parity is generated for data reads from either port A or port B of a bidirectional FIFO by asserting parity generate A (PGA) and parity generate B (PGB), respectively (CSA/B low, PGA/B high, ENA/B high). In Figure 1, a write to a FIFO or mailbox register stores the levels applied to all 36 inputs, regardless of the state of the parity-generate input PGB. When data is written to a port, the lower eight bits of each byte are copied to the parity-generate tree. These bits are then used to generate a parity bit according to the level of the ODD/$\overline{\text{EVEN}}$ select pin (see Table 1). When PGB is asserted, the results of the parity generator are written to the MSB of the output register. If PGB is low, the original contents of the MSB of the byte under consideration are transferred to the corresponding location in the output register.

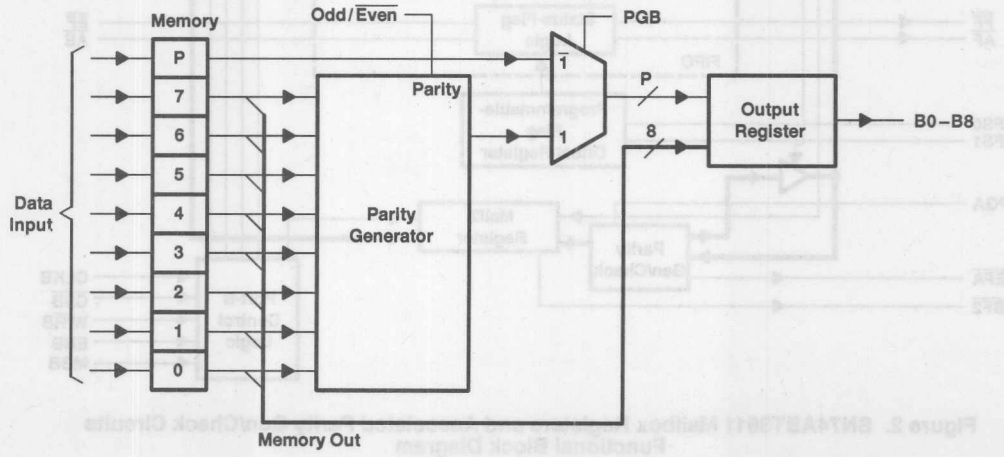


Figure 1. Parity-Generate Circuit

Table 1. Parity-Generate Input Pins

PACKAGE	PIN NUMBER		
	$\overline{PEFA}$	$\overline{PEFB}$	ODD/$\overline{EVEN}$
120-pin TQFP (PCB)	39	53	44
132-pin PQFP (PQ)	9	125	3

Each mailbox register has an associated parity-generate and check (gen/check) circuit (see Figure 2) that enables parity to be generated and checked on either port of the FIFO. The circuit that generates parity for the Mail1 mailbox register is shared by the port-B bus (B0–B35) and generates and checks parity for the FIFO data bus, as well as to check parity for the Mail2 mailbox register. The circuit that generates parity for the Mail2 mailbox register is shared by the port A bus (A0–A35) to check parity for FIFO data and mailbox register. The shared parity trees of a port generate parity bits for the data in a mailbox register when the port write/read select input is low, port-mail select input is high, and port-parity-generate select is high. Generating parity for mail register data does not change the contents of the register.

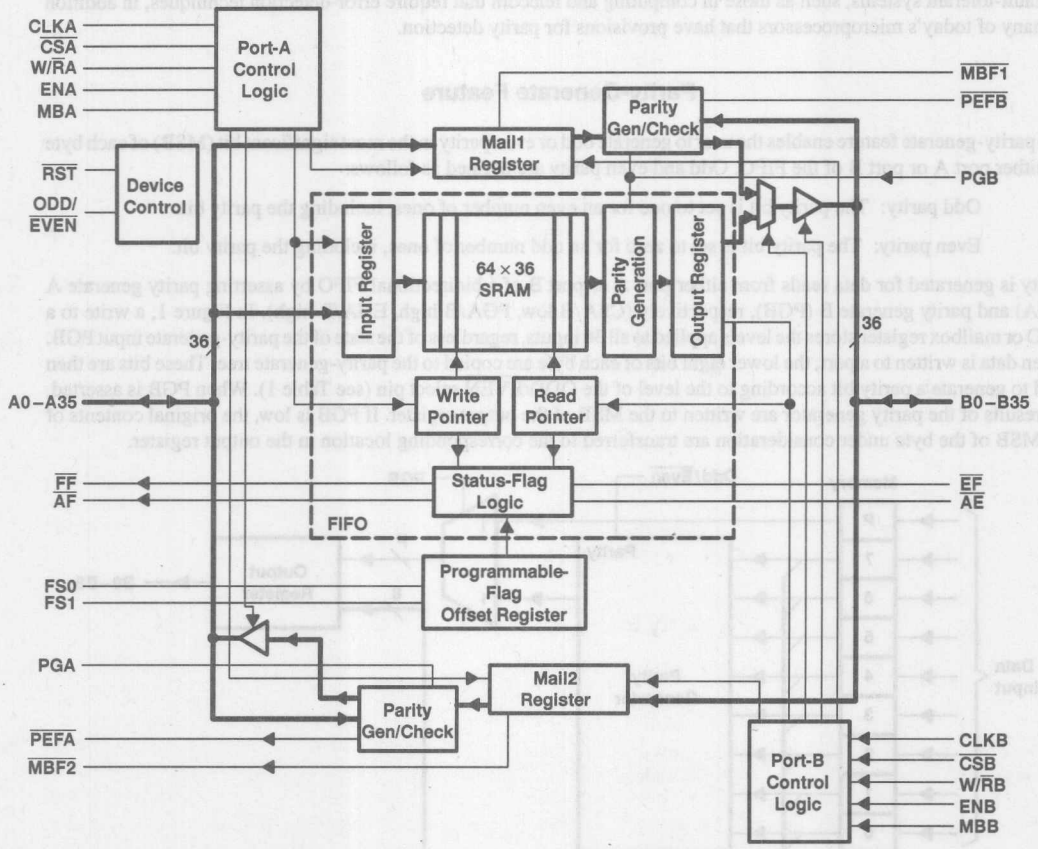


Figure 2. SN74ABT3611 Mailbox Registers and Associated Parity Gen/Check Circuits Functional Block Diagram

The parity-generate and parity-check features allow the user to select odd or even parity and to passively check the results of all incoming data to either port A or port B of the FIFO without disrupting normal operations. Both port A (A0–A35) inputs and port B (B0–B35) inputs have four 9-bit parity trees to check the parity of incoming or outgoing data (see Figure 3). Parity is checked on the ninth MSB of each byte.

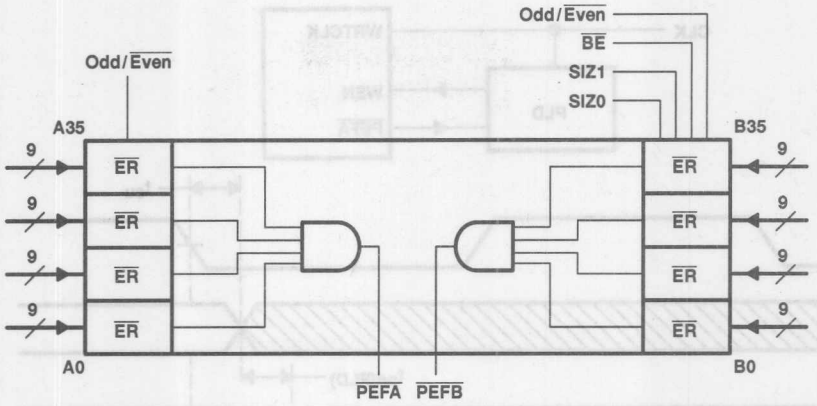


Figure 3. Parity Trees

A parity failure on one or more bytes of the input bus is indicated by a low level on the port parity-error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) (see Table 2). The parity-error flags can be ignored if this feature is not desired.

Table 2. Parity-Error Input Pins

PACKAGE	PIN NUMBER		
	PGA	PGB	ODD/$\overline{\text{EVEN}}$
120-pin TQFP (PCB)	38	54	44
132-pin PQFP (PQ)	10	124	3

The user can choose odd or even parity by asserting the ODD/$\overline{\text{EVEN}}$ input or allow the FIFO to default to even parity. In this manner, the user can select the parity format that best fits the application requirements. Since four 9-bit parity trees are used, it is possible to implement the parity-check function on the bus-configuration port in conjunction with the bus-matching feature of the internetworking FIFOs. In this manner, any bus width that has been selected, 9-bit through 36-bit, can have parity checked. The parity-checking circuit is designed to ignore all error flags that may be generated on unused bytes.

As in parity generate, the four parity trees used to check the port-A inputs are shared by the Mail2 mailbox register. Port-B inputs on bidirectional FIFOs are shared by the Mail1 mailbox register (see Figure 2); therefore, parity errors are detected before the data is entered into the FIFO SRAM core.

Using Parity Error to Force an Exception

Although the parity-check feature is passive, it permits the designer to disregard data before it is written into the FIFO SRAM core. This type of functionality is easily implemented by the circuit shown in Figure 4. Since parity is checked on the inputs before being written to the FIFO, it is possible to capture the erred data and force an exception. Figure 4 shows a data error that has been detected by a low on $\overline{\text{PEFA}}$. The associated propagation delay, [$t_{pd(D-PE)}$] of a valid error flag is 10 ns for the –15 speed sort. This allows adequate time for a fast programmable logic device ($t_{pd\ PLD}$) to disallow a data write prior to the data becoming valid. If no parity error is detected, the data write is performed. If FIFOs with slower speed sorts (–20, –30) are used, the associated propagation delay is increased. This method eliminates the need for external counters to track the erroneous data through the FIFO to the output. By forcing an exception, the parity is captured and the clock cycle passes without writing the data to the FIFO memory core.

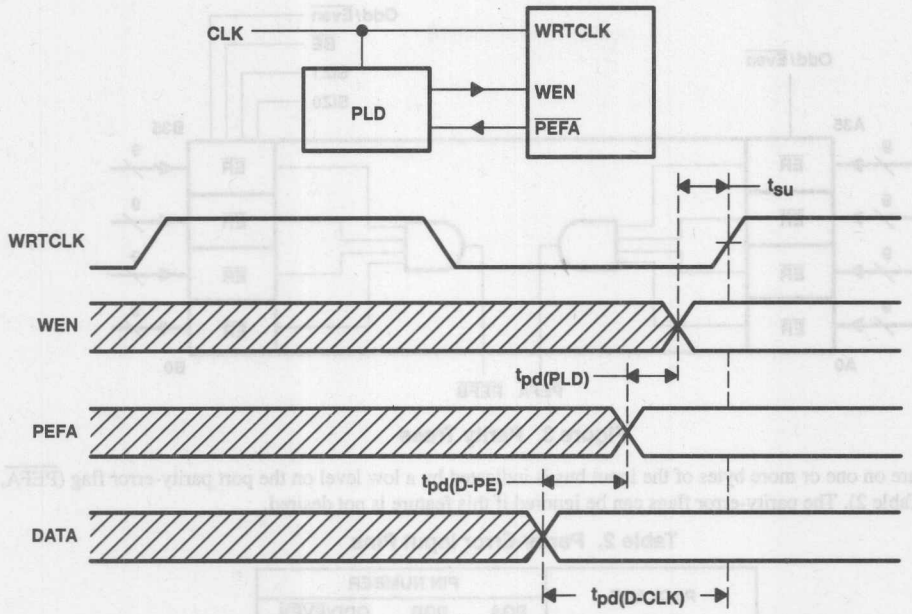


Figure 4. Parity-Error Exception Circuit

Conclusion

As systems become more integrated and bus speeds increase, there is a growing need to ensure data integrity. When parity generate or parity check is required by dynamic random-access memory (DRAM) refresh cycles, bus noise, or other card-to-card performance issues, TI's parity-generate and parity-check features provide a high-speed, space-saving alternative.

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Multiple-Queue First-In, First-Out Memory SN74ACT53861

Peter Forstner
Semiconductor Group

SCAA026A

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Introduction

This application report presents a detailed description of the versatile functions of the SN74ACT53861 multiple-queue (Multi-Q™) first-in, first-out (FIFO) memory. Examples of circuits show how the device can be controlled and cascaded. Typical application examples show how the device can be used in asynchronous transfer mode (ATM) telecommunications exchange systems.

Memories are indispensable circuit components of digital-system subassemblies. There are a large number of memories in various configurations for many application requirements. Each memory is suited for specific and specialized applications.

One of these specialized memories is the FIFO memory, which provides intermediate storage of data being transferred between two electronic systems. The designation FIFO indicates how the data flows. A FIFO has separate data input and data output; however, the first word of data written into the memory is the first to leave when it is read (see Figure 1). Within the FIFO, words of data wait in a data queue. If a FIFO is configured between two systems that are working asynchronously, the FIFO must be able to manage the synchronization of the data flow to both systems to prevent metastable situations.

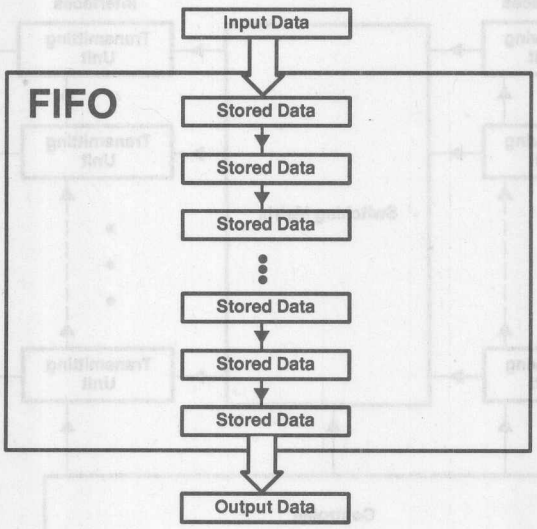


Figure 1. FIFO Data Flow

FIFOs differ from one another in their word widths, memory capacity, and in the way they are controlled. Texas Instruments (TI) offers FIFOs with word widths from 1 to 36 bits and memory capacities from 64 to 4096 words. Because FIFOs have alternative methods of control, TI offers strobed FIFOs and clocked FIFOs. A detailed description of the various methods of controlling FIFOs can be found in other TI application reports. The various word widths and memory capacities available are described in the 1996 *High-Performance FIFO Memories Data Book*, literature number SCAD003C.

In addition to standard FIFOs, versions for special purposes have been designed for specific applications. The TI Multi-Q FIFO is an application-specific FIFO designed for ATM telecommunications exchange systems.

Multi-Q is a trademark of Texas Instruments Incorporated.

Main Areas of Application

The SN74ACT53861 Multi-Q FIFO is designed specifically for ATM telecommunications exchange systems.

As shown in Figure 2, ATM telecommunications exchange systems can have three functional parts:

- Receiving unit (one per channel)
- Switching matrix
- Transmitting unit (one per channel)

The ATM used for data transmission supplies the receiving unit with digital information, which is usually apportioned in cells having a length of 53 bytes. Each cell consists of a 5-byte cell header and a 48-byte payload. The cell header includes:

- Ultimate destination: virtual channel identifier (VCI)
- Immediate next destination, i.e., the next ATM exchange installation through which the ultimate destination is reached: virtual path identifier (VPI)
- The type of information contained in the cell: payload type (PT)
- The importance, or priority, of the cell: cell-loss-priority (CLP) bit
- Error-correction controller: header error control (HEC)

In certain applications, extending the cell header by one to two bytes provides the ATM exchange installation with internal information (tagged cells) (see Figure 3).

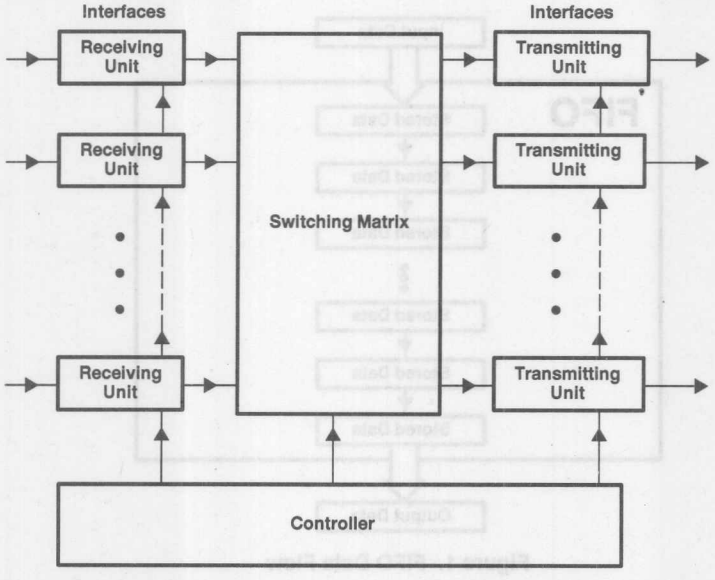


Figure 2. ATM Telecommunications Exchange System Block Diagram

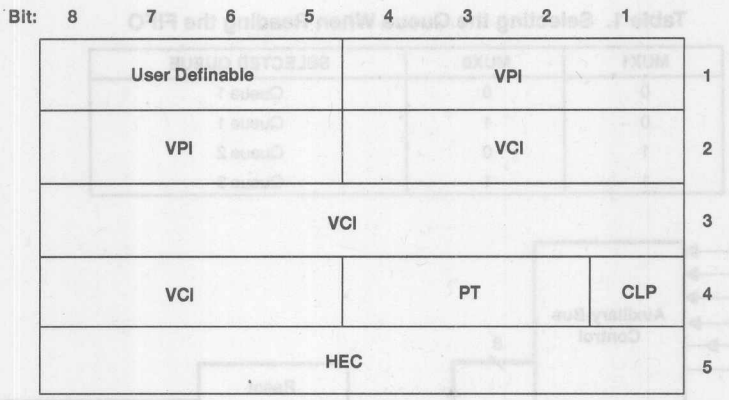


Figure 3. ATM-Header Structure

If delays occur because transmission channels in the ATM exchange are not available, the Multi-Q FIFO allocates cell priorities, known as quality of service (QOS), by interpreting the PT information and the CLP bit in the cell header. Data that is critical as to the time taken for transmission, such as audio or video signals, is swept more rapidly through the ATM exchange than, for example, less critical computer data. If the CLP bit is set to 0, the cell contains important data that must reach its destination; whereas cells with the CLP bit set to 1 can be deleted. In a digital ATM exchange system, a priority control for cell transmission must be implemented.

The cells being received arrive asynchronously to the clock signal of the exchange system; therefore, synchronization of the input data stream to the system clock is necessary.

The Multi-Q FIFO solves synchronization problems and controls transmission priority with minimal complexity. The architecture of this FIFO, unlike conventional FIFOs, is not based on words of data but on cells. This device can control up to three priorities. The writing of the input data can be performed completely asynchronously with respect to the reading of the output data.

The Multi-Q FIFO

The most remarkable feature of the Multi-Q FIFO is that memory can be allocated to three independent queues. These queues allow the implementation of three QOS priorities.

Construction of the Multi-Q FIFO

Figure 4 shows the functional block diagram of the Multi-Q FIFO, which is clocked; i.e., it has inputs for free-running write and read clocks. Write accesses occur at the rising edges of the write clock when one of the three write-enable-x, (WRTENx) (x = 1, 2, or 3) lines is set. Read accesses are implemented at the rising edges of the read clock by setting the read-enable (RDEN) line. Reading or writing stops when a low level is applied to WRTENx or RDEN. For writing operations, the three control lines, WRTENx per queue, are individually brought out. The control lines for write accesses are operated by a multiplexer. The desired queue is chosen with MUX0 and MUX1 selecting access to the chosen queue using RDEN (see Table 1).

Before use, this device must be reset by four rising edges of the write clock (WRTCLK) and four rising edges of the read clock (RDCLK) while the reset input ($\overline{RST}$) is high.

Table 1. Selecting the Queue When Reading the FIFO

MUX1	MUX0	SELECTED QUEUE
0	0	Queue 1
0	1	Queue 1
1	0	Queue 2
1	1	Queue 3

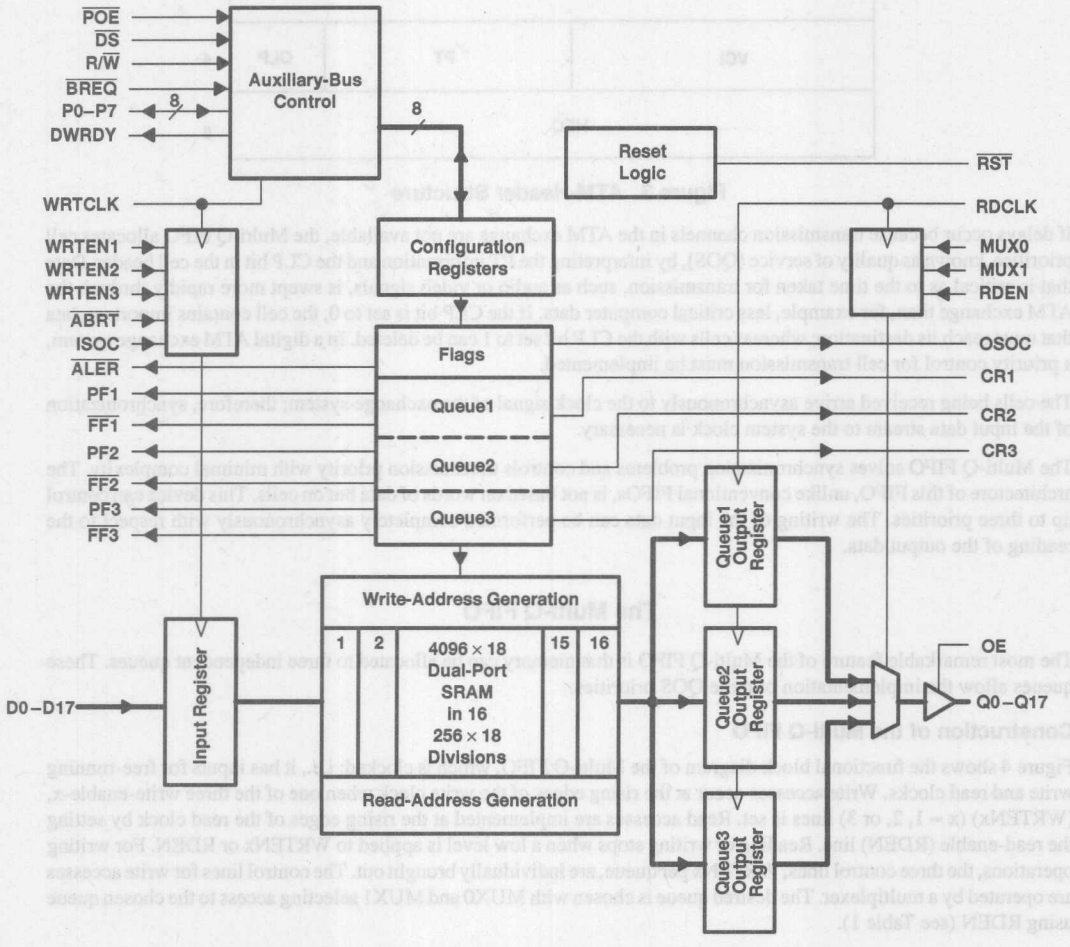


Figure 4. Multi-Q FIFO Functional Block Diagram

Configuration Registers

Eleven configuration registers allow matching the FIFO to requirements of a particular application (see Table 2). These configuration registers can be written to and read from using a microcontroller through the auxiliary-bus control interface.

Table 2. Configuration Registers

REGISTER SYMBOL	REGISTER NAME	NO. OF BITS	DEFAULT VALUE	PROGRAMMABLE RANGE	FUNCTION
PORT	Port control	5	0	Bit-slice control	Chooses the data input and output bus size and format. Controls output byte destuffing.
QL1	Queue 1 length	5	8	0–16	Defines the number of 256 x 18 memory blocks for Queue 1
QL2	Queue 2 length	4	6	0–15	Defines the number of 256 x 18 memory blocks for Queue 2
QL3	Queue 3 length	4	2	0–15	Defines the number of 256 x 18 memory blocks for Queue 3
CLSZ	Cell size	6	27	10–32	Defines the cell size in 18-bit words
PF1_W	Programmable flag 1, write threshold	9	71	0–409	Defines the number of cells in Queue 1 to set PF1 low
PF1_R	Programmable flag 1, read threshold	9	70	1–408	Defines the number of cells in Queue 1 to set PF1 high
PF2_W	Programmable flag 2, write threshold	9	51	0–383	Defines the number of cells in Queue 2 to set PF2 low
PF2_R	Programmable flag 2, read threshold	9	50	1–382	Defines the number of cells in Queue 2 to set PF2 high
PF3_W	Programmable flag 3, write threshold	8	13	1–383	Defines the number of cells in Queue 3 to set PF3 low
PF3_R	Programmable flag 3, read threshold	8	12	0–382	Defines the number of cells in Queue 3 to set PF3 high

Allocation of Queues

The Multi-Q FIFO memory consists of 4096 18-bit words that have a maximum of three independent queues. These queues can be called up to control up to three QOS priorities of ATM cells. Using configuration registers QL1, QL2, and QL3, the sizes of the individual queues can be allocated in steps of 256 18-bit words. The initial value of QL1 = 8 if Queue 1 has a size of $8 \times 256 = 2048$ 18-bit words. The development engineer has access only to configuration registers QL1 and QL2 and can only determine the size of the first two queues; after that, the Multi-Q FIFO automatically reserves the part of the memory that is still available for the third queue. Programming queue lengths of zero allocates the memory to one or two queues.

The word width of the memory is 18 bits; however, the development engineer can choose between 9-bit and 18-bit access when reading and writing. In these cases, the bus widths for reading and writing operations can be different. For example, it is possible to write with 9-bit access but implement the reading cycle with a word width of 18 bits. If the 9-bit access is chosen, the FIFO can write the first 9-bit word to the lower significant half of the 18-bit memory and the second 9-bit word to the higher significant half (little endian). Alternatively, this order can be reversed (big endian). The programming for write accesses is performed in the configuration register PORT using bits INSIZ, OUTSIZ, and INBE (see Table 3). With read accesses, the 9-bit data word is output on bits Q8–Q0 in little-endian data format and on the bits Q17–Q9 in big-endian format. In this case, the hardware wiring determines the data format; whereas with the input data, the software programming determines the data format.

Table 3. Port-Control Register PORT

OUTSTF Bit 4	OUTSIZ Bit 3	INST Bit 2	INBE Bit 1	INSIZ Bit 0	FUNCTION
X	X	X	X	0	18-bit input bus
X	X	0	0	1	9-bit input bus with an even number of bytes per cell in little-endian data format
X	X	0	1	1	9-bit input bus with an even number of bytes per cell in big-endian data format
X	X	1	0	1	9-bit input bus with an odd number of bytes per cell in little-endian data format
X	X	1	1	1	9-bit input bus with an odd number of bytes per cell in big-endian data format
X	0	X	X	X	18-bit output bus
0	1	X	X	X	9-bit output bus with an even number of bytes per cell
1	1	X	X	X	9-bit output bus with an odd number of bytes per cell

Cells Instead of Words of Data

The Multi-Q FIFO flags (e.g., empty, full, etc.) indicate the presence or the absence of complete cells. The cell size can be set with the configuration register CLSZ in the range of 10 to 32 18-bit words to allow a cell size of 20 to 64 bytes. The Multi-Q FIFO can also be programmed to odd cell sizes (e.g., 53 bytes) with 9-bit writing access by byte stuffing and with 9-bit reading access by removing the stuffing bytes (see Figure 5). This property can be chosen in the configuration register PORT with the help of bits INST and OUTSTF (see Table 3).

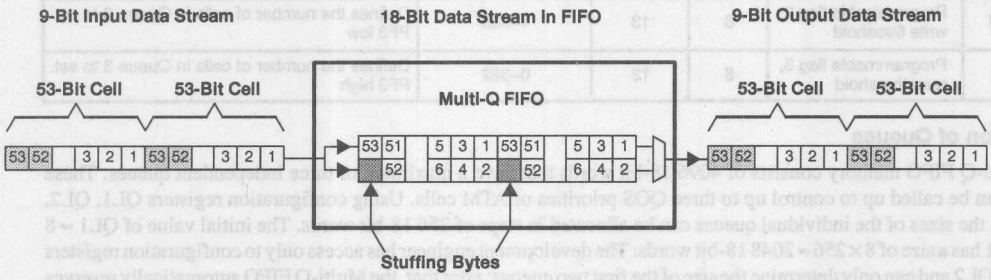


Figure 5. Data Stream With Odd Cell Size

When writing into a cell, the Multi-Q FIFO must be informed of the beginning of a cell with the input start-of-cell (ISOC) signal, as shown in Figure 6. At the rising clock-pulse edge when the first data word of a cell is written into the FIFO, both ISOC and the valid data word must be set high. If a cell has been written completely into the FIFO, ISOC must again be set with the beginning of the next cell. The FIFO compares the beginning of a cell, which has been indicated, with the expected cell beginning in accordance with the previously implemented programming of the cell size and indicates any fault at the alarm ($\overline{\text{ALER}}$) output (see Figure 7 and Figure 8). If a fault of this kind occurs and $\overline{\text{ALER}}$ is low, the fault must be reset with the abort ($\overline{\text{ABRT}}$) input signal before further cells can be written into the FIFO.

When reading from cells, the output start-of-cell (OSOC) signal indicates the beginning of a cell. OSOC can be used to control subsequent parts of the circuit (see Figure 9).

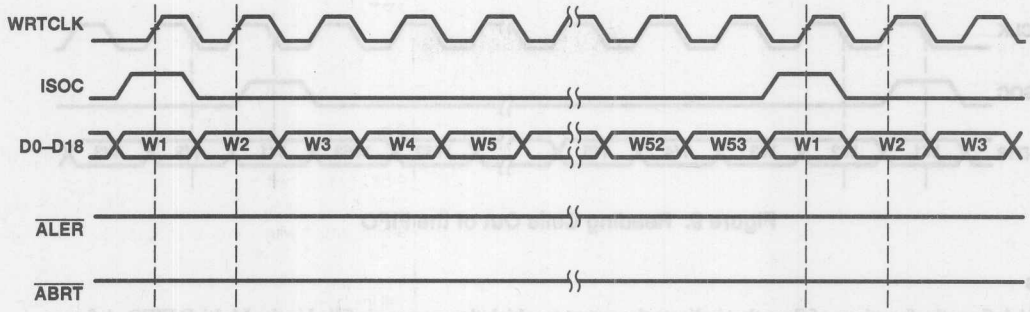


Figure 6. Writing Cells Into the FIFO

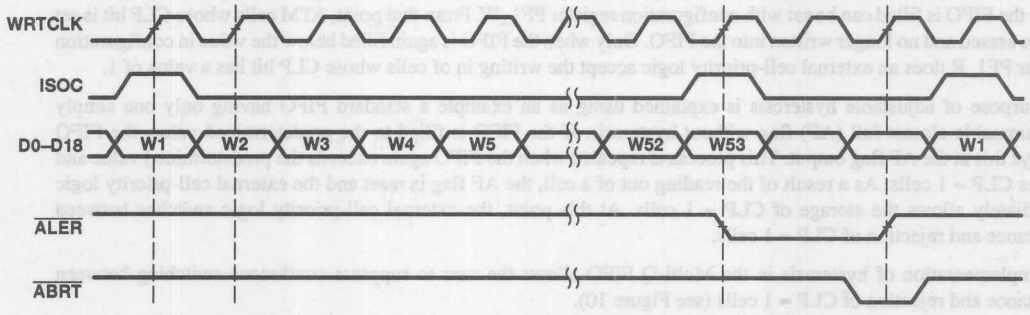


Figure 7. Faulty Writing of Cells Into the FIFO: ISOC Comes Too Soon

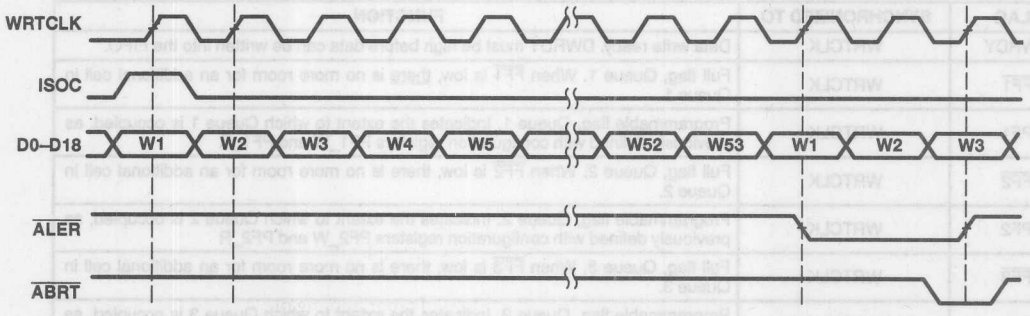


Figure 8. Faulty Writing of Cells Into the FIFO: ISOC Comes Too Late or Not at All

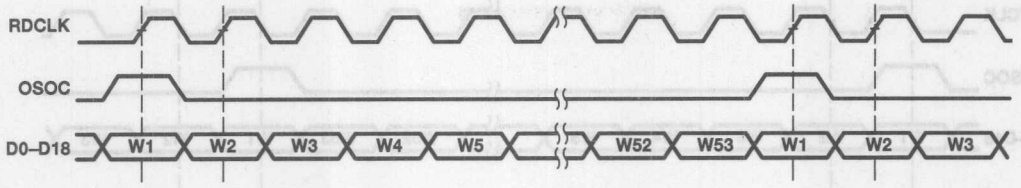


Figure 9. Reading Cells Out of the FIFO

Flags

Table 4 defines the functions of flags that indicate the extent to which the memory is filled in the Multi-Q FIFO. A form of hysteresis is implemented with the programmable flags PF1, PF2, and PF3. The number of required cells in Queue 1 to set PF1 low is determined using the configuration register. At subsequent readout, PF1 is reset to high as soon as the number of the cells still remaining in the memory reaches the value PF1_R in the configuration register. The extent to which the FIFO is filled can be set with configuration register PF1_W. From that point, ATM cells whose CLP bit is set to 1 are erased and no longer written into the FIFO. Only when the FIFO is again filled below the value in configuration register PF1_R does an external cell-priority logic accept the writing in of cells whose CLP bit has a value of 1.

The purpose of adjustable hysteresis is explained using as an example a standard FIFO having only one simply programmable almost-full (AF) flag without hysteresis. If the FIFO is filled to the predetermined value, the FIFO displays this at the AF flag output. This process is repeated when the FIFO again exceeds the predetermined value and ignores CLP = 1 cells. As a result of the reading out of a cell, the AF flag is reset and the external cell-priority logic immediately allows the storage of CLP = 1 cells. At this point, the external cell-priority logic switches between acceptance and rejection of CLP = 1 cells.

The implementation of hysteresis in the Multi-Q FIFO allows the user to suppress continuous switching between acceptance and rejection of CLP = 1 cells (see Figure 10).

Hysteresis can be suppressed by an appropriate choice of threshold values for PF1_W and PF1_R.

Table 4. Multi-Q FIFO Flags

FLAG	SYNCHRONIZED TO	FUNCTION
DWRDY	WRTCLK	Data write ready. DWRDY must be high before data can be written into the FIFO.
$\overline{FF1}$	WRTCLK	Full flag, Queue 1. When $\overline{FF1}$ is low, there is no more room for an additional cell in Queue 1.
PF1	WRTCLK	Programmable flag, Queue 1. Indicates the extent to which Queue 1 is occupied, as previously defined with configuration registers PF1_W and PF1_R
$\overline{FF2}$	WRTCLK	Full flag, Queue 2. When $\overline{FF2}$ is low, there is no more room for an additional cell in Queue 2.
PF2	WRTCLK	Programmable flag, Queue 2. Indicates the extent to which Queue 2 is occupied, as previously defined with configuration registers PF2_W and PF2_R
$\overline{FF3}$	WRTCLK	Full flag, Queue 3. When $\overline{FF3}$ is low, there is no more room for an additional cell in Queue 3.
PF3	WRTCLK	Programmable flag, Queue 3. Indicates the extent to which Queue 3 is occupied, as previously defined with configuration registers PF3_W and PF3_R
CR1	RDCLK	Cell ready, Queue 1. If there is at least a complete cell in Queue 1, CR1 is high.
CR2	RDCLK	Cell ready, Queue 2. If there is at least a complete cell in Queue 2, CR2 is high.
CR3	RDCLK	Cell ready, Queue 3. If there is at least a complete cell in Queue 3, CR3 is high.

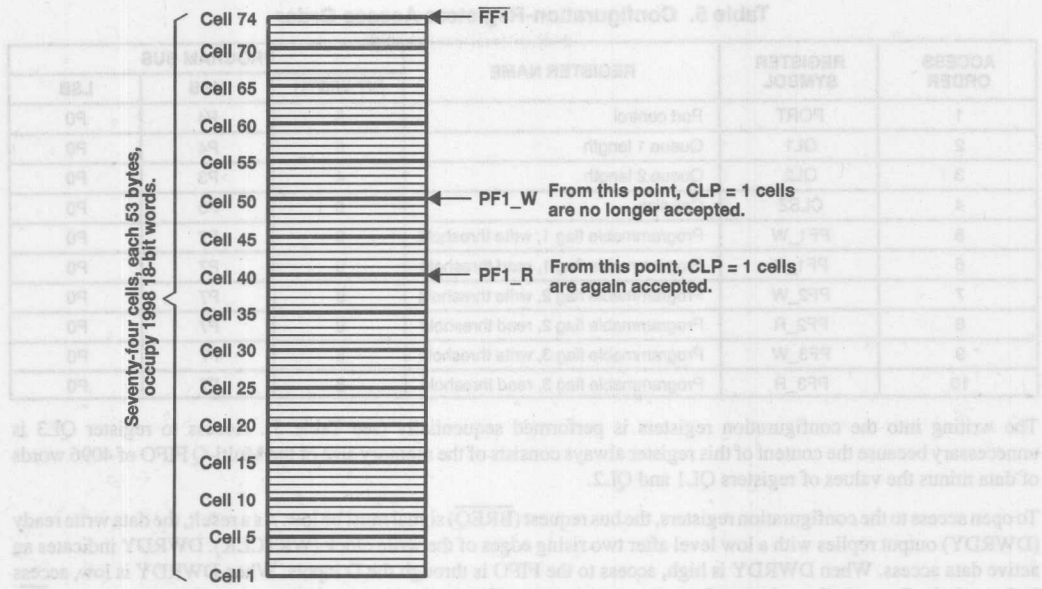


Figure 10. Hysteresis of the PF1 Flags With Configuration Registers PF1_W and PF1_R

Programming

The Multi-Q FIFO can be set up to meet the requirements of a particular application after resetting and before writing in the first word of data with the configuration registers. These registers are written to and read from using a microcontroller via the auxiliary-bus control interface (see Figure 11).

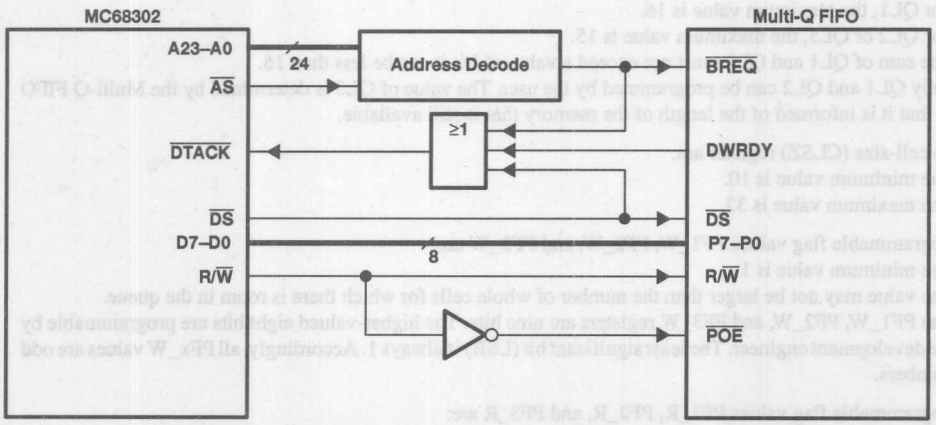


Figure 11. Connection of a Microcontroller to the Auxiliary Bus

Table 5. Configuration-Registers Access Order

ACCESS ORDER	REGISTER SYMBOL	REGISTER NAME	PROGRAM BUS		
			BIT WIDTH	MSB	LSB
1	PORT	Port control	5	P4	P0
2	QL1	Queue 1 length	5	P4	P0
3	QL2	Queue 2 length	4	P3	P0
4	CLSZ	Cell size	6	P5	P0
5	PF1_W	Programmable flag 1, write threshold	9	P7	P0
6	PF1_R	Programmable flag 1, read threshold	9	P7	P0
7	PF2_W	Programmable flag 2, write threshold	9	P7	P0
8	PF2_R	Programmable flag 2, read threshold	9	P7	P0
9	PF3_W	Programmable flag 3, write threshold	8	P7	P0
10	PF3_R	Programmable flag 3, read threshold	8	P7	P0

The writing into the configuration registers is performed sequentially (see Table 5). Access to register QL3 is unnecessary because the content of this register always consists of the memory size of the Multi-Q FIFO of 4096 words of data minus the values of registers QL1 and QL2.

To open access to the configuration registers, the bus request ($\overline{\text{BREQ}}$) signal must be low. As a result, the data write ready (DWRDY) output replies with a low level after two rising edges of the write clock (WRTCLK). DWRDY indicates an active data access. When DWRDY is high, access to the FIFO is through the D inputs. When DWRDY is low, access is through the P terminals to the configuration registers (see Figure 4). At every falling edge of the data strobe ($\overline{\text{DS}}$) signal, the FIFO writes an 8-bit data word from the P terminals in sequence to the configuration registers. If all ten configuration registers from Table 5 are filled with values, the FIFO ignores all further write accesses. Only after a renewed reset of the device are write accesses to the configuration registers again possible.

The following rules apply for the values that are permitted to be written into the configuration registers.

Rules for the length of the queues QL1, QL2, QL3 are:

- The minimum value is 0.
- For QL1, the maximum value is 16.
- For QL2 or QL3, the maximum value is 15.
- The sum of QL1 and QL2 must not exceed a value of 16; it can be less than 16.
- Only QL1 and QL2 can be programmed by the user. The value of QL3 is determined by the Multi-Q FIFO in that it is informed of the length of the memory that is still available.

Rules for the cell-size (CLSZ) register are:

- The minimum value is 10.
- The maximum value is 32.

Rules for programmable flag values PF1_W, PF2_W, and PF3_W are:

- The minimum value is 1.
- The value may not be larger than the number of whole cells for which there is room in the queue.
- The PF1_W, PF2_W, and PF3_W registers are nine bits. The higher-valued eight bits are programmable by the development engineer. The least significant bit (LSB) is always 1. Accordingly, all PFx_W values are odd numbers.

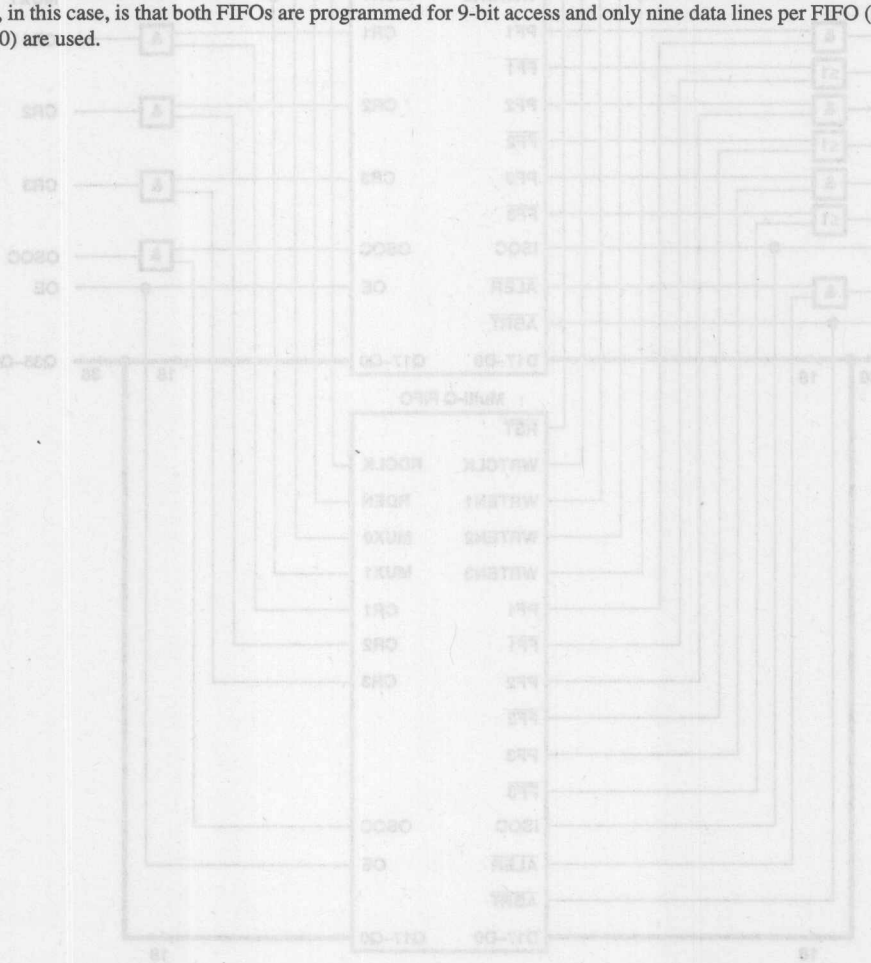
Rules for programmable flag values PF1_R, PF2_R, and PF3_R are:

- The minimum value is 1.
- The value must be smaller than the value of the corresponding PFx_W register.
- The PF1_R, PF2_R, and PF3_R registers each consist of nine bits. The higher-valued eight bits are programmable by the development engineer. The LSB is always 0. Accordingly, all PFx_R values are even numbers.

Extension of Word Width

An extension of word width is possible with a 36-bit access. As shown in Figure 12 (36-bit access), all input control lines must be switched in parallel while the flag outputs are connected together with AND or OR gates. In theory, both FIFOs must have the same internal state and, accordingly, signal-identical flags; however, when there is unfavorable overlapping, the flag of one device can change one clock cycle later than the other device. This does not cause differences in the contents of memory or loss of data. The flag synchronization can decide on a clock-pulse edge sooner or later, resulting in differences in the display. In this case, the connection with AND or OR gates ensures reliable results.

If an 18-bit access is desired with an extension of word width, this can be achieved as shown in Figure 12. The only difference, in this case, is that both FIFOs are programmed for 9-bit access and only nine data lines per FIFO (D8–D0 and Q8–Q0) are used.



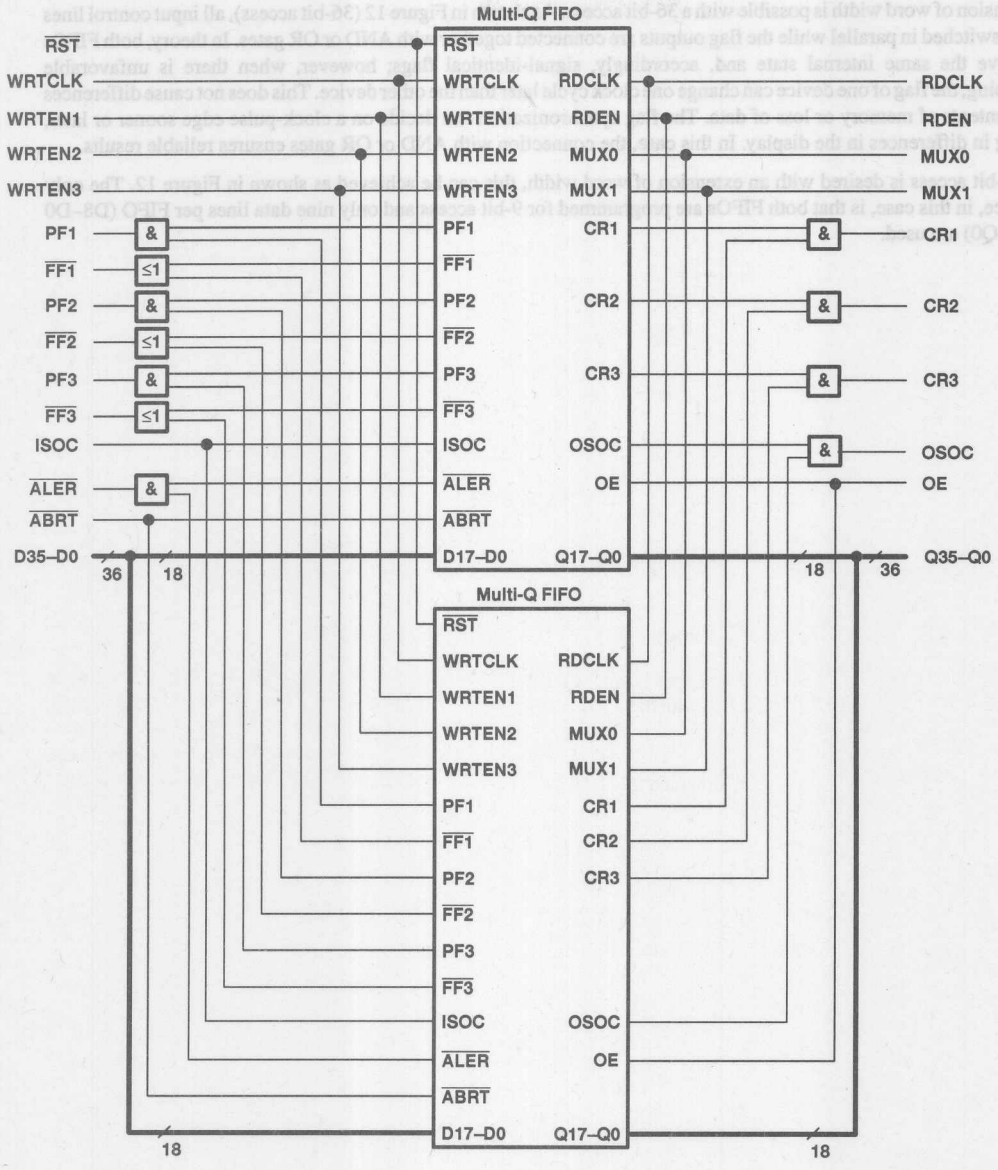


Figure 12. Extension of Word Width With 18-Bit or 36-Bit Input and/or Output Data

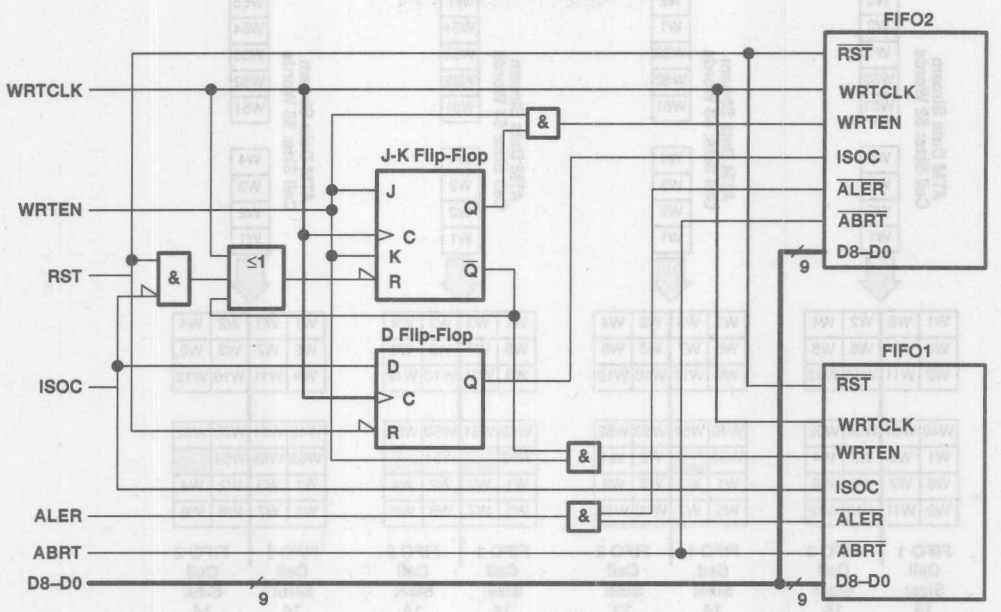
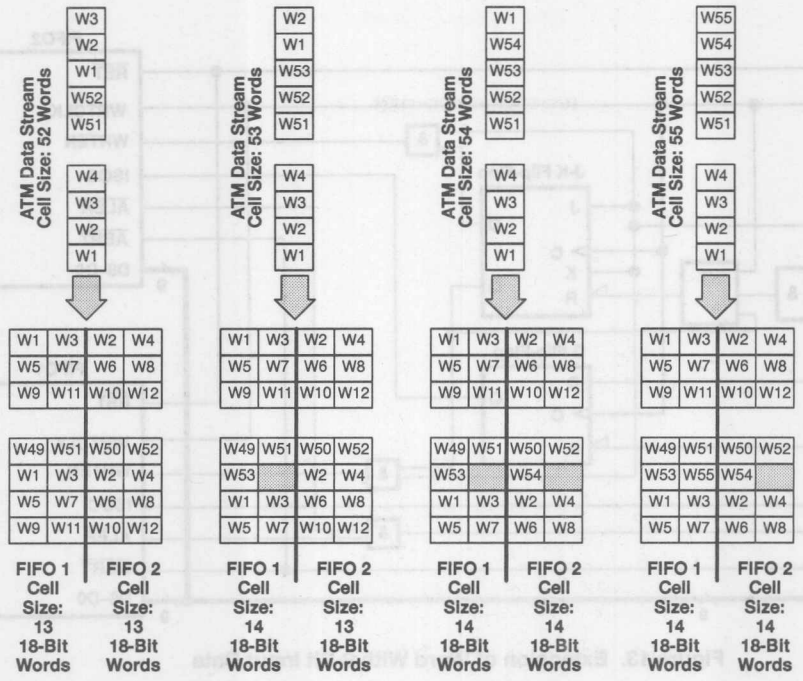


Figure 13. Extension of Word With 9-Bit Input Data

If a 9-bit access to two Multi-Q FIFOs having extended word width is desired, these devices must be provided with external logic to control them in accordance with the ping-pong principle. In Figure 13, WRTEN and ISOC control lines demonstrate the ping-pong principle; i.e., the first 9-bit word is read into FIFO1 and the second 9-bit word is read into FIFO2. In this case, ISOC must also be generated for the second 9-bit data word, because this data word represents the beginning of a cell of FIFO2. The order in which the 9-bit words are read into the two FIFOs is shown in Figure 14.



NOTE A: Two Multi-Q FIFOs are connected as a 36-bit-wide FIFO with 9-bit data access.

Figure 14. Data Flow of an ATM Data Stream in Two Multi-Q FIFOs

Programming Examples

Before use, the Multi-Q FIFO must be reset and programmed to perform the desired function using the configuration registers (see Table 2). Table 6, Table 7, and Table 8 show examples of register programming.

Table 6. Example of Configuration Registers Programming: 18-Bit Write, 18-Bit Read

Function:	Cell size: 53 bytes → 27 18-bit words Write access: 18 bit Read access: 18 bit Size of Queue 1: 75 ATM cells → 2048 18-bit words Size of Queue 2: 56 ATM cells → 1536 18-bit words Size of Queue 3: 18 ATM cells → 512 18-bit words PF1_W: 65 ATM cells PF1_R: 55 ATM cells PF2_W: 50 ATM cells PF2_R: 40 ATM cells PF3_W: 15 ATM cells PF3_R: 10 ATM cells									
REGISTER	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**	**HEX**	**DESCRIPTION**
PORT	0	0	0	0	0	0	0	0	00	P0 = 0 → 18-bit input bus P3 = 0 → 18-bit output bus
QL1	0	0	0	0	1	0	0	0	08	8 × 256 = 2048 18-bit words
QL2	0	0	0	0	0	1	1	0	06	6 × 256 = 1536 18-bit words
CLSZ	0	0	0	1	1	0	1	1	1B	53 cells → 27 18-bit words
PF1_W	0	1	0	0	0	0	0	1	41	65 ATM cells
PF1_R	0	0	1	1	0	1	1	1	37	55 ATM cells
PF2_W	0	0	1	1	0	0	1	0	32	50 ATM cells
PF2_R	0	0	1	0	1	0	0	0	28	40 ATM cells
PF3_W	0	0	0	0	1	1	1	1	0F	15 ATM cells
PF3_R	0	0	0	0	1	0	1	0	A	10 ATM cells

Table 7. Example of Configuration Registers Programming: 9-Bit Write, 18-Bit Read

Function:	Cell size: 53 bytes → 27 18-bit words Write access: 9 bit, little endian Read access: 18 bit Size of Queue 1: 66 ATM cells → 1792 18-bit words Size of Queue 2: 56 ATM cells → 1536 18-bit words Size of Queue 3: 28 ATM cells → 768 18-bit words PF1_W: 60 ATM cells PF1_R: 50 ATM cells PF2_W: 50 ATM cells PF2_R: 40 ATM cells PF3_W: 24 ATM cells PF3_R: 16 ATM cells									
REGISTER	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**	**HEX**	**DESCRIPTION**
PORT	0	0	0	0	0	1	0	1	00	P0 = 1 → 9-bit input bus P1 = 0 → little endian P2 = 1 → odd-numbered cell size P3 = 0 → 18-bit output bus
QL1	0	0	0	0	0	1	1	1	07	7 × 256 = 1792 18-bit words
QL2	0	0	0	0	0	1	1	0	06	6 × 256 = 1536 18-bit words
CLSZ	0	0	0	1	1	0	1	1	1B	53 cells → 27 18-bit words
PF1_W	0	0	1	1	1	1	0	0	3C	60 ATM cells
PF1_R	0	0	1	1	0	0	1	0	32	50 ATM cells
PF2_W	0	0	1	1	0	0	1	0	32	50 ATM cells
PF2_R	0	0	1	0	1	0	0	0	28	40 ATM cells
PF3_W	0	0	0	1	1	0	0	0	18	24 ATM cells
PF3_R	0	0	0	1	0	0	0	0	10	16 ATM cells

Table 8. Example of Configuration Registers Programming: 18-Bit Write, 9-Bit Read

Function:	Cell size: 54 bytes → 27 18-bit words Write access: 18 bit Read access: 9 bit Size of Queue 1: 56 ATM cells → 1536 18-bit words Size of Queue 2: 56 ATM cells → 1536 18-bit words Size of Queue 3: 37 ATM cells → 1024 18-bit words PF1_W: 50 ATM cells PF1_R: 40 ATM cells PF2_W: 50 ATM cells PF2_R: 40 ATM cells PF3_W: 30 ATM cells PF3_R: 20 ATM cells									
Register	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**	**HEX**	**Description**
PORT	0	0	0	0	1	0	0	0	00	P0 = 0 → 18-bit input bus P3 = 1 → 9-bit output bus P4 = 0 → even-numbered cell size
QL1	0	0	0	0	0	1	1	0	07	6 × 256 = 1536 18-bit words
QL2	0	0	0	0	0	1	1	0	06	6 × 256 = 1536 18-bit words
CLSZ	0	0	0	1	1	0	1	1	1B	54 cells → 27 18-bit words
PF1_W	0	0	1	1	0	0	1	0	32	50 ATM cells
PF1_R	0	0	1	0	1	0	0	0	28	40 ATM cells
PF2_W	0	0	1	1	0	0	1	0	32	50 ATM cells
PF2_R	0	0	1	0	1	0	0	0	28	40 ATM cells
PF3_W	0	0	0	1	1	1	1	0	1E	30 ATM cells
PF3_R	0	0	0	1	0	1	0	0	14	20 ATM cells

Applications

The Multi-Q FIFO provides several alternatives for arranging the priority control of various QOS classes. A common implementation is the priority control in the receiving unit (see Figure 15) and transmitting unit (see Figure 16) of an ATM exchange. If the content of the transmitted ATM cells in the receiving unit is larger than the capacity of the switching matrix, a priority control must be installed and cells of less importance put in a waiting queue or eliminated completely. The same phenomenon can arise with the transmitting unit when the capacity of the outgoing line cannot accept the cells received from the switching matrix. In both cases, use of a Multi-Q FIFO is recommended.

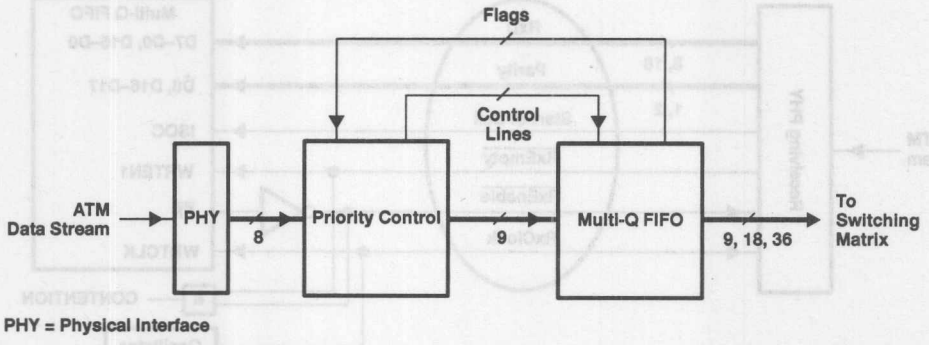


Figure 15. ATM-Exchange Receiving Unit

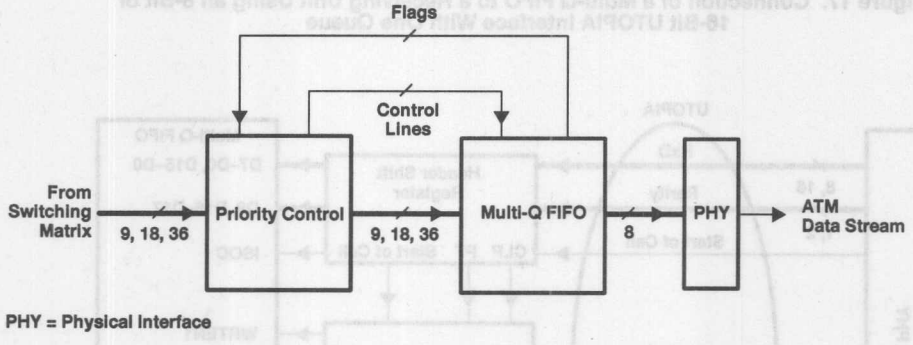


Figure 16. ATM-Exchange Transmitting Unit

The universal test and operations physical interface to ATM (UTOPIA) in 8-bit and 16-bit bus widths has become the preferred interface between the physical interface (PHY) and the subsequent or preceding stages. Figure 17 shows the connection of the Multi-Q FIFO on the receiving side to a PHY with a UTOPIA interface when one queue is used. When priority control of the ATM cells is implemented, an arrangement as shown in Figure 18 can be used. Similarly, the connection on the transmitting side to a PHY with a UTOPIA interface can be implemented as shown in Figure 19 and Figure 20.

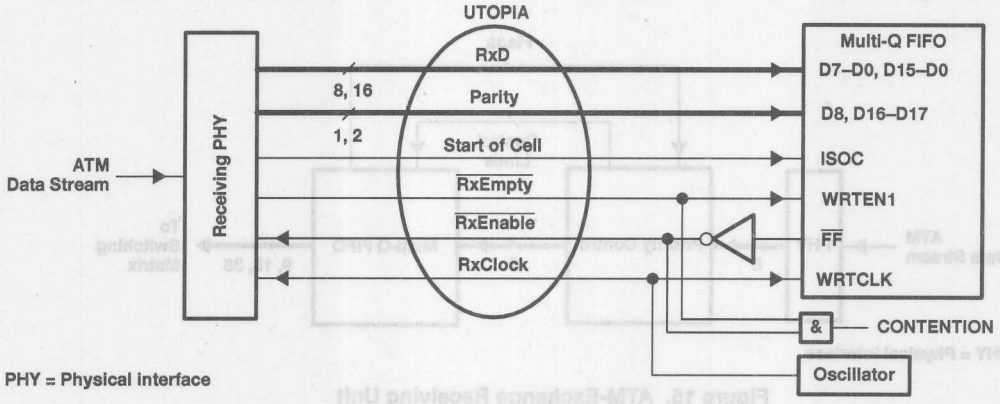


Figure 17. Connection of a Multi-Q FIFO to a Receiving Unit Using an 8-Bit or 16-Bit UTOPIA Interface With One Queue

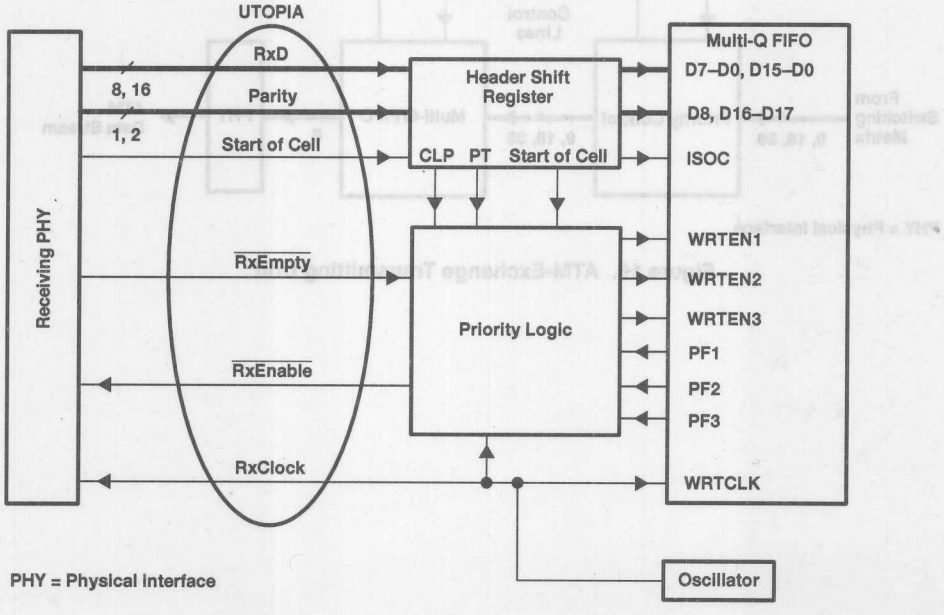


Figure 18. Priority-Controlled Connection of a Multi-Q FIFO to a Receiving Unit Using an 8-Bit or 16-Bit UTOPIA Interface

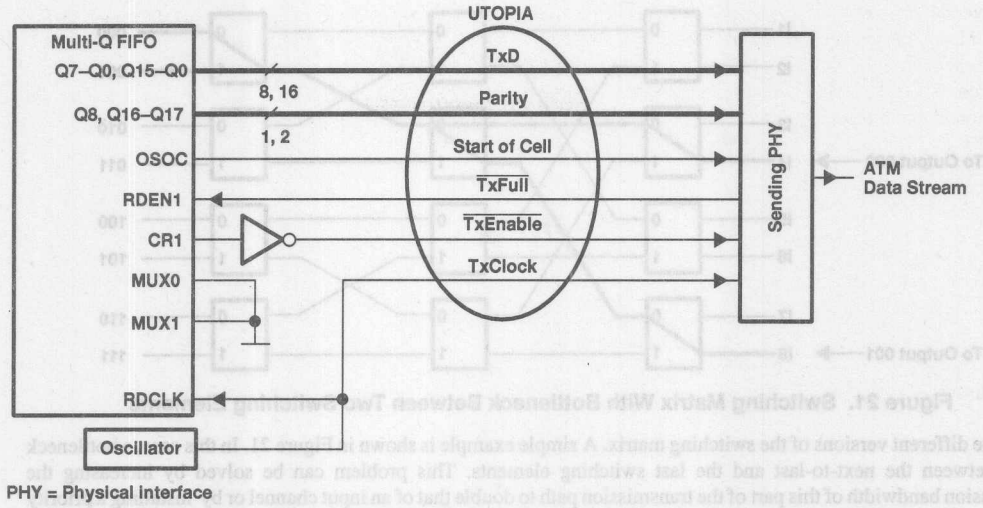


Figure 19. Connection of a Multi-Q FIFO to a Transmitting Unit Using an 8-Bit or 16-Bit UTOPIA Interface With One Queue

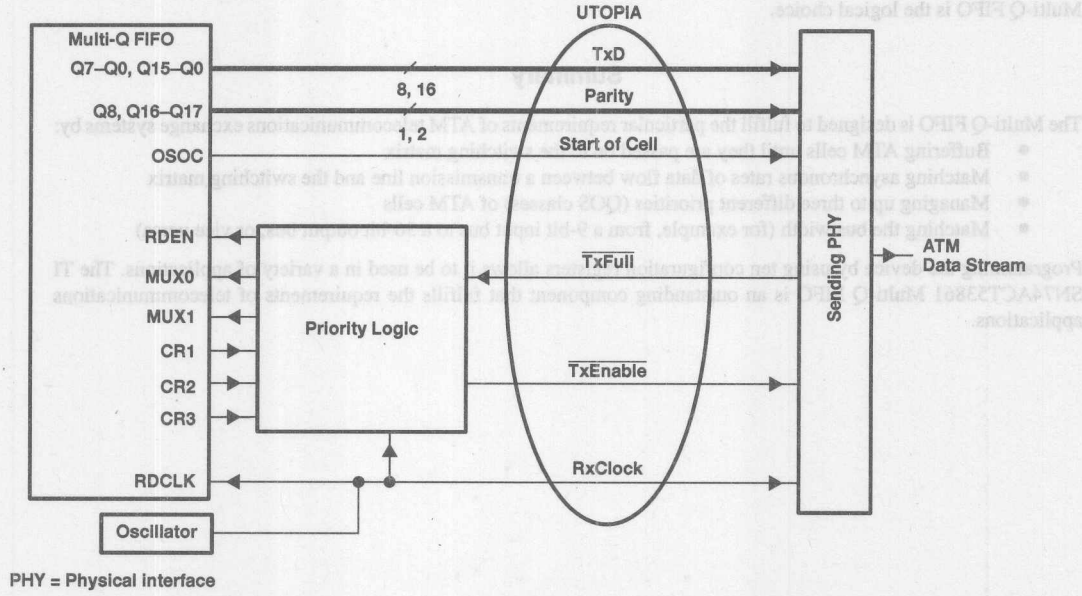


Figure 20. Priority-Controlled Connection of a Multi-Q FIFO to a Transmitting Unit Using an 8-Bit or 16-Bit UTOPIA Interface

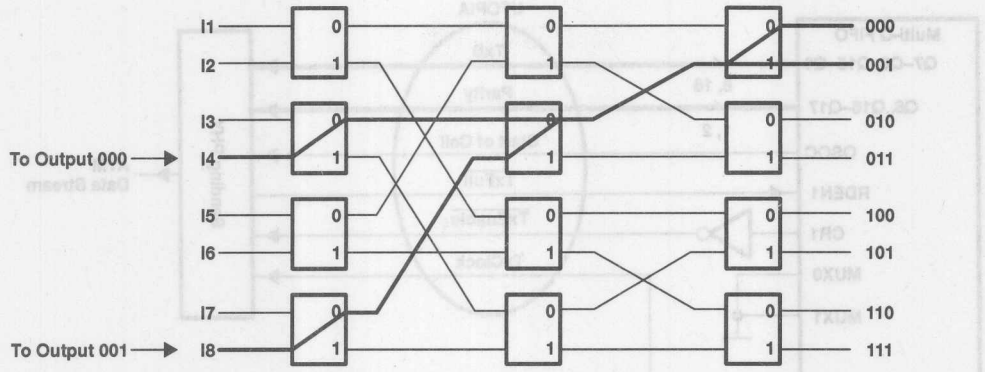


Figure 21. Switching Matrix With Bottleneck Between Two Switching Elements

There are different versions of the switching matrix. A simple example is shown in Figure 21. In this case, a bottleneck arises between the next-to-last and the last switching elements. This problem can be solved by increasing the transmission bandwidth of this part of the transmission path to double that of an input channel or by installing a priority control for the ATM cells to be transmitted. A Multi-Q FIFO is a suitable device for implementing this priority control.

In view of the many ways in which an ATM exchange system can be implemented, there are certainly a large number of potential applications for the Multi-Q FIFO. When the priority control of up to three QOS classes is required, the Multi-Q FIFO is the logical choice.

Summary

The Multi-Q FIFO is designed to fulfill the particular requirements of ATM telecommunications exchange systems by:

- Buffering ATM cells until they are passed on to the switching matrix
- Matching asynchronous rates of data flow between a transmission line and the switching matrix
- Managing up to three different priorities (QOS classes) of ATM cells
- Matching the bus width (for example, from a 9-bit input bus to a 36-bit output bus, or vice versa)

Programming the device by using ten configuration registers allows it to be used in a variety of applications. The TI SN74ACT53861 Multi-Q FIFO is an outstanding component that fulfills the requirements of telecommunications applications.

Interfacing TI Clocked FIFOs With TI Floating-Point Digital Signal Processors

First-In, First-Out Technology



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Introduction

Digital signal processors (DSPs) are used in a variety of applications to analyze real-time data or speed computationally intensive tasks. A DSP is a microprocessor tuned to the task of number crunching by an instruction set that conveniently ties together special hardware components needed for fast floating-point and fixed-point math and by powerful input/output (I/O) functions that keep data flowing quickly. Design of the I/O for a digital-signal-processing system is one of the major factors that dictates the machine's performance. First-in, first-out (FIFO) memories often are used as data rate buffers to optimize the throughput of digital-signal-processing systems and increase overall performance.

A FIFO is a dual-port memory with built-in write and read addressing to pass out data in the same order it is written. Data reads and writes can be done asynchronous to one another. Flag circuitry indicates when the queue is empty or full, preventing simultaneous read/write access to the same memory location. Advanced FIFO memories from Texas Instruments (TI) produced in CMOS or BiCMOS technology also have user-programmable almost-empty and almost-full flags to measure the number of words in memory. FIFOs provide a seamless bridge between two buses operating at different clock speeds and acting as temporary data bins to exchange information between two systems without handshaking delay.

TI's TMS320C3x and TMS320C4x processors are popular DSPs that include a 40-/32-bit floating-/fixed-point math unit, one or two 32-bit external buses, and an on-board direct-memory-access (DMA) controller. Unidirectional and bidirectional clocked FIFO devices from TI frequently are used to support systems built around these processors. Attractive features offered by TI clocked FIFOs are synchronous (clocked) interface on each port, asynchronous I/O capability, programmable flags, maximum write/read frequencies up to 80 MHz, maximum read access times as low as 9 ns, and fine-pitch surface-mount packaging.

DSP Applications Using FIFOs

DSP systems doing real-time data analysis or control functions use analog-to-digital (A/D) converters to translate continuous-time, real-valued signals into discrete-time, integer-valued sequences. The rate used to sample the analog signal is chosen based on the frequency bandwidth of the signal. This sample rate is independent of the microprocessor-bus rate, and asynchronous buffering is required to pass the information to the DSP. Serial ports on the TMS320C3x/C4x processors provide an asynchronous interface with A/D converters and are adequate when the incoming data traffic has a relatively low bit rate. For higher bit rates, unidirectional clocked FIFOs provide a parallel buffer between the converters and the DSP bus.

Figure 1 shows several digitized signals, each using a FIFO for rate buffering to the processor bus. An example of this application is multiplexing several analog telephone lines for compression or symbol detection. An input signal packet is gathered in the FIFO and burst into memory by the DMA unit on the TMS320C3x/C4x. This method also is useful when the analog data is sampled at a high rate for short duration, as in some medical-imaging equipment. Each FIFO holds its A/D samples in queue until the processor retrieves the information that must be completed before the next sampling period. The block labeled FIFO Enable can have a single-memory-space address and control the FIFOs in round-robin fashion as the DMA fills the random-access memory (RAM) with digitized signals.

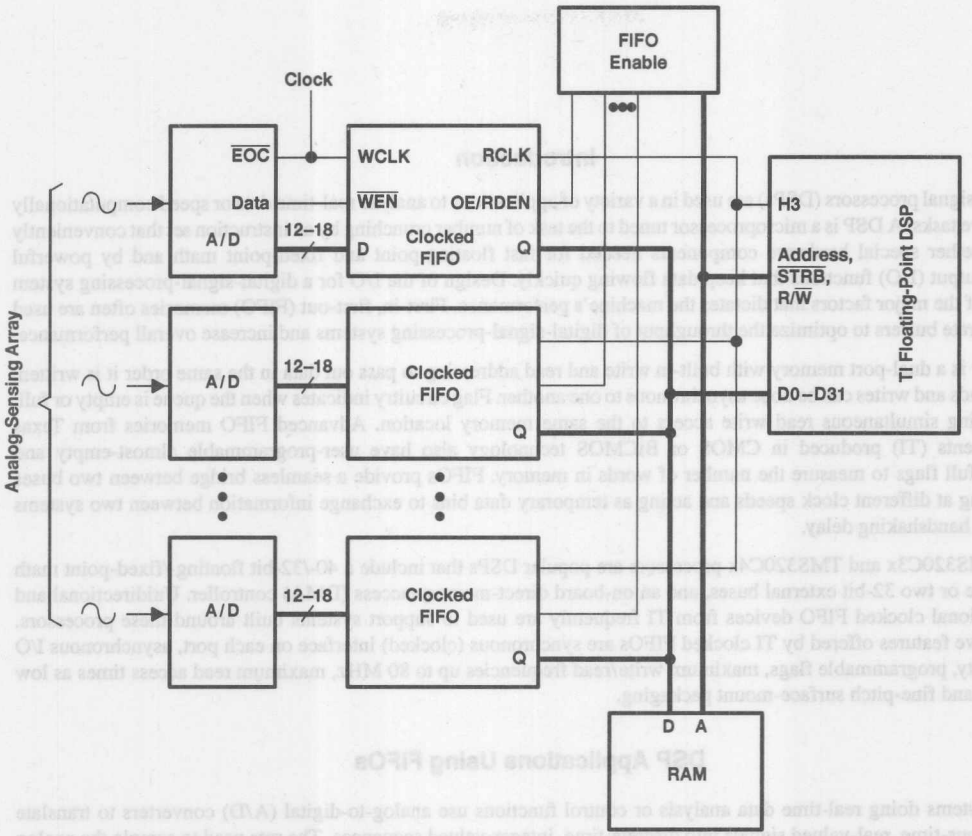


Figure 1. Clocked FIFOs Used for High-Speed Data Acquisition

DSP algorithms are drawn as functional boxes with interconnecting lines representing data streams. This concept can translate directly to a hardware organization as shown in the pipelined image-processing system (see Figure 2), wherein the unidirectional TI clocked FIFOs provide the data connection between the TI floating-point DSPs. The FIFO that connects the bus to the first processing element (PE) performs the task of rate matching, as the bus generally operates at a slower rate than the DSP bus. FIFOs that connect adjacent PEs are used as packet builders; that is, a packet of data is stored and then detected with the use of the almost-full/almost-empty or half-full flags and read by the next processor. Transferring a known packet size simplifies DMA control. The FIFO interconnect between PEs eliminates the need for processor interlock protocols and reduces clock-distribution requirements by allowing each PE to utilize its own independent clock.

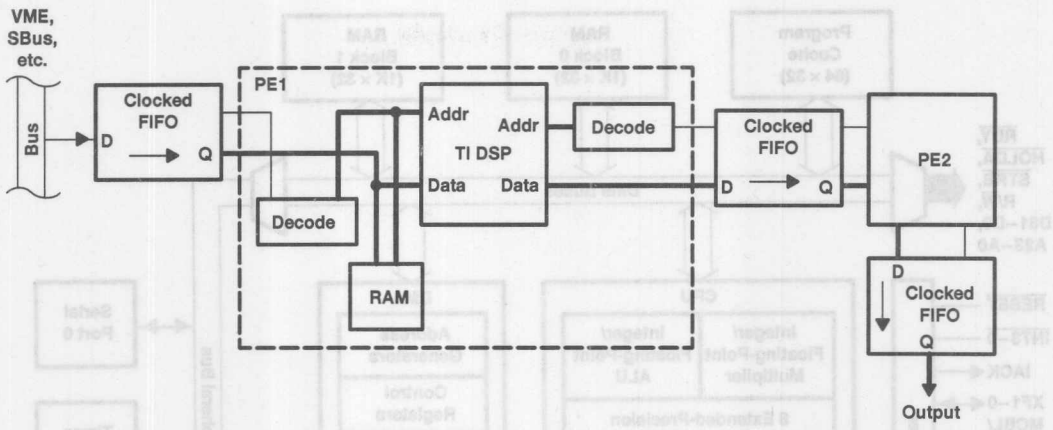


Figure 2. Clocked FIFOs Used in Pipelined Image-Processing Systems

Software applications often are written for a general-purpose workstation platform, incorporating signal-processing functions that are not efficiently performed by the workstation. A solution to this problem is to use a special-purpose DSP system as a coprocessor for the application and communicate with the host computer via a local or backplane bus (see Figure 3). The bidirectional clocked FIFO is most useful when data traffic is heavy both to and from the host computer, such as when the host provides the input data and receives the processed results. Bidirectional FIFOs also can be used as instruction queues between a host processor and the DSP. The FIFO in the datapath provides clock partitioning so each bus can operate at its maximum rate; it also eliminates transfer delay required for a bus request to be granted to either the host or the DSP.

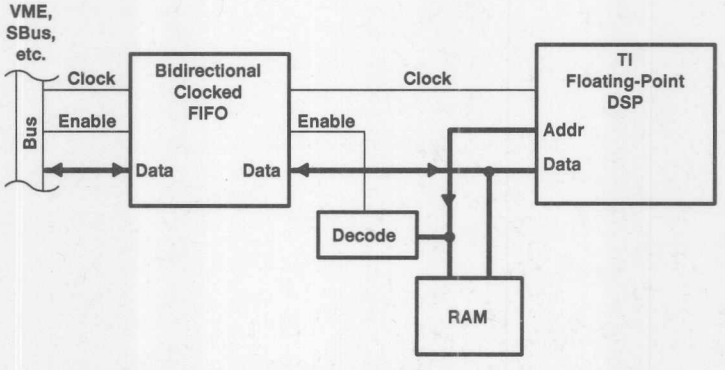


Figure 3. Bidirectional Clocked FIFO Used for Bus-Speed Matching

Communication Between a TI Bidirectional Clocked FIFO and a TI Floating-Point DSP

An interface between a TI floating-point DSP and a TI clocked FIFO was created as an example of FIFO memory mapping, DMA considerations, flag-offset programming, and bus-cycle control. The processor chosen for the example was the TMS320C31-40 (see Figure 4) since its functions and terminals are a subset of the TMS320C30 and comparable to the TMS320C40. The FIFO chosen was the SN74ACT3632, which is a bidirectional device that contains two 512-word by 36-bit FIFOs to buffer data in opposite directions (see Figure 5). A single SN74ACT3632 device in either a 132-pin quad flat package or 120-pin thin quad flat package provides a 32-bit bidirectional datapath. The clocked architecture of the FIFO simplifies the interface by directly using many of the DSP bus-control signals. The bidirectional function provides both data read and write examples.

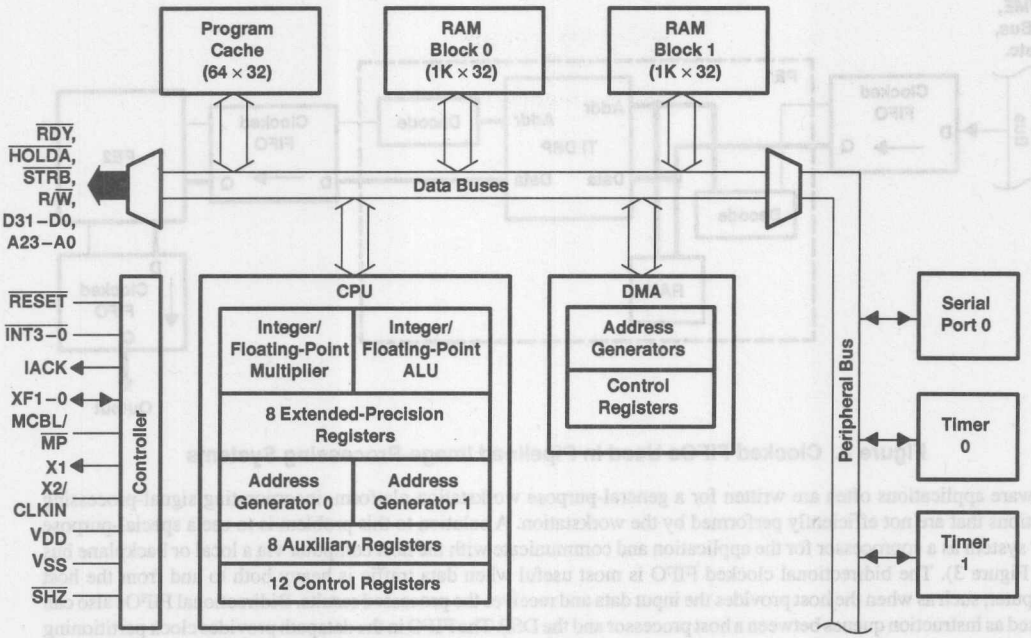


Figure 4. TMS320C31 DSP

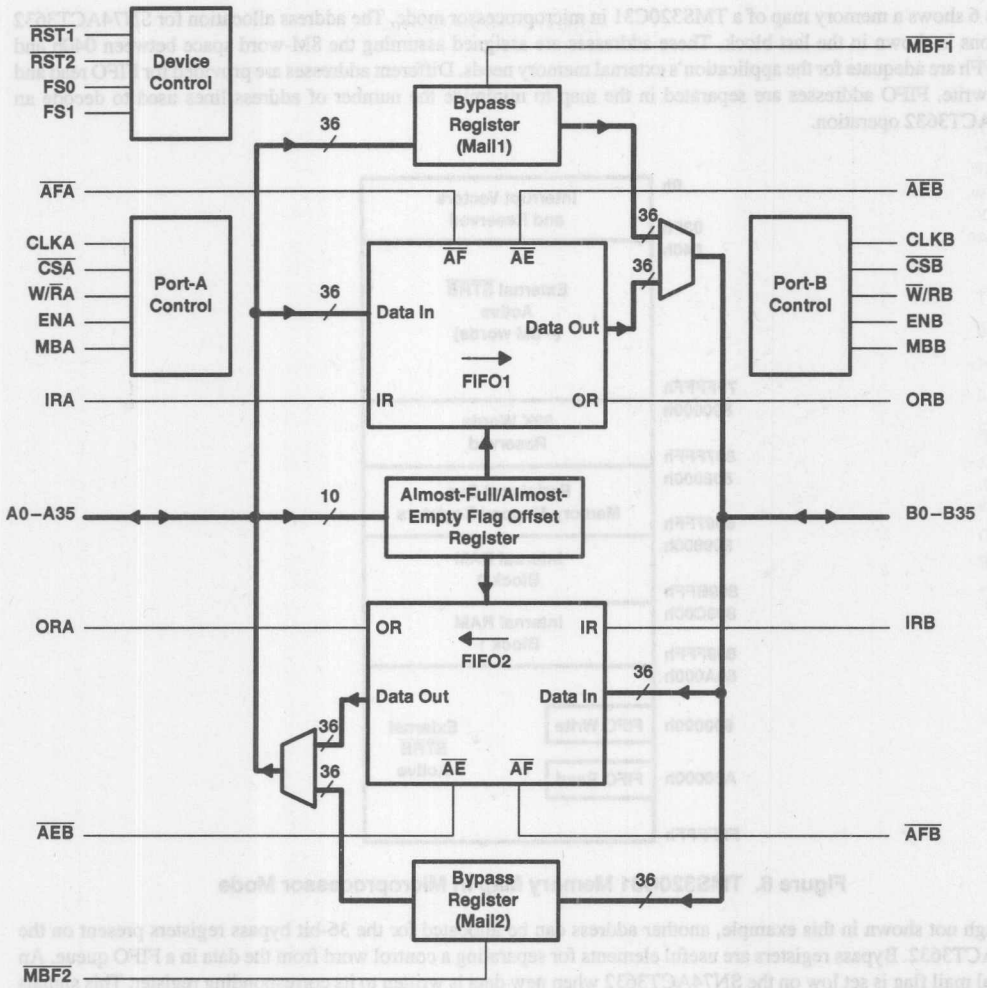


Figure 5. SN74ACT3632 512 × 36 × 2 Bidirectional FIFO

Figure 6 shows a memory map of a TMS320C31 in microprocessor mode. The address allocation for SN74ACT3632 functions is shown in the last block. These addresses are assigned assuming the 8M-word space between 040h and 7FFFFFh are adequate for the application's external memory needs. Different addresses are provided for FIFO read and FIFO write. FIFO addresses are separated in the map to minimize the number of address lines used to decode an SN74ACT3632 operation.

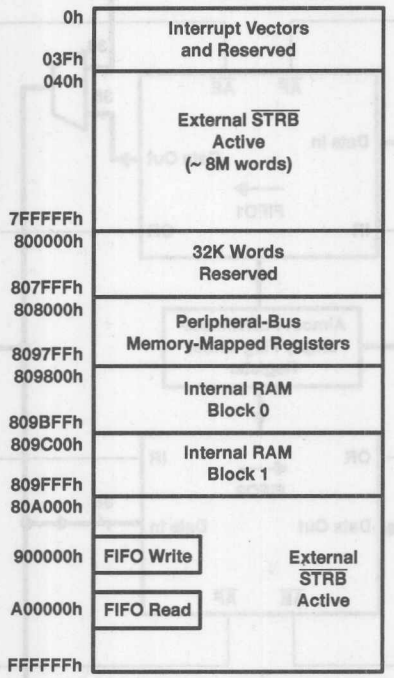


Figure 6. TMS320C31 Memory Map in Microprocessor Mode

Although not shown in this example, another address can be allocated for the 36-bit bypass registers present on the SN74ACT3632. Bypass registers are useful elements for separating a control word from the data in a FIFO queue. An external mail flag is set low on the SN74ACT3632 when new data is written to its corresponding register. This signals the receiving bus of an available control word, and the external mail flag is set high when the bypass register is read. One use of the bypass registers is to pass packet-size information between the SN74ACT3632 ports for DMA initialization.

The FIFO addresses in the memory map are accessible by the processor's DMA or through single-word load and store instructions. DMA transfer is the preferred method for moving large blocks of data. Instead of using the CPU for each single-word transfer, a small DMA setup overhead is needed to initialize the transfer of several words. The DMA becomes a bus master and performs the block transfer while the CPU is not using the external bus. This frees the CPU to accomplish its primary task of floating-point and fixed-point mathematical operations.

DMA Considerations

The DMA processor gives the user flexibility in designing the FIFO data flow control. The transfer counter that initializes the DMA for the number of transfers is decremented after each transfer is complete. Once the transfer counter reaches zero, transfers can be stopped and an interrupt can be sent to the CPU. Each DMA transfer can be synchronized to the source, synchronized to the destination, or synchronized to both the source and destination for a transfer by using the DSP interrupts. The user also can choose to increment or decrement the source and destination addresses after each transfer. These flexible features create several decisions to be made by the designer.

The method used to initiate the DMA for a FIFO transfer also introduces several considerations. One method is to schedule a FIFO write or read in software, where the DMA is initiated at a particular point in the program. This is the simplest method, but requires the most knowledge about the data-transfer characteristics (e.g., knowing at what point in the program data is ready to be transferred to or from the FIFO). This often is difficult to assess for FIFO reads when the data is queued asynchronous to the DSP program and is more useful for initiating FIFO writes. DMA synchronization to the SN74ACT3632 using the output-ready (OR) flag of the reading FIFO and the input-ready (IR) flag of the writing FIFO prevents reading from an empty FIFO or writing to a full FIFO. DMA synchronization is needed in this instance, since a read or write to a FIFO that is not ready results in multiple wait states on the DSP bus until the FIFO is ready for the specific transfer. Furthermore, DMA synchronization eliminates the need for generating a TMS320C31 ready ($\overline{\text{RDY}}$) signal based on the FIFO flags. This is a great benefit due to the small address valid to $\overline{\text{RDY}}$ maximum delay specification that must be met for zero-wait-state operation.

Another method to schedule a DMA operation is through hardware by using the programmable almost-full and almost-empty flags available on the SN74ACT3632. These flags can be used to interrupt the DSP when a data packet is available for transfer (or when space is available to receive a packet transfer). This can be done with fixed packet sizes or packets of variable length. For a fixed packet length, the programmable FIFO flags are set to show when the FIFO is ready to transmit or receive an entire packet of data. The DMA is then set for a transfer length equal to the packet size. This eliminates the need for source/destination synchronization, while ensuring reads are not attempted from an empty FIFO nor writes attempted to a full FIFO.

Hardware scheduling of a DMA operation using variable packet lengths generally needs to use DMA synchronization for controlling the FIFO. The SN74ACT3632 almost-full and almost-empty flags can be programmed to indicate when a portion of the packet in the receiving FIFO has been stored or when a portion of the packet space is available in the transmitting FIFO. DMA synchronization to the SN74ACT3632 with the IR and OR flags prevents FIFO overflow and underflow. The additional hardware required to support this method includes either four TMS320C31 interrupt lines ($\overline{\text{IRQn}}$) or an external device that combines the function of two or more interrupt lines into a single interrupt line.

Example Control of the SN74ACT3632 Using the DMA

The following example illustrates the use of the SN74ACT3632 FIFO to channel data between a TMS320C31 DSP and a generic local or backplane bus. The emphasis of the example is on the DSP-to-FIFO interface hardware and software. Data transfers to and from the DSP are in fixed packet sizes. This requirement results in minimal hardware complexity and a slight increase in software complexity. The higher software complexity required to divide a large data transfer in the fixed-length packets and track the number of packets delivered or received.

Data to be received by the DSP is put in the FIFO asynchronous to the DSP program execution; therefore, a hardware-scheduling mechanism is used to initiate the DMA to read data from the SN74ACT3632. DMA writes to the FIFO are scheduled in software.

Figure 7 shows the flow chart for controlling FIFO reads. FIFO reads are scheduled with hardware using packet-detecting interrupts generated by the almost-empty flag of a receiving FIFO. A combination of enabling the interrupt and polling its status initiates FIFO reads. The enabled interrupt initiates the first packet transfer after a FIFO empty condition, and interrupt polling handles transfers when multiple packets are stored in the FIFO. The read transfers are fixed in packet size and require no DMA synchronization. CPU interrupts from the FIFO almost-empty flag are disabled at the first of the routine and are not enabled at the end of the routine. Before a DMA operation is initiated, the interrupt routine checks if the DMA transfer counter (TCOUNT) is zero to avoid interfering with any concurrent DMA operation. If the DMA is being used, the destination address is written to a read schedule table and the routine terminates. If the TCOUNT value is zero, a DMA sequence is initiated to move the data packet from the FIFO to processor memory. An additional algorithm, such as concatenating a number of blocks together, manages the memory placement of the incoming data block.

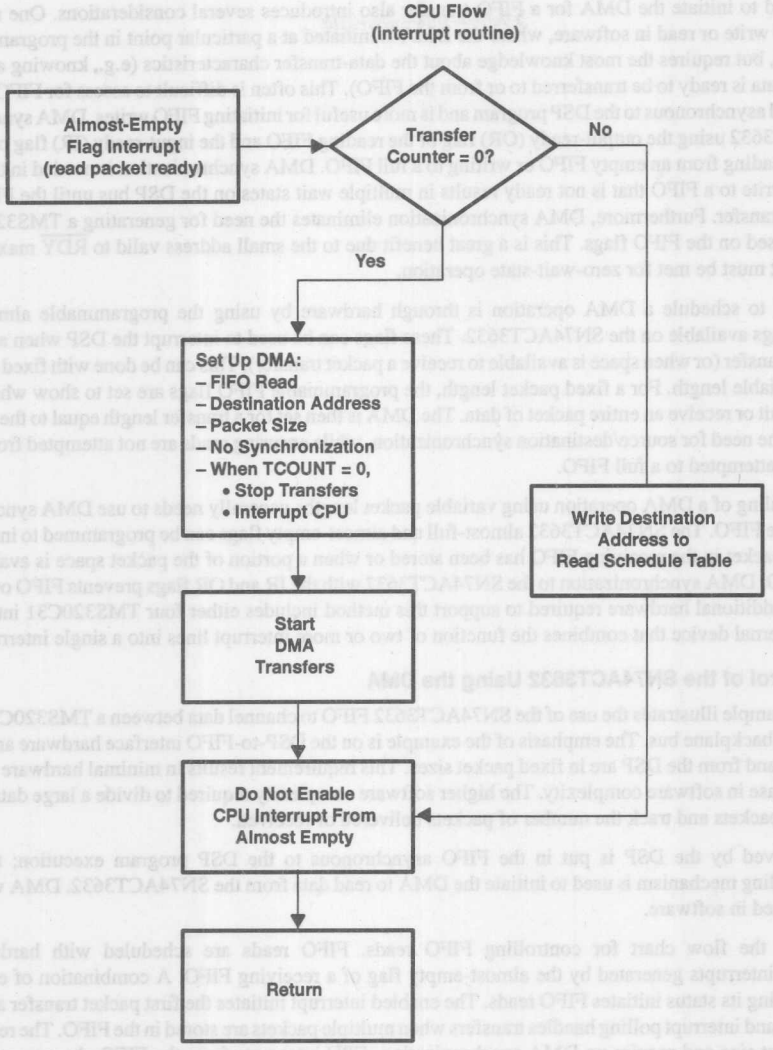


Figure 7. Routine for Almost-Empty Flag CPU Interrupt to Schedule FIFO Reads

The read schedule table comprises two memory locations, organized as a stack. The bottom of the stack is an arbitrary null pointer that indicates an empty table on top of the stack. Only one schedule location is needed since the interrupt from the receiving FIFO indicates the presence of a singular packet. When the interrupt routine finds the DMA in use, the beginning DMA destination address is pushed on top of the stack. This buffered information can be used at the end of the current DMA operation to initiate a new sequence.

Figure 8 shows an example flow chart for controlling FIFO writes. FIFO writes are scheduled in software by polling the almost-full flag of the transmit buffer on the SN74ACT3632. Packet sizes are assumed fixed in length to mirror the FIFO read operation and eliminate the need for DMA destination synchronization. The source address is written to a write schedule table if either the almost-full flag indicates adequate space is not available for a block write or if the DMA is in use. This write schedule table is a circular buffer with two memory pointers indicating the head and the tail of the buffer. To schedule a write to the FIFO, the beginning source address is written to the buffer and the write pointer is incremented.

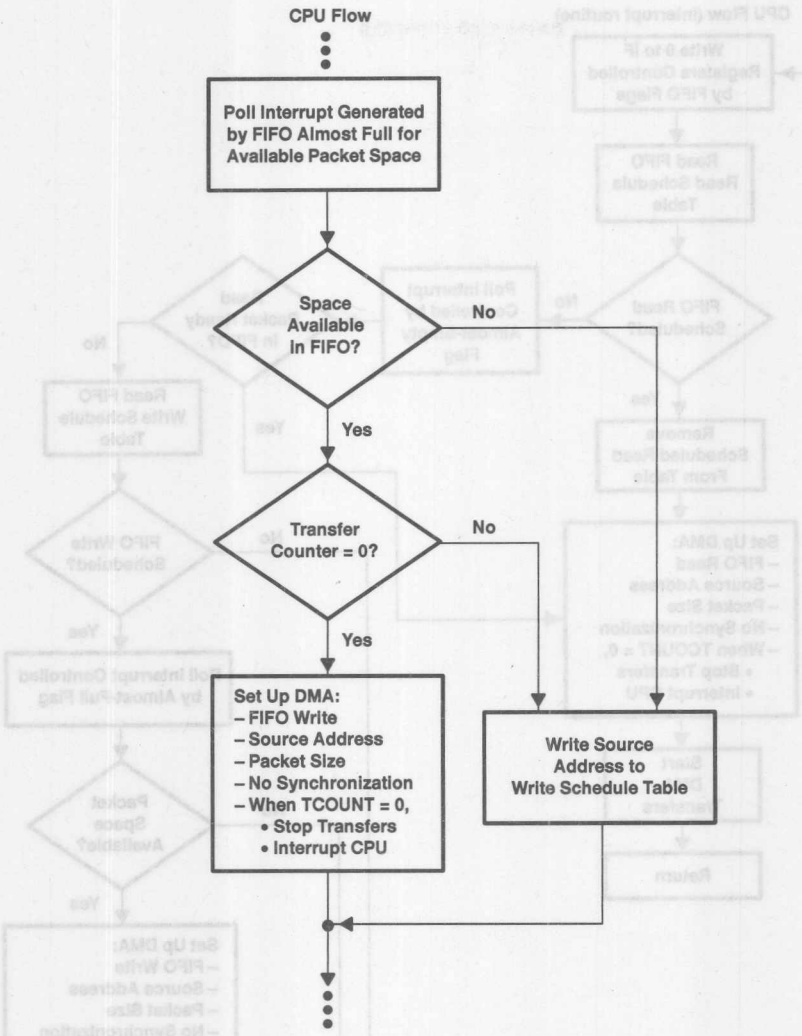


Figure 8. Scheduling FIFO Writes

For both FIFO writes and FIFO reads, no destination or source synchronization is used since the block sizes are known and packet-detecting mechanisms are used. The DMA transfer counter is loaded with the block size and the DMA global control is programmed to stop transfers and interrupt the CPU when the counter is zero. When writing to the FIFO from memory, the source address is incremented or decremented after each transfer and the destination address is not changed. The converse is true for reading FIFO data and placing the block in memory.

Figure 9 shows a flow chart of the interrupt routine initiated when the transfer counter reaches zero. Scheduled FIFO reads have priority over FIFO writes in the program, but scheduled FIFO writes can take precedence. The internal TMS320C31 interrupt-flag (IF) bits controlled by the FIFO flags are cleared at the beginning of the routine. This ensures a disabled interrupt is reflected by its IF status if the preceding DMA transfer sequence resulted in disabling one of the external interrupt lines.

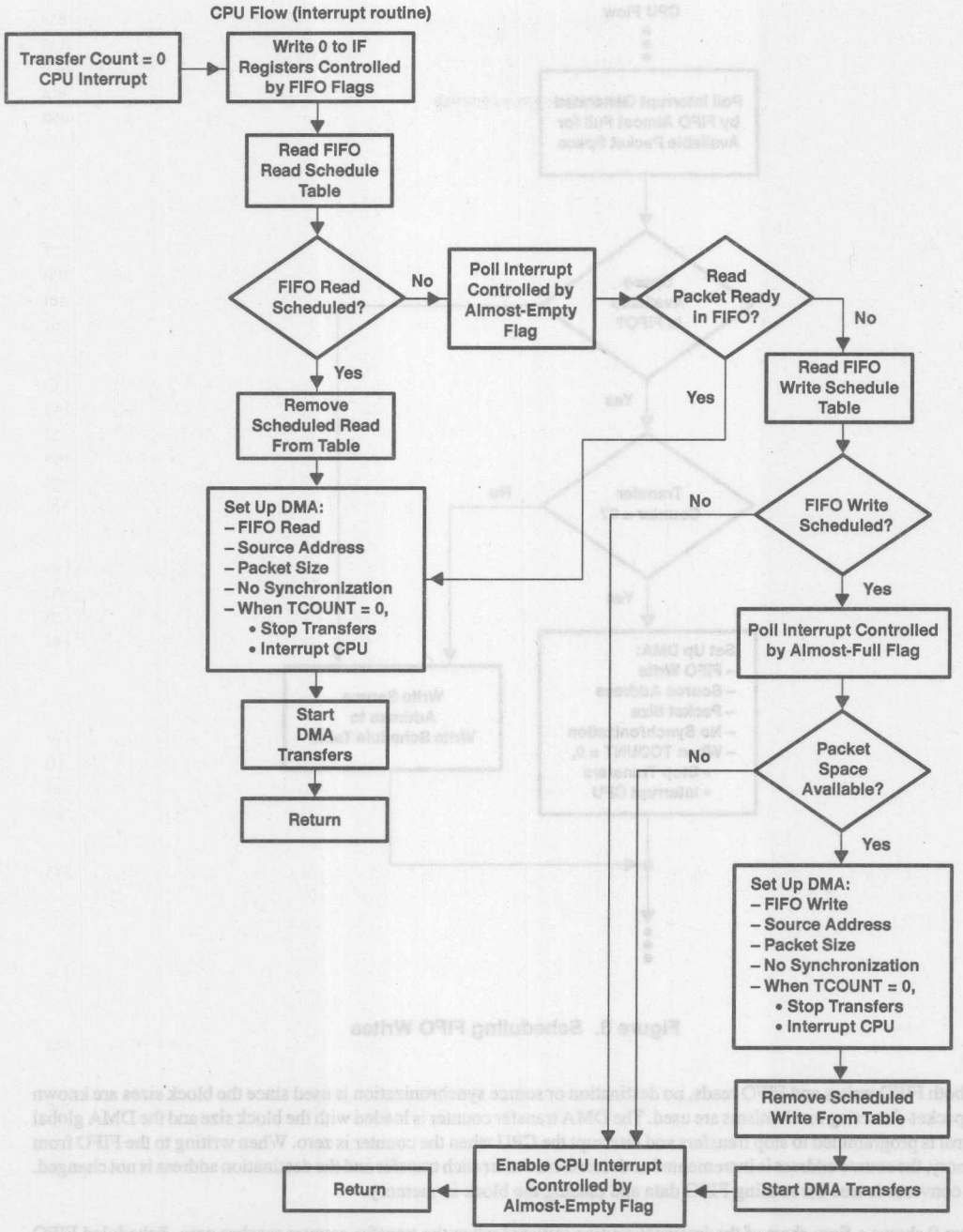


Figure 9. Routine for DMA Interrupt to CPU When Transfer Counter Reaches Zero

When FIFO writes or reads are scheduled in a table, a DMA sequence is started using the source or destination address found in the table. The almost-empty flag of the receiving FIFO is polled if there are no scheduled reads, and a read is started if a packet is present. The almost-full flag of the transmitting FIFO is polled before starting a DMA sequence writing the FIFO to ensure sufficient space is allocated for the transfer. If there are no scheduled FIFO reads and a data packet is not ready for transmission, the CPU interrupt generated by the almost-empty flag is enabled to use hardware-driven scheduling of FIFO reads.

Programming the FIFO Almost-Full-Flag and Almost-Empty-Flag Offsets

The SN74ACT3632 flexible flag-programming scheme aids the designer in creating a custom packet size. A choice of three hardware-coded values can be selected during reset or the offsets can be programmed by the user. Two SN74ACT3632 flag-select pins (FS0, FS1) are tied low to put the device in the user-programmable mode. After a reset with FS0 and FS1 low, the first four data writes to FIFO1 from port A of the device load offset values for the four almost-full and almost-empty flags of the device.

Port A of the SN74ACT3632 is connected to the TMS320C31 bus in this example so that the DSP can choose the FIFO offsets during system initialization. Both FS0 and FS1 on the SN74ACT3632 are tied to ground so that the first four FIFO writes on port A result in programming the almost-full/almost-empty flag offsets. This offset information is not stored in FIFO memory, and the device automatically begins normal operation when the programming is complete. Bypass registers on the SN74ACT3632 enable the DSP to gather flag offset values from the system controlling the opposite port of the FIFO. Flag offset values can be programmed from 1 to 508 by the binary value on SN74ACT3632 bits A0–A8. Input levels on FIFO bits A9–A35 are ignored for flag-offset programming.

A FIFO almost-empty ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$) flag is low when the number of words stored in its buffer is less than or equal to the flag's offset value, and high when the number of stored words exceeds the offset value. A FIFO almost-full ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$) flag is low when the number of empty locations in a FIFO is less than or equal to the flag's offset value and is high when the number of empty locations is greater than the offset value. Flag-offset values are easily selected based on packet size.

Calculating FIFO Flag-Offset Values

In the following example, the port-A almost-empty ($\overline{\text{AEA}}$) flag is used to alert the TMS320C31 of an available packet in FIFO2 and the port-A almost-full ($\overline{\text{AFA}}$) flag signals the processor of an available packet space in FIFO1. Figure 10 shows a method to choose flag-offset values assuming a packet size of 128. Almost-full flag selection is straightforward since the $\overline{\text{AFA}}$ flag is high when offset + 1 or more empty locations are available in FIFO1. The first-word fallthrough characteristic of the SN74ACT3632 must be considered for almost-empty flag offset selection.

First-word fallthrough refers to the method used to send new data to a FIFO output register. New data is read from a FIFO to its output register on a rising edge of the FIFO reading clock when one of these two conditions is true:

A new word is available in memory and the FIFO's output-ready (ORA, ORB) flag is low.

A new word is available in memory, the FIFO's output-ready (ORA, ORB) flag is high, and a FIFO read is selected by the port enables.

A new word is available in a FIFO when at least two low-to-high transitions of the FIFO reading clock have occurred since the word was written to the FIFO.

A word stored in an empty FIFO is automatically shifted to the FIFO output register. This unsolicited read frees one location in FIFO memory; therefore, the almost-empty offset selection must be made with this characteristic in mind. Although the first-word fallthrough seems to complicate the FIFO control, this characteristic is beneficial from the hardware-design standpoint.

FLAG	INDICATION	CHOSEN PACKET SIZE	STORED PACKET SIZE AFTER FIRST-WORD FALLTHROUGH	FLAG OFFSET VALUE
$\overline{AEA}$	High level indicates available packet in FIFO2	128 (P)	127 (P – 1)	126 (P – 2)

a) CHOOSING AN $\overline{AEA}$ OFFSET FOR THE SN74ACT3632

FLAG	INDICATION	CHOSEN PACKET SIZE	FLAG OFFSET VALUE
$\overline{AFA}$	High level indicates available packet space in FIFO1	128 (P)	127 (P – 1)

b) CHOOSING AN $\overline{AFA}$ OFFSET FOR THE SN74ACT3632

Figure 10. Almost-Full-Flag and Almost-Empty-Flag Offset Selection

Hardware Interface

Figure 11 shows the connections necessary to interface an SN74ACT3632-30 FIFO to a TMS320C31-40 DSP. The decode programmable logic device (PLD) is a simple circuit to translate the TMS320C31 address selection into an SN74ACT3632 write or read enable. The FIFO mailbox-select (MBA, MBB) pins are tied to ground in this example, but also can have a unique TMS320C31 address when the bypass registers are needed. Flag-select (FS0, FS1) inputs also are tied to ground to put the SN74ACT3632 in processor-programming mode upon reset.

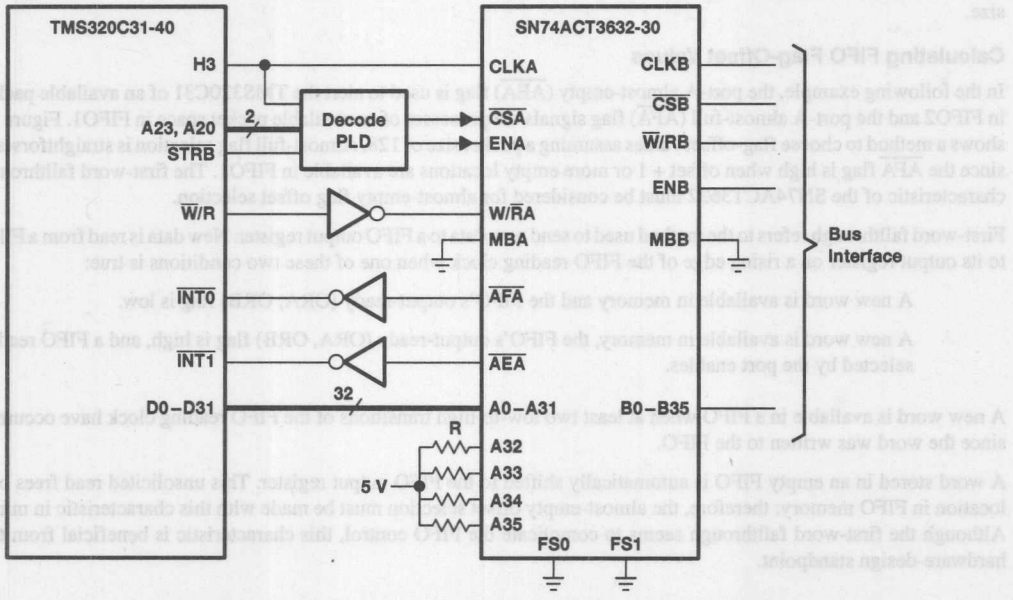
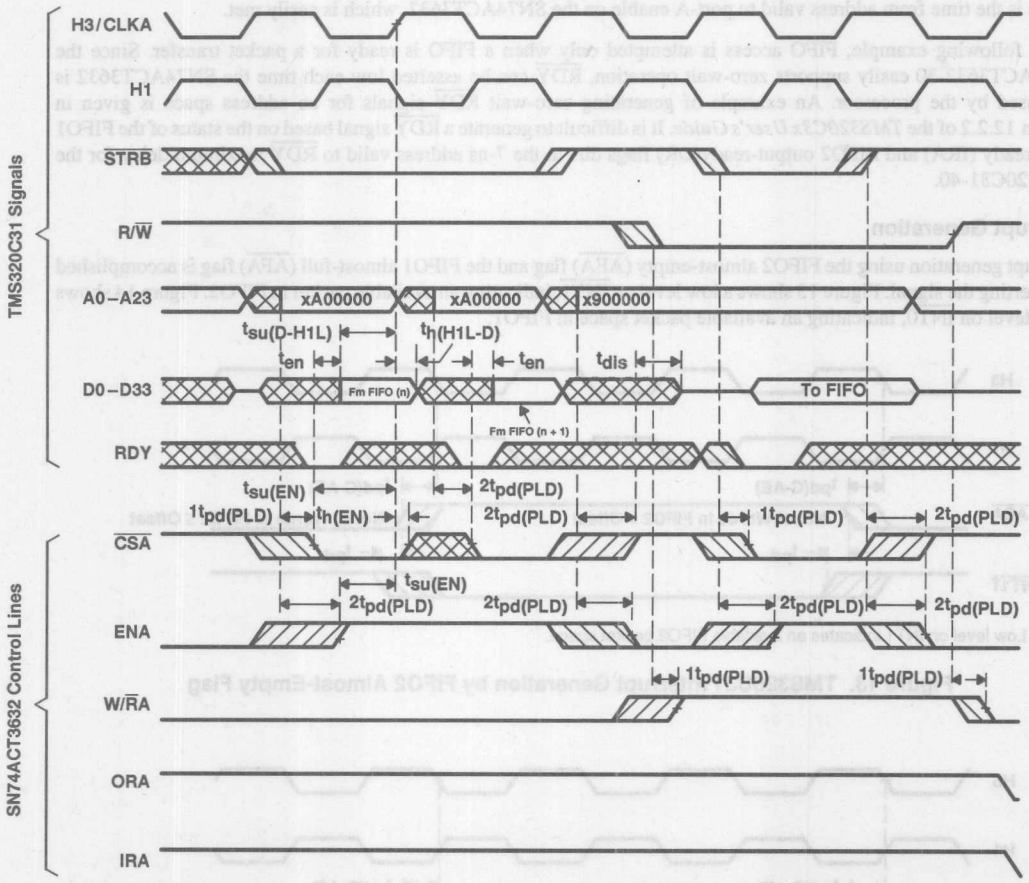


Figure 11. TMS320C31-40 Interface to an SN74ACT3632-30 FIFO

Read and Write Cycles

Figure 12 shows TMS320C31-40 read-read-write timing diagram in which the SN74ACT3632 port-A control lines accept the processor read and write cycles. Because the W/$\overline{R}$A input separates read and write cycles for the SN74ACT3632, the port-A chip select ($\overline{CSA}$) is logically sufficient for FIFO control. Due to timing considerations, the port-A enable (ENA) also is used to control FIFO read and write operations.

The H3 signal from the processor is used as an SN74ACT3632 rising-edge clock (CLKA). The rising edge of H3 occurs between 0 ns and 4 ns after the falling edge of H1, which is the processor bus-synchronizing event. According to the TMS320C31-40 timing, the processor address and $\overline{STRB}$ signals can change at the time of the falling edge of H1. If the minimum delay through the decode circuitry to a valid $\overline{CSA}$ signal is less than 5 ns, the SN74ACT3632 $\overline{CSA}$ to rising edge of CLKA hold time is violated.



Time values:

$1t_{pd(PLD)}$ = one PLD delay (3 ns min, 10 ns max)
$2t_{pd(PLD)}$ = two PLD delays (6 ns min, 10 ns max)
$t_{su(EN)}$ = 6 ns min
$t_{h(EN)}$ = 1 ns (hold time) + 4 ns (H1 low to H3 high) = 5 ns min

Figure 12. TMS320C31-40 Read-Read-Write Timing Diagram With an SN74ACT3632 512 × 36 × 2 FIFO

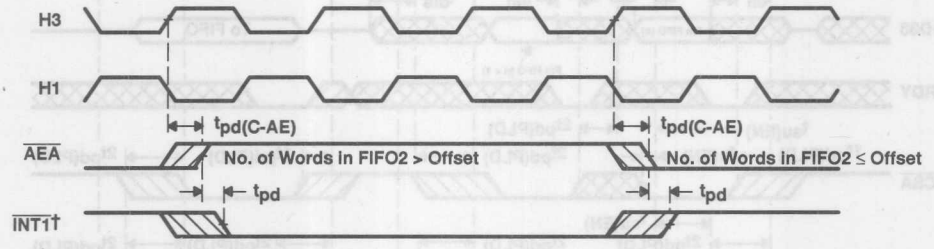
The minimum and maximum propagation delay times of a 10-ns PLD are 3 ns and 10 ns, respectively. A signal that feeds through the PLD twice has min/max switching of 6/20 ns, which eliminates the $\overline{CSA}$ hold-time problem but delays when the FIFO output bus is enabled. The solution to this problem is to design the $\overline{CSA}$ signal to have a single delay (3 ns, 10 ns) when switching from high to low for quick FIFO bus-enable times and a double delay (6 ns, 20 ns) when switching from low to high for proper $\overline{CSA}$ hold times. To prevent a $\overline{CSA}$ high-to-low transition from enabling a FIFO port-A transfer too early, the ENA signal is the inverse of the $\overline{CSA}$ signal with double delays (6 ns, 20 ns) for both high-to-low and low-to-high transitions.

A low on the TMS320C31 $\overline{RDY}$ signal during the low-to-high transition of H1 informs the processor that the present data-transfer cycle terminates on the next H1 falling edge. The first word written to an empty FIFO is automatically read to the FIFO output register. This data is available when the processor attempts to access it, since a FIFO2 read is attempted only when a data packet is available in FIFO2. Therefore, the first-word fallthrough characteristic of the SN74ACT3632 ensures FIFO reads can be done with zero wait cycles. The only constraint affecting zero-wait-state read access is the time from address valid to port-A enable on the SN74ACT3632, which is easily met.

In the following example, FIFO access is attempted only when a FIFO is ready for a packet transfer. Since the SN74ACT3632-30 easily supports zero-wait operation, $\overline{RDY}$ can be asserted low each time the SN74ACT3632 is addressed by the processor. An example of generating zero-wait $\overline{RDY}$ signals for an address space is given in section 12.2.2 of the *TMS320C3x User's Guide*. It is difficult to generate a $\overline{RDY}$ signal based on the status of the FIFO1 input-ready (IRA) and FIFO2 output-ready(OR) flags due to the 7-ns address valid to $\overline{RDY}$ maximum delay for the TMS320C31-40.

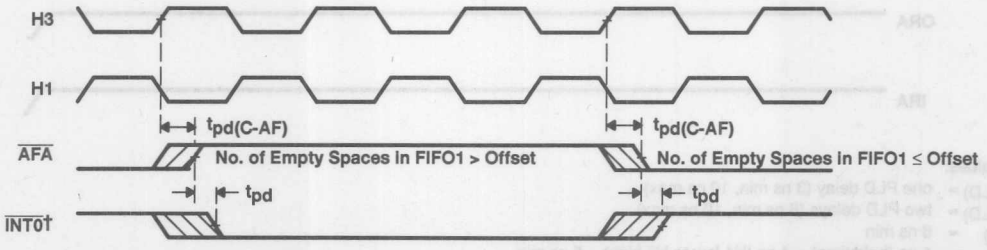
Interrupt Generation

Interrupt generation using the FIFO2 almost-empty ($\overline{AEA}$) flag and the FIFO1 almost-full ($\overline{AFA}$) flag is accomplished by inverting the signal. Figure 13 shows a low level on $\overline{INT1}$, indicating an available packet in FIFO2. Figure 14 shows a low level on $\overline{INT0}$, indicating an available packet space in FIFO1.



† Low level on $\overline{INT1}$ indicates an available FIFO2 packet space.

Figure 13. TMS320C31 Interrupt Generation by FIFO2 Almost-Empty Flag



† Low level on $\overline{INT0}$ indicates an available FIFO1 packet space.

Figure 14. TMS320C31 Interrupt Generation by FIFO1 Almost-Full Flag

Conclusion

FIFO memories are used in DSP systems for matching two datapaths with asynchronous clock or data rates. The SN74ACT3632 512 × 36 × 2 clocked FIFO provides a single-chip bidirectional buffering solution that interfaces nicely with TI floating-point DSPs. Programmable FIFO flags enable a variety of DMA control techniques to be used in handling data flow, and the FIFO control signals are easily derived from TMS320C3x outputs. Available in a variety of speed options, the SN74ACT3632 can interface a DSP to buses operating up to 67 MHz.

FIFOs With a Word Width of One Bit

First-In, First-Out Technology

Peter Forstner
Mixed Signal Logic Products

TEXAS INSTRUMENTS

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Introduction

In every digital system, data is continually being exchanged between various subsystems. Intermediate storage is always necessary if data arrives at the receiving subsystem at a high rate or in batches but can then only be processed slowly or irregularly. Such *intermediate stores* are familiar to us in our daily lives, for example, as queues of customers at the checkout of a supermarket or cars waiting at traffic lights. The checkout of goods at the supermarket point of sale proceeds slowly and regularly, while customers arrive there unpredictably; if many customers all want to pay at the same time, a queue builds up that the cashier processes on the principle of *first come, first served.* Queues of cars at traffic lights result from the sporadic arrival of traffic, which the lights allow to proceed only in regular batches.

An intermediate store or memory that operates on the above principle is known as a first-in, first-out (FIFO) memory. The first data written into a FIFO is also the first to leave it at readout. Texas Instruments (TI) offers a variety of FIFOs. These are available with word widths from 1 bit to 36 bits, storage densities from 64 to 2048 words of data, and clock speeds of up to 80 MHz. This application report is concerned exclusively with FIFOs having a word width of one bit and it suggests various possible applications for them.

Whenever a buffer memory is needed for serial-data transmission, there is a requirement for 1-bit-wide FIFOs. Digital telecommunications, local-area networks (LANs), serial transmission of data with the help of data compression, and communication between signal processors are all examples of serial data-transfer applications that require 1-bit-wide FIFOs. In some applications, the FIFOs are already integrated into the application-specific integrated circuit (ASIC) or the chip set with LANS. However, very often *discrete* FIFO components are required.

FIFO Basics

Every memory component for which the first word of data written to the memory is also the first to leave it when the memory is read out can be classified as a FIFO (see Figure 1). In practice, a further characteristic often required from a FIFO is asynchronism between the writing and reading processes. This kind of FIFO is known as an asynchronous FIFO.

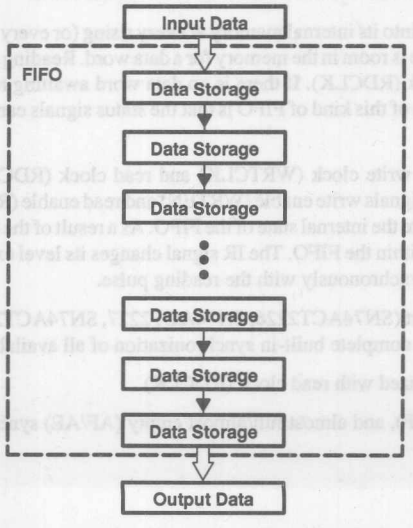


Figure 1. First-In, First-Out Data Flow

A FIFO has an input to which data words are written and a separate output from which data words are read. Since writing can take place completely asynchronously to reading, it is permissible for the writing and reading pulses to have completely different clock speeds, chosen at will. Control signals such as full, empty, half full, and almost full allow the controlling circuitry to monitor the internal state of the FIFO before every writing or reading process.

According to the control signals to write and read, asynchronous FIFOs can be classified into two groups; strobed FIFOs (see Figure 2) and clocked FIFOs (see Figure 3).

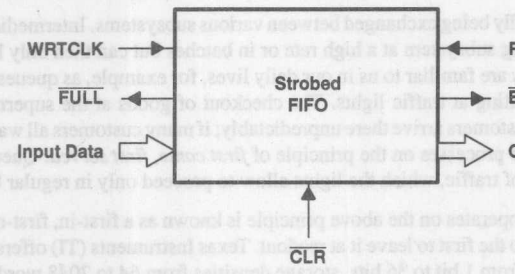


Figure 2. Connections of a Strobed FIFO

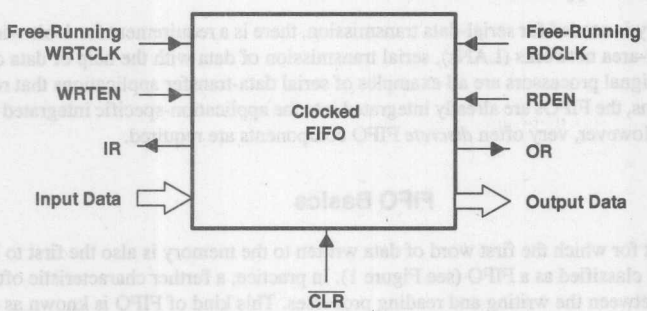


Figure 3. Connections of a Clocked FIFO

The strobed FIFO enters a word of data into its internal memory at every rising (or every falling) edge of the write clock (WRTCLK). $\overline{\text{FULL}}$ shows whether there is room in the memory for a data word. Reading a data word takes place at every rising (or falling) edge of the read clock (RDCLK). If there is no data word awaiting readout, this is indicated by the status signal $\overline{\text{EMPTY}}$. The disadvantage of this kind of FIFO is that the status signals cannot be fully synchronized with the corresponding clock signals.

Clocked FIFOs require a free-running write clock (WRTCLK) and read clock (RDCLK). The writing and reading processes are controlled by the control signals write enable (WRTEN) and read enable (RDEN). The status signals input ready (IR) and output ready (OR) indicate the internal state of the FIFO. As a result of the two free-running clock signals, all status signals can be synchronized within the FIFO. The IR signal changes its level exclusively in synchronism with the writing pulse, while OR switches synchronously with the reading pulse.

The 1-bit FIFOs in this application report (SN74ACT2226, SN74ACT2227, SN74ACT2228, and SN74ACT2229) are, without exception, clocked FIFOs with complete built-in synchronization of all available status signals, including:

Output ready (OR) synchronized with read clock (RDCLK)

Input ready (IR), half full (HF), and almost full/almost empty (AF/AE) synchronized with write clock (WRTCLK)

Telecommunications

The rapidly increasing need for telecommunication installations cannot, in the long run, be met by providing a separate line for every telephone connection; the simultaneous use of one line for several channels is a requirement. Digital transmission via pulse-code modulation (PCM) techniques enables the cost-effective use of single lines for multichannel transmission. Using these techniques, digitized telephone signals are switched successively onto a connecting line with the help of a multiplexer and separated from one another at the end of the line with a demultiplexer (see Figure 4).

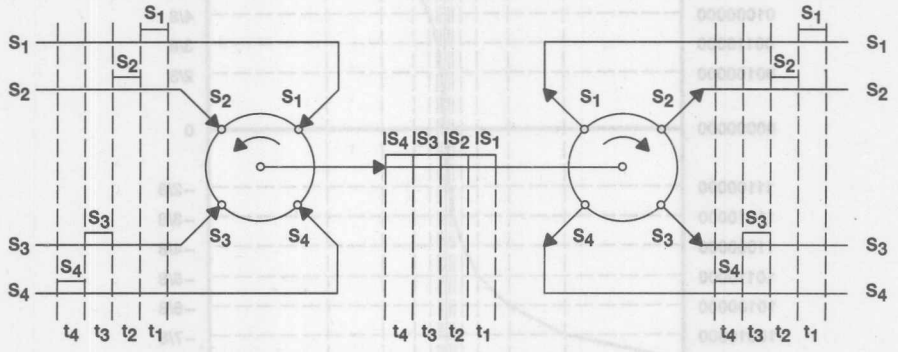


Figure 4. Time-Division Multiplex of Several Channels

With the 3.4-kHz upper bandwidth limit of a telephone channel and the internationally standardized sampling frequency for digitizing the signal ($f_0 = 8$ kHz), there remains enough space in the frequency band to insert the edge of the necessary bandwidth-limiting low-pass filter.

Although extensive tests of syllable intelligibility have shown that 7-bit quantization with 128 quantization intervals is adequate even with successive analog-to-digital-to-analog conversion, an 8-bit quantization with 256 intervals has been made the standard. For the compression of the instantaneous value of the signal, the logarithmic 13-segment characteristic shown in Figure 5 is used.

For the transmission of a channel, a bit rate of 8 kHz × 8 bit = 64 kbit/s is necessary and, correspondingly, a line for 32 multiplexed channels must attain a transmission rate of 64 kbit/s × 32 = 2048 kbit/s (CCITT recommendations G.732 and G.704).

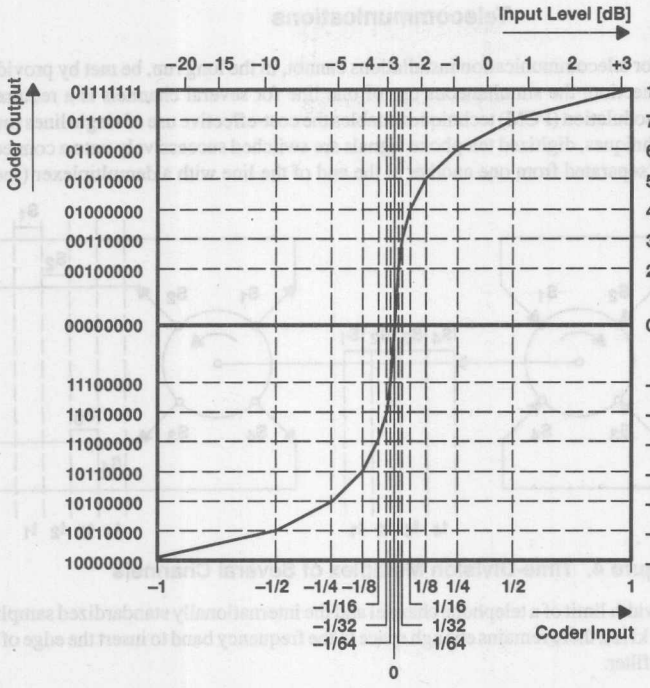


Figure 5. Logarithmic 13-Segment Characteristics for the Coding of Telephone Signals

Digital-Transmission Methods

At present, four different digital-transmission methods are used for telecommunications:

- European plesiochronous digital hierarchy (PDH, see Table 1)
- American plesiochronous digital hierarchy (PDH, see Table 1)
- Japanese plesiochronous digital hierarchy (PDH, see Table 1)
- Synchronous digital hierarchy (SDH, see Table 2)

Signals coming from various clock generators should have the same bit speeds but, in practice, the bit speed may deviate by a certain tolerance from the nominal value. These signals are referred to as plesiochronous signals.

The lack of worldwide standardization of the three PDH transmission methods makes world networking much more difficult, and the use of equipment from various manufacturers is limited to the networks of individual national telecommunications organizations. The fact that the standard for synchronous digital hierarchy (SDH, see Table 2) has worldwide validity does, however, offer the promise of assistance. SDH evolved from the North American synchronous optical network (SONET) specifications but is based (as described in the CCITT recommendations G.707, G708, and G709) on a bit rate of 155520 kbit/s (see Table 2); that is, exactly three times the SONET basic bit rate of 51840 kbit/s. The SDH basic signal is designated as synchronous transport module level one (STM-1); higher hierarchy levels are whole integer multiples of the level-one bit rate.

Table 1. Plesiochronous Digital Hierarchies

HIERARCHY LEVEL	HIERARCHIES BASED ON 2 Mbit/s	HIERARCHIES BASED ON 1.5 Mbit/s	
	EUROPE, SOUTH AMERICA	USA	JAPAN
1	2048 kbit/s	1544 kbit/s	1544 kbit/s
2	8448 kbit/s	6312 kbit/s	6312 kbit/s
3	34368 kbit/s	44736 kbit/s	32064 kbit/s
4	139264 kbit/s		97728 kbit/s

Table 2. Synchronous Digital Hierarchy and SONET

BIT RATE	SDH		SONET	
	LEVEL	SIGNAL IDENTIFICATION	LEVEL	SIGNAL IDENTIFICATION
51840 kbit/s			STS-1	OC-1
155520 kbit/s	1	STM-1	STS-3	OC-3
466560 kbit/s			STS-9	OC-9
622080 kbit/s	4	STM-4	STS-12	OC-12
933120 kbit/s			STS-18	OC-18
1244160 kbit/s			STS-24	OC-24
1866240 kbit/s			STS-36	OC-36
2488320 kbit/s	16	STM-16	STS-48	OC-48

A PDH Application Example

The plesiochronous digital hierarchy and the application of FIFOs for the synchronization of the PDH signals are demonstrated using as an example European transmissions based on a bit speed of 2048 kbit/s.

Frame Structure of the First Hierarchy Level

The bit speed of the first hierarchy level (2048 kbit/s, see Table 1) allows the transmission of 32 telephone channels, each of 64 kbit/s, over a normal telephone line. In this case, only 30 telephone conversations are transmitted, since two channels are required for the following additional information (see Figure 6):

Frame recognition word for the synchronization of the receiver

Cyclic-redundancy-check (CRC4) bits for the recognition of bit faults during the transmission

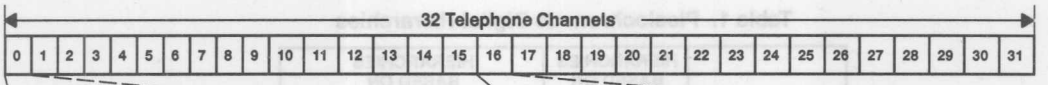
Service bits for initiating alarms

Registration bits for national and international telecommunication traffic

Telephone exchange technical identification (signalization)

Each of the eight bits of the 32 channels is multiplexed bit by bit; that is, bit 0 of the 32 channels is first sent serially over the line followed by 32 times bit 1, etc. These 8×32 bits = 256 bits are consolidated in a frame (see Figure 6). Channels 0 and 16 contain the necessary control information, while the remaining channels can be used for the transmission of 30 telephone connections. The transmission of a 256-bit frame of this kind at 2048 kbit/s requires a time period of 125 µs.

Sixteen frames together make up a $16 \times 256 = 4096$-bit multiple frame with a transmission time period of 2 ms. The 256 control bits in channels 0 and 16 can be seen in Figure 6.



FRAME NO.	FRAME BITS							
	1	2	3	4	5	6	7	8
0	C_1	0	0	1	1	0	1	1
1	D	1	D	N	S_n	S_n	S_n	S_n
2	C_2	0	0	1	1	0	1	1
3	0	1	D	N	S_n	S_n	S_n	S_n
4	C_3	0	0	1	1	0	1	1
5	0	1	D	N	S_n	S_n	S_n	S_n
6	C_4	0	0	1	1	0	1	1
7	0	1	D	N	S_n	S_n	S_n	S_n
8	C_1	0	0	1	1	0	1	1
9	0	1	D	N	S_n	S_n	S_n	S_n
10	C_2	0	0	1	1	0	1	1
11	0	1	D	N	S_n	S_n	S_n	S_n
12	C_3	0	0	1	1	0	1	1
13	0	1	D	N	S_n	S_n	S_n	S_n
14	C_4	0	0	1	1	0	1	1
15	0	1	D	N	S_n	S_n	S_n	S_n

FRAME NO.	FRAME BITS							
	1	2	3	4	5	6	7	8
0	0	0	0	0	X	Y	X	X
1	a_1	b_1	c_1	d_1	a_{17}	b_{17}	c_{17}	d_{17}
2	a_2	b_2	c_2	d_2	a_{18}	b_{18}	c_{18}	d_{18}
3	a_3	b_3	c_3	d_3	a_{19}	b_{19}	c_{19}	d_{19}
4	a_4	b_4	c_4	d_4	a_{20}	b_{20}	c_{20}	d_{20}
5	a_5	b_5	c_5	d_5	a_{21}	b_{21}	c_{21}	d_{21}
6	a_6	b_6	c_6	d_6	a_{22}	b_{22}	c_{22}	d_{22}
7	a_7	b_7	c_7	d_7	a_{23}	b_{23}	c_{23}	d_{23}
8	a_8	b_8	c_8	d_8	a_{24}	b_{24}	c_{24}	d_{24}
9	a_9	b_9	c_9	d_9	a_{25}	b_{25}	c_{25}	d_{25}
10	a_{10}	b_{10}	c_{10}	d_{10}	a_{26}	b_{26}	c_{26}	d_{26}
11	a_{11}	b_{11}	c_{11}	d_{11}	a_{27}	b_{27}	c_{27}	d_{27}
12	a_{12}	b_{12}	c_{12}	d_{12}	a_{28}	b_{28}	c_{28}	d_{28}
13	a_{13}	b_{13}	c_{13}	d_{13}	a_{29}	b_{29}	c_{29}	d_{29}
14	a_{14}	b_{14}	c_{14}	d_{14}	a_{30}	b_{30}	c_{30}	d_{30}
15	a_{15}	b_{15}	c_{15}	d_{15}	a_{31}	b_{31}	c_{31}	d_{31}

0011011 Frame Recognition Word
$C_4 \ldots C_1$ CRC4 Control Bits
D, N Bits for Alarm Initiation
S_i, S_n Registration Bits

0000XYXX Multiple Frame Recognition Word
$a_n \ldots d_n$ Signalization for Channel n

Figure 6. Frame Structure of the 2048-kbit/s Multiplex Signal (First Hierarchy Level)

Frame Structures of the Second to Fifth Hierarchy Levels

For further sections, four 2048-kbit/s signals are transmitted with successive bit-by-bit time-division multiplexing combined with the pulse-stuffing procedure at bit speeds of 8448 kbit/s, 34368 kbit/s, 139264 kbit/s, and 564992 kbit/s.

If several plesiochronous signals are multiplexed, they must be synchronized before the multiplexing process. Plesiochronous signals have nominally the same bit speeds; but, in practice, the following kinds of asynchronism can arise:

The bit rates deviate from one another within the specified tolerance (drift).

As a result of long transmission distances and significant differences of temperature, etc., the bit speeds fluctuate for short periods (jitter).

For the synchronization of many plesiochronous 2048 kbit/s signals, positive pulse-stuffing techniques are used when multiplexing these signals into an 8-mbit/s signal. The principle of this technique is based on the fact that, in the multiplexed signal, a bandwidth is made available that is wider than the nominal bit rate requires. If at particular points in the transmission information bits or empty bits (so-called stuffing bits) are sent out, the bit speed can be reduced and thus adjusted to suit the input signal. This technique also compensates for drift and jitter of the input signal.

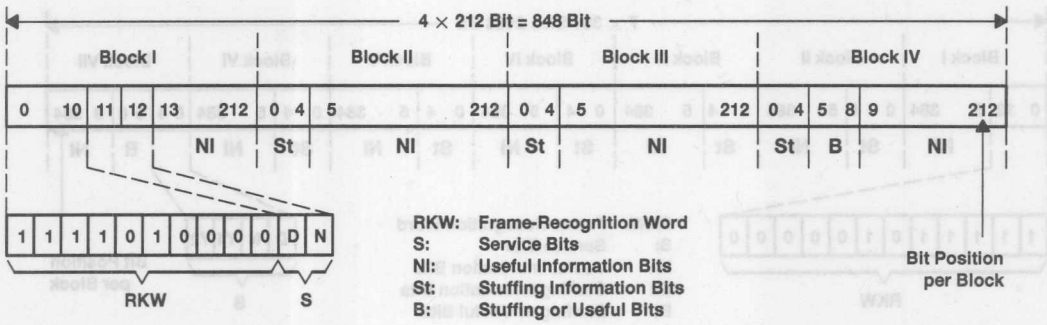


Figure 7. Frame Structure of the 8448-kbit/s Multiplex Signal (Second Hierarchy Level)

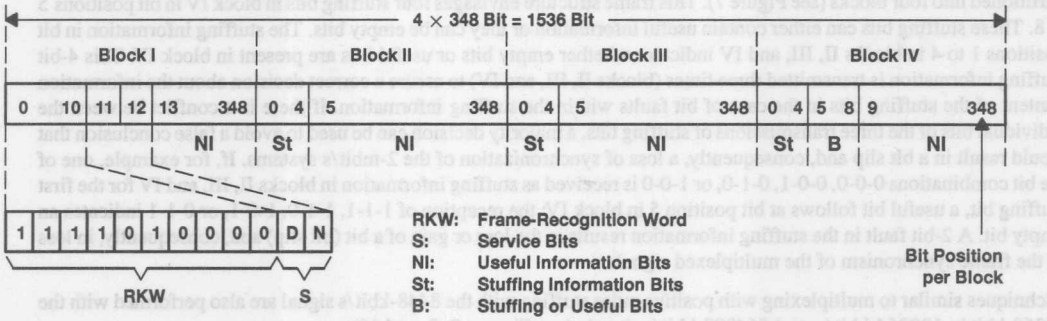


Figure 8. Frame Structure of the 34368-kbit/s Multiplex Signal (Third Hierarchy Level)

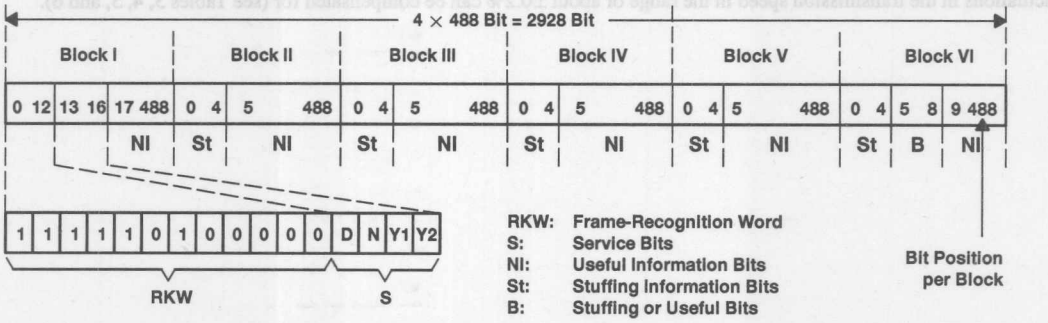


Figure 9. Frame Structure of the 139264-kbit/s Multiplex Signal (Fourth Hierarchy Level)

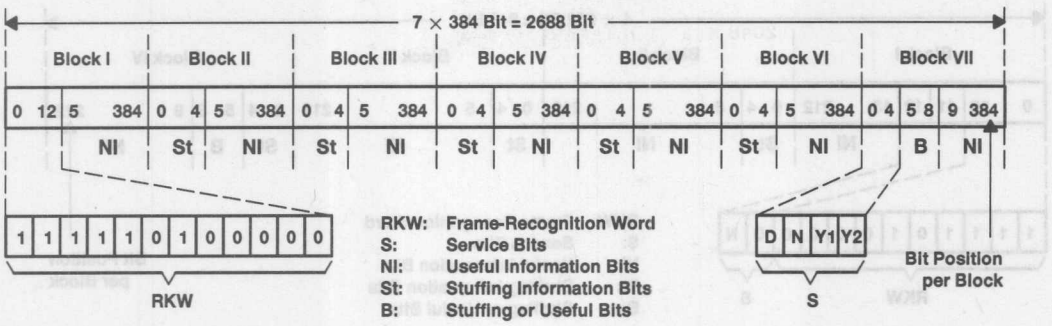


Figure 10. Frame Structure of the 564992-kbit/s Multiplex Signal (Fifth Hierarchy Level)

When multiplexing with positive pulse-stuffing techniques, a frame that is constructed with a 8448-kbit/s signal is partitioned into four blocks (see Figure 7). This frame structure envisages four stuffing bits in block IV in bit positions 5 to 8. These stuffing bits can either contain useful information or they can be empty bits. The stuffing information in bit positions 1 to 4 in blocks II, III, and IV indicates whether empty bits or useful bits are present in block IV. This 4-bit stuffing information is transmitted three times (blocks II, III, and IV) to assure a correct decision about the information content of the stuffing bits in the case of bit faults within the stuffing information. If there is a conflict between the individual bits of the three transmissions of stuffing bits, a majority decision can be used to avoid a false conclusion that would result in a bit slip and, consequently, a loss of synchronization of the 2-mbit/s systems. If, for example, one of the bit combinations 0-0-0, 0-0-1, 0-1-0, or 1-0-0 is received as stuffing information in blocks II, III, and IV for the first stuffing bit, a useful bit follows at bit position 5 in block IV; the reception of 1-1-1, 1-1-0, 1-0-1, or 0-1-1 indicates an empty bit. A 2-bit fault in the stuffing information results in the loss or gain of a bit (bit slip) and, consequently, in loss of the frame synchronism of the multiplexed signals.

Techniques similar to multiplexing with positive pulse stuffing with the 8448-kbit/s signal are also performed with the 34368-kbit/s, 139264-kbit/s, and 564992-kbit/s signals (see Figures 8, 9, and 10).

As a result of these stuffing techniques, a 8448-kbit/s frame has a transmission speed in the range of 8169-kbit/s to 8209-kbit/s useful bits. With the nominal transmission speed for four multiplexed 2048-kbit/s signals of 8192-kbit/s, fluctuations in the transmission speed in the range of about ±0.2% can be compensated for (see Tables 3, 4, 5, and 6).

Table 3. Spread of the Transmission Capacity of an 8448-kbit/s Signal Consisting of Four Multiplexed 2048-kbit/s Signals With a Net Nominal Transmission Speed of 4 × 2048 kbit/s = 8192 kbit/s

	FRAME	USEFUL BITS		
		0 STUFFING BITS	2 STUFFING BITS	4 STUFFING BITS
Frame Capacity	848 bits	820 bits	822 bits	824 bits
Transmission Speed	8448 kbit/s	8169 kbit/s	8189 kbit/s	8209 kbit/s
Nominal Value		8192 kbit/s	8192 kbit/s	8192 kbit/s
Deviation from Nominal Value		−0.28%	−0.04%	+0.21%

Table 4. Spread of the Transmission Capacity of a 34368-kbit/s Signal Consisting of Four Multiplexed 8448-kbit/s Signals With a Net Nominal Transmission Speed of 4 × 8448 kbit/s = 33792 kbit/s

	FRAME	USEFUL BITS		
		0 STUFFING BITS	2 STUFFING BITS	4 STUFFING BITS
Frame Capacity	1536 bits	1508 bits	1510 bits	1512 bits
Transmission Speed	34368 kbit/s	33742 kbit/s	33786 kbit/s	33831 kbit/s
Nominal Value		33792 kbit/s	33792 kbit/s	33792 kbit/s
Deviation from Nominal Value		−0.15%	−0.02%	+0.12%

Table 5. Spread of the Transmission Capacity of a 139264-kbit/s Signal Consisting of Four Multiplexed 34368-kbit/s Signals With a Net Nominal Transmission Speed of 4 × 34368 kbit/s = 137472 kbit/s

	FRAME	USEFUL BITS		
		0 STUFFING BITS	2 STUFFING BITS	4 STUFFING BIts
Frame Capacity	2928 bits	2888 bits	2890 bits	2892 bits
Transmission Speed	139264 kbit/s	137361 kbit/s	137457 kbit/s	137552 kbit/s
Nominal Value		137472 kbit/s	137472 kbit/s	137472 kbit/s
Deviation from Nominal Value		−0.08%	−0.01%	+0.06%

Table 6. Spread of the Transmission Capacity of a 564992-kbit/s Signal Consisting of Four Multiplexed 139264-kbit/s Signals With a Net Nominal Transmission Speed of 4 × 139264 kbit/s = 557056 kbit/s

	FRAME	USEFUL BITS		
		0 STUFFING BITS	2 STUFFING BITS	4 STUFFING BITS
Frame Capacity	2688 bits	2648 bits	2650 bits	2652 bits
Transmission Speed	564992 kbit/s	556584 kbit/s	557005 kbit/s	557425 kbit/s
Nominal Value		557056 kbit/s	557056 kbit/s	557056 kbit/s
Deviation from Nominal Value		−0.08%	−0.01%	+0.07%

Clock Adjustment With FIFOs

Clock Adjustment at the Transmitting End

A block diagram showing the principle of clock adjustment at the transmitting end with positive pulse-stuffing techniques is shown in Figure 11. In this case, each channel is provided with an elastic memory in the form of a FIFO.

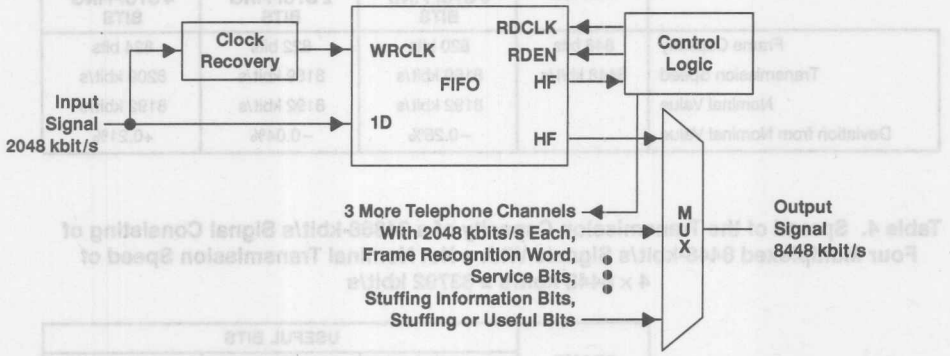


Figure 11. Clock Adjustment at the Transmitting End With Positive Pulse-Stuffing Techniques Block Diagram

The input data is written into this FIFO with the help of a circuit for clock recovery. The FIFO takes on the buffering of the input data while the frame and stuffing information is being transmitted. If information bits are to be transmitted, the control logic of the transmission path extracts the data from the FIFO. With positive pulse-stuffing techniques, the net bit speed of the transmission path is slightly higher than the bit speed of the incoming signal. As a result, the transmission-path controller reads the data from the FIFO more quickly than it can deliver it to the input channel. Whenever the FIFO contains less than a certain minimum filled level (e.g., half full), the transmission path sends at the next possible moment a stuffing bit instead of a data bit. As a result, the input channel has enough time to raise the filled level of the FIFO above the specified minimum level by writing in further data (see Figure 12).

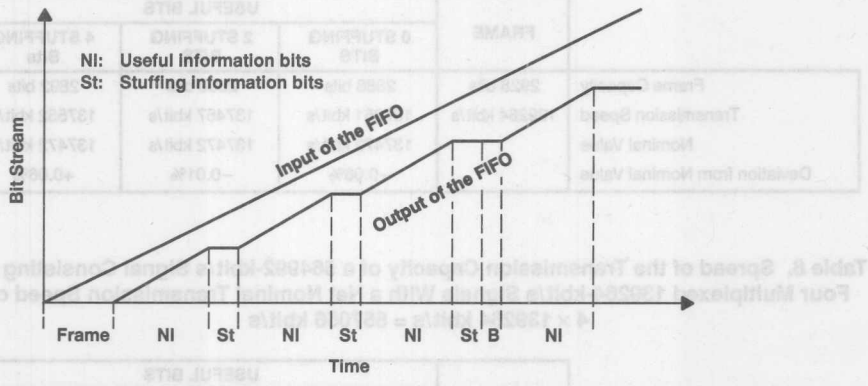


Figure 12. Bit Stream at the FIFO of the Transmitter-Clock Adjustment

If the minimum level of the FIFO when sending block II (see Figure 7) is not reached, the stuffing information in block II can no longer be changed. Accordingly, a wait must be made until the next frame when the necessary stuffing-information bits and the associated stuffing bits can be transmitted. The maximum number of data words that can be stored in the FIFO should be chosen such that the FIFO will not become empty during this time period. In addition, the FIFO must be in a position to buffer the arriving data during the transmission of the frame bits.

Clock Adjustment at the Receiving End

There is also an elastic memory (FIFO) at the receiving end of each channel. Figure 15 shows that the information is written into the FIFO with the multiplex clock pulse divided by n. As a result of the now well-known frame structure, writing must be inhibited while the additional information is being received. The writing process also must be interrupted when stuffing bits are received (see Figure 13). Consequently, received data is written into the FIFO block by block (see Figure 14).

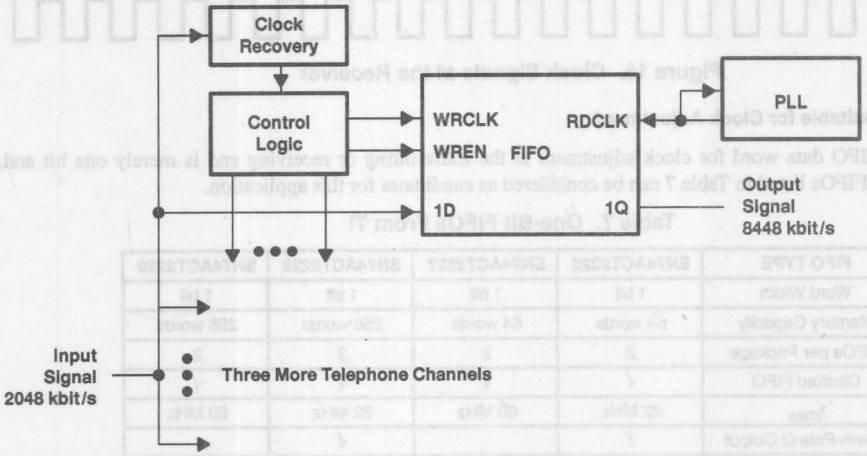


Figure 13. Clock Adjustment at the Receiving End With Positive Pulse-Stuffing Techniques Block Diagram

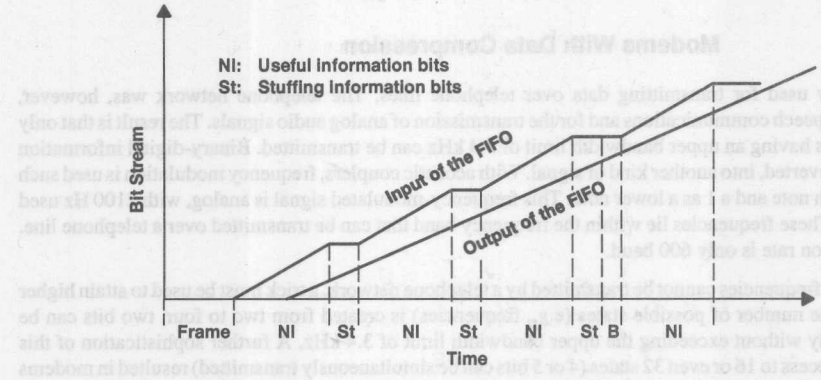


Figure 14. Bit Stream at the FIFO of the Receiver-Clock Adjustment

The write clock of the FIFO has as a nominal clock frequency (the multiplex clock divided by n); however, during the reception of the frame and the stuffing bits, several clock periods are omitted. Over a long period of time, the bit speed is identical with that of the original signal at the transmitter end (see Figure 15). As a read pulse for the FIFO, a regular clock without gaps is needed so that a continual bit stream conforming to the original signal is supplied. A PLL circuit reconstitutes this continuous clock signal from the clock signal containing gaps, although there is a small amount of jitter.

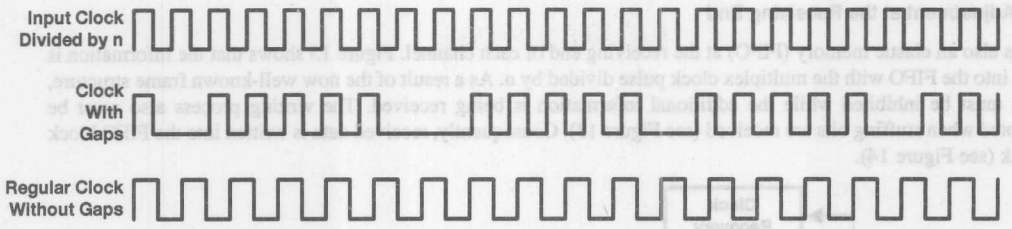


Figure 15. Clock Signals at the Receiver

Types of FIFOs Suitable for Clock Adjustment

The width of a FIFO data word for clock adjustment at the transmitting or receiving end is merely one bit and, consequently, the FIFOs listed in Table 7 can be considered as candidates for this application.

Table 7. One-Bit FIFOs From TI

FIFO TYPE	SN74ACT2226	SN74ACT2227	SN74ACT2228	SN74ACT2229
Word Width	1 bit	1 bit	1 bit	1 bit
Memory Capacity	64 words	64 words	256 words	256 words
FIFOs per Package	2	2	2	2
Clocked FIFO	√	√	√	√
f_{max}	22 MHz	60 MHz	22 MHz	60 MHz
Totem-Pole Q Output	√		√	
3-State Q Output		√		√
Half-Full Flag	√	√	√	√
Almost-Full Flag	√	√	√	√

Modems With Data Compression

Modems are now widely used for transmitting data over telephone lines. The telephone network was, however, originally developed for speech communications and for the transmission of analog audio signals. The result is that only alternating-current signals having an upper bandwidth limit of 3.4 kHz can be transmitted. Binary-digital information must be modulated, or converted, into another kind of signal. With acoustic couplers, frequency modulation is used such that a 0 is audible as a high note and a 1 as a lower note. This frequency-modulated signal is analog, with 2100 Hz used for 0 and 1700 Hz for 1. These frequencies lie within the frequency band that can be transmitted over a telephone line. The maximum transmission rate is only 600 baud.

Since significantly higher frequencies cannot be transmitted by a telephone network, a trick must be used to attain higher transmission speeds. If the number of possible states (e.g., frequencies) is created from two to four, two bits can be transmitted simultaneously without exceeding the upper bandwidth limit of 3.4 kHz. A further sophistication of this multistage modulation process to 16 or even 32 states (4 or 5 bits can be simultaneously transmitted) resulted in modems having a transmission capacity of up to 9600 bit/s but at the same time a transmission system that was more susceptible to interference.

A further increase of transmission speed by means of yet more sophisticated modulation methods would have been difficult; therefore, data compression has been used to improve performance. This involves examining the bit stream for redundant information, then compressing it. The receiver recognizes the parts of the signal that have been compressed and expands them in order to reconstitute the original signal. In a typical case, redundancy of the transmitted bit stream allows a 50% reduction of the original data, whereby the possibility for compression can typically range from 0% to 75%.

If, for example, a computer sends data via synchronous serial interface to a modem having a data rate of 4800 baud, the modem uses data compression to reduce the information to a transmission speed of 2400 baud and subsequently sends it without problems over a telephone line (see Figure 16). Variations in the compressibility of the signal are, in this case, buffered by a FIFO. If the transmitted data is not compressible, the data received from the interface line is temporarily stored by a FIFO in the modem. When the potential for data compression increases to over 50%, the modem again accepts data stored in the FIFO. Only if the compressibility of the transmitted data deviates significantly and for a long time from the average value (50%) must the arriving data stream be halted or the data stream that is leaving be interrupted.

The same speed variations arise with data expansion at the receiver as with compression at the transmitter. A FIFO also is used here to buffer the data and to ensure a constant flow of data to the receiver.

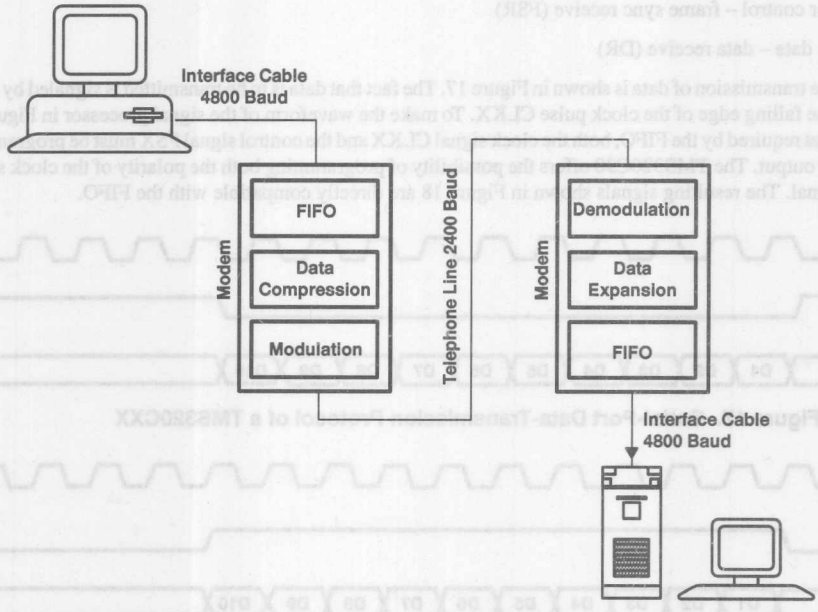


Figure 16. Data Transmission by Modem With Data Compression

Since in this application a serial stream needs to be buffered by the FIFO, the FIFOs having a word width of one bit shown in Table 7 are suitable. The two FIFOs needed for duplex operation (for transmitter and receiver) have already been integrated with these FIFO types into a single package.

Signal-Processor Interfaces

The signal processors from TI's TMS320CXX family have one or more serial ports to allow them to communicate with other signal processors or for data exchange with peripheral equipment such as the analog interface circuit (AIC). For data transmission, the signal processors make use of the following signals:

Transmit clock – clock transmit (CLKX)

Transmitter control – frame sync transmit (FSX)

Transmit data – data transmit (DX)

Receiver clock – clock receive (CLKR)

Receiver control – frame sync receive (FSR)

Receive data – data receive (DR)

The protocol for the transmission of data is shown in Figure 17. The fact that data is to be transmitted is signaled by FSX, which occurs on the falling edge of the clock pulse CLKX. To make the waveform of the signal processor in Figure 17 compatible with that required by the FIFO, both the clock signal CLKX and the control signal FSX must be programmed to give an inverted output. The TMS320C30 offers the possibility of programming both the polarity of the clock signal and the control signal. The resulting signals shown in Figure 18 are directly compatible with the FIFO.

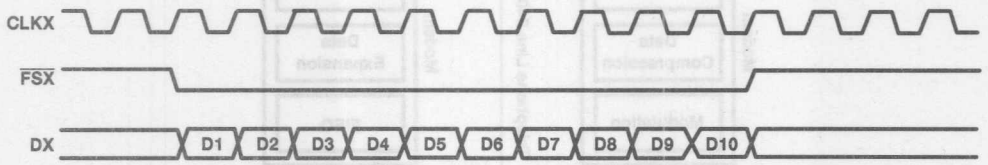


Figure 17. Serial-Port Data-Transmission Protocol of a TMS320CXX

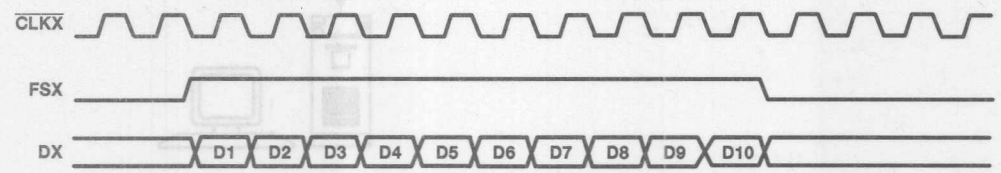


Figure 18. Serial-Port Data-Transmission Protocol With Inverted Signals

With data transmission via a serial port, both the transmitter and the receiver must normally be ready to operate simultaneously since the TMS320CXX has only a single word of internal buffer memory apart from the transmit and receive buffers. If a SN74ACT2229 FIFO is switched into the communication channel, both transmitter and receiver do not need to transfer data simultaneously. Each participant can complete the data transfer when time allows. The time that is saved is available for processing other jobs.

Figure 19 shows the connection of two TMS320C30 devices. The connection of an analog interface circuit (AIC) to a TMS320C30 is made similarly. Since two independent FIFOs are integrated into a single SN74ACT2229, full-duplex operation is possible with only one package.

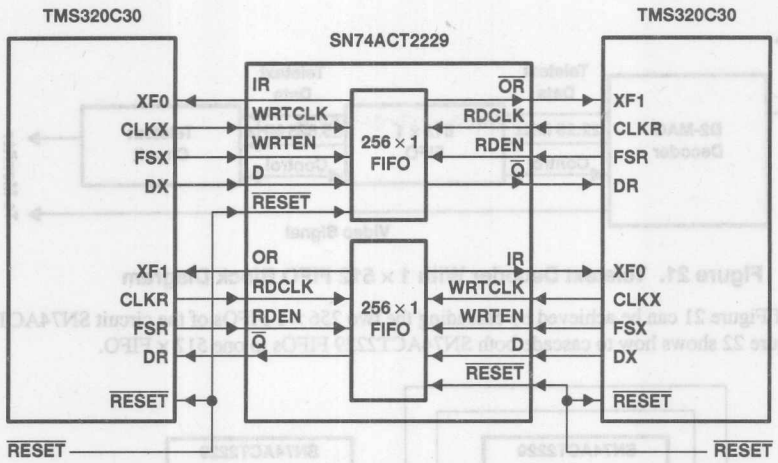


Figure 19. Connection of Two Signal Processors via a Serial Port With the Help of the FIFO SN74ACT2229

Teletext Decoders

With teletext, pages of text are transmitted as digital information in addition to the normal television signal. To be compatible with existing TV receivers, this digital information is transmitted in the picture-frequency blanking interval. The invisible picture lines, sent during beam flyback but after those for picture synchronization, contain the digital teletex data instead of picture information (see Figure 20). With D2-MAC, 360 bits with a bit rate of 20.25 Mbit/s are transmitted per TV line; therefore, the teletext information occupies 17.8 µs of the 64 µs for which the TV line lasts. In this example, a D2-MAC decoder extracts the digital teletext information from the television signal and conducts it to a 512 x 1 FIFO (see Figure 21). The D2-MAC decoder writes the data block by block at a rate of 20.25 Mbit/s into the FIFO. The teletext module is now able to read out and process the 360-bit digital information within 64 µs at a significantly slower rate of up to 5.625 Mbit/s. In this example, the FIFO undertakes the adjustment and synchronization of the two different rates.

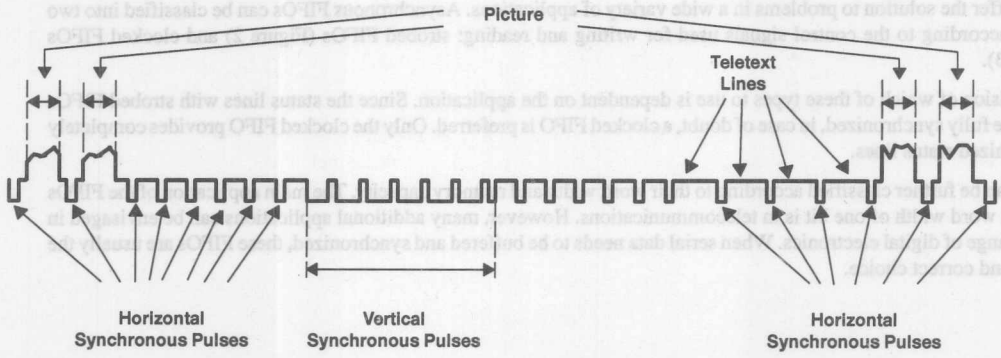


Figure 20. Video Signal

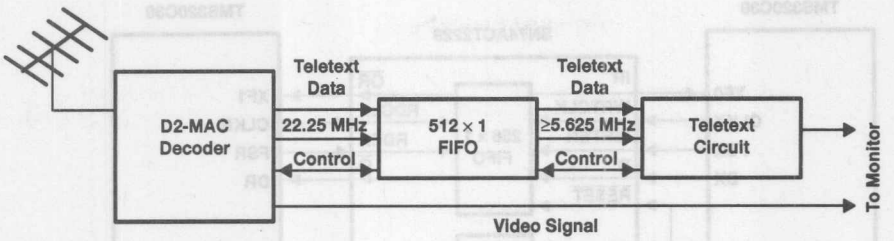


Figure 21. Teletext Decoder With 1 × 512 FIFO Block Diagram

The 512 × 1 FIFO of Figure 21 can be achieved by cascading the two 256 × 1 FIFOs of the circuit SN74ACT2228 or SN74ACT2229. Figure 22 shows how to cascade both SN74ACT2229 FIFOs to one 512 × FIFO.

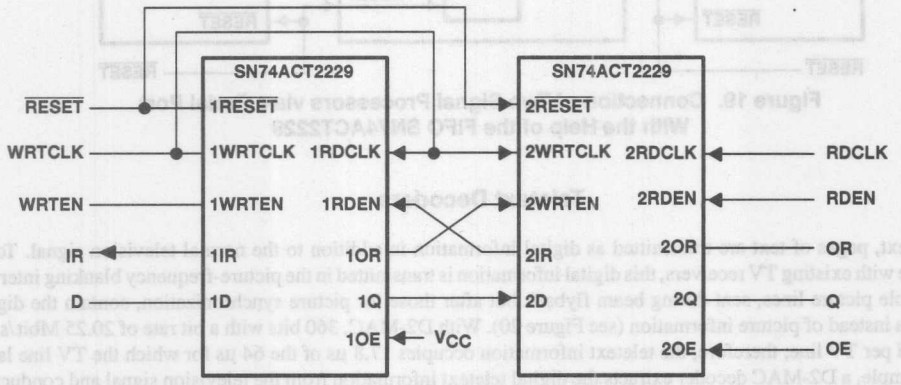


Figure 22. Extending Memory Depth of a SN74ACT2229 FIFO to 512 × 1 Bit

Summary

FIFOs offer the solution to problems in a wide variety of applications. Asynchronous FIFOs can be classified into two groups according to the control signals used for writing and reading: strobed FIFOs (Figure 2) and clocked FIFOs (Figure 3).

The decision of which of these types to use is dependent on the application. Since the status lines with strobed FIFOs cannot be fully synchronized, in case of doubt, a clocked FIFO is preferred. Only the clocked FIFO provides completely synchronized status lines.

FIFOs can be further classified according to their word width and memory capacity. The main application of the FIFOs having a word width of one bit is in telecommunications. However, many additional applications can be envisaged in a wide range of digital electronics. When serial data needs to be buffered and synchronized, these FIFOs are usually the logical and correct choice.

Internetworking the SN74ABT3614

Chris Wellheuser and Vasanta Madduri
Advanced System Logic – Semiconductor Group

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Introduction

Texas Instruments (TI's) SN74ABT3614 is a clocked first-in, -first-out (FIFO) memory with enhanced features required by today's complex networks. The FIFO has all the necessary logic for performing bus-matching, byte-swapping, parity-generation, and parity-checking functions integrated onto a single chip. This on-chip integration greatly simplifies the system designer's job in several ways:

- Easier interconnection of complex networks
- Reduces system bottlenecks
- Helps meet critical timing delays
- Reduces board area

This application report describes the architectural implementation of each of these enhanced features. The first section provides an overview of the SN74ABT3614 architecture and the enhanced features and applications rationale for combining these features with FIFO memory. The second section describes port-B configurations for bus matching and byte swapping. The second section highlights the internal register arrangements, the order of their access during port-B configurations, and the effect of these configurations on the flag operation. The third section describes parity-generation and parity-checking schemes. The fourth section includes an internetworking application example of the SN74ABT3614.

FIFO Architecture

The SN74ABT3614 functional block diagram is shown in Figure 1. The device utilizes dual-port SRAM architecture to provide simultaneous read and write access. Port A is a 36-bit-wide port and port B can be programmed to variable bus widths. All data transfers through a port are synchronized to the low-to-high transition of a continuous port clock by enable signals. The port clocks are independent of one another and can be asynchronous or coincident.

Two independent 64 × 36 FIFOs (FIFO1 and FIFO2) provide bidirectional data buffering between the two ports. Each of these FIFOs supports clock frequencies up to 67 MHz and has data access times as fast as 10 ns. Both FIFOs have full (FF), almost-full ($\overline{AF}$), almost-empty ($\overline{AE}$), and empty ($\overline{EF}$) flags to indicate their relative status. The $\overline{AF}$ and $\overline{AE}$ flags are programmable, which provides flexibility and control during data transfers. The two 36-bit mailbox registers, (MAIL1 and MAIL2) provide a path around these FIFOs to transmit information in each direction. Each mailbox register has a status flag to alert the user that data is present in the mailbox.

The bidirectional-FIFO core previously described is coupled with additional logic to perform bus matching, byte swapping, and parity generation and checking. The bus-matching logic enables port B of the chip to perform byte-size, word-size, or long-word-size data transfers. In addition, this logic allows the user to chose big-endian or little-endian configurations with byte (9-bit), word-size (18-bit), and long-word-size (36-bit) implementations. These size implementations can be achieved dynamically. The SN74ABT3614 can be used to facilitate data communication between processors or buses of different widths and speeds. Figure 2 shows an example of a 9-bit HDLC communications controller interfacing to a 36-bit high-speed bus using the SN74ABT3614.

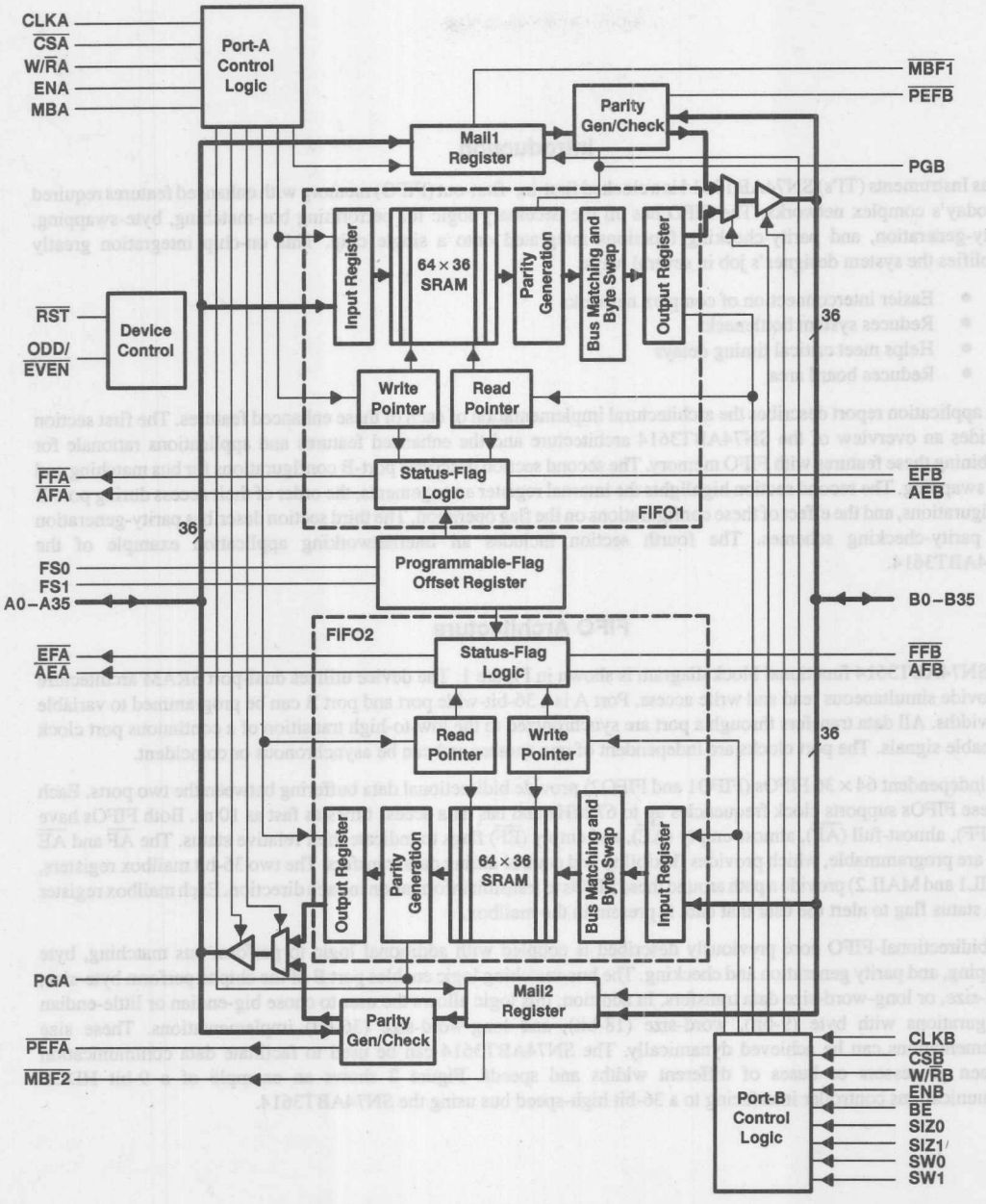


Figure 1. SN74ABT3614 Functional Block Diagram

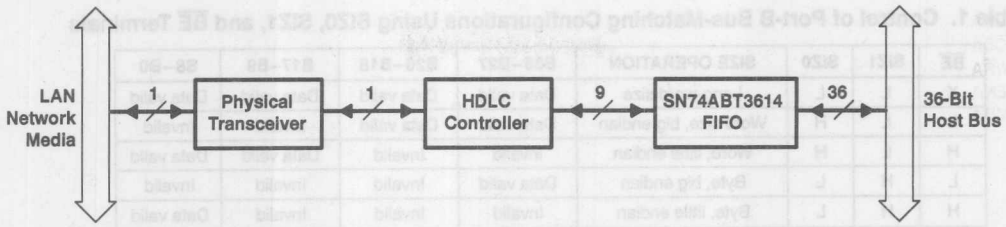


Figure 2. Bus-Matching Example

The byte swapping logic implements four different byte-order arrangements on port B: no swap, byte swap, word swap, and byte-word swap. In particular, the byte-swap operation is useful when a compatible interface between processors from different families is required. For example, the memory organization for the Intel™ 8086 and Motorola 68000 processors is shown in Figure 3. The Intel 8086 uses the little-endian format and Motorola 68000 uses the big-endian format for byte ordering. The byte order within the word has to be swapped in order to establish communication between the two processors. The byte-swap operation of the SN74ABT3614 implements a hardware solution that is faster than a software solution. The byte-swap arrangements can be implemented in conjunction with the size configurations, giving the user great flexibility in configuring networks.

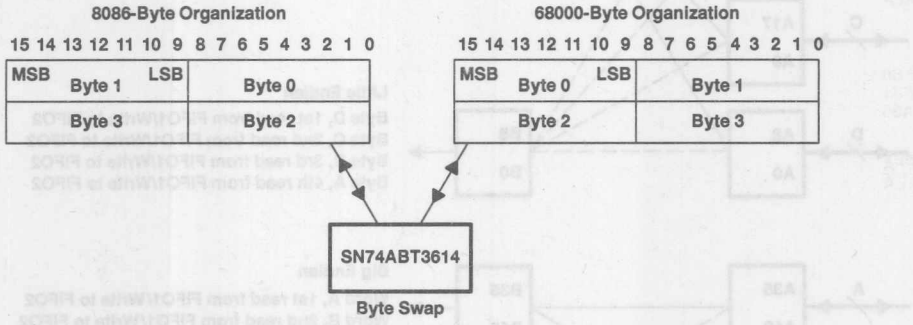


Figure 3. Memory Organization in Different Processor Families

The parity-checking logic allows a form of error checking in data-transmission circuits. Either odd- or even-parity checking can be chosen on incoming data on both port A and port B. A parity error on one or more valid data bytes on a port is alerted by the port's parity-error flag.

Like parity checking, either odd- or even-parity generation can be performed on both ports. The parity-generation logic replaces the most significant bit of each byte to make the total number of ones in the byte (including the parity bit) either odd or even.

Port-B Configuration for Bus Matching and Byte Swapping

Bus Sizing

Port B can be configured for byte-size (9-bit), word-size (18-bit), or long-word-size (36-bit) data transfers, with a choice of big-endian or little-endian formats for byte- and word-size configurations. The size (SIZ1and SIZ0) and big-endian ($\overline{BE}$) input terminals are used to achieve these bus-matching configurations.

During bus-matching operations, each low-to-high transition of the port-B clock (CLKB) cycle stores the levels on the SIZ0, SIZ1, and $\overline{BE}$ input terminals and implements the size on the next clock cycle. Table 1 shows the levels on the five input terminals and the respective size selected. Figure 4 illustrates the data transfer during byte- and word-size configurations. The data transfer for big-endian implementation is indicated by the solid lines; little-endian implementation is indicated by the dotted lines.

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Table 1. Control of Port-B Bus-Matching Configurations Using SIZ0, SIZ1, and $\overline{BE}$ Terminals

$\overline{BE}$	SIZ1	SIZ0	SIZE OPERATION	B35–B27	B26–B18	B17–B9	B8–B0
X	L	L	Long-word size	Data valid	Data valid	Data valid	Data valid
L	L	H	Word size, big endian	Data valid	Data valid	Invalid	Invalid
H	L	H	Word, little endian	Invalid	Invalid	Data valid	Data valid
L	H	L	Byte, big endian	Data valid	Invalid	Invalid	Invalid
H	H	L	Byte, little endian	Invalid	Invalid	Invalid	Data valid

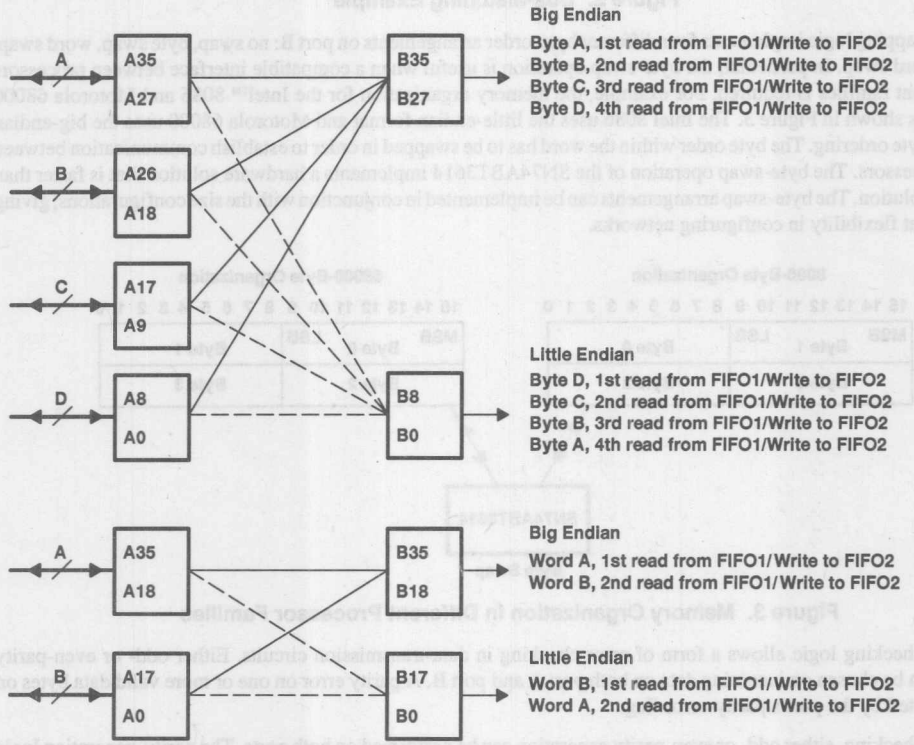


Figure 4. Port-B Bus-Matching Configurations

The bus size can be reconfigured dynamically and synchronous to CLKB rising edge using the SIZ0, SIZ1, and $\overline{BE}$ inputs as control. However, if the low-to-high CLKB transition of a particular CLKB cycle stores new levels on the control terminals, it is the next CLKB cycle that implements the size configuration chosen by those new levels; therefore, bus size can be changed on the fly with a minimum of one clock-cycle latency. If the dynamic bus-sizing option is not exercised, the SIZ0, SIZ1, and $\overline{BE}$ control terminals can simply be hardwired to required levels to implement the port-B size selection.

The bus-matching operation is always handled in auxiliary registers, either after the data is read from FIFO1 SRAM during a port-B read cycle or before the data is written to the FIFO2 SRAM during a port-B write cycle. The following is an in-depth look at read and write accesses on port B during bus-sizing operation and the effect of sizing on the flag operation.

Read Accesses on Port B

To explain how bus sizing is implemented when performing reads from FIFO1 to port B, it helps to start with the internal memory-access architecture of a normally configured 36-bit port. Read accesses are made alternately on odd and even

memory blocks as shown in Figure 5; the interleaved architecture being necessary for high-frequency operation. As each 36-bit word is accessed, it is stored temporarily in one of the two banks of transparent latches represented by TL1 and TL2 in Figure 5. These are multiplexed together and loaded alternately into the output storage registers upon each successive clock pulse. All memory accesses are full-length 36-bit words and each valid read clock produces a full 36-bit word at the outputs.

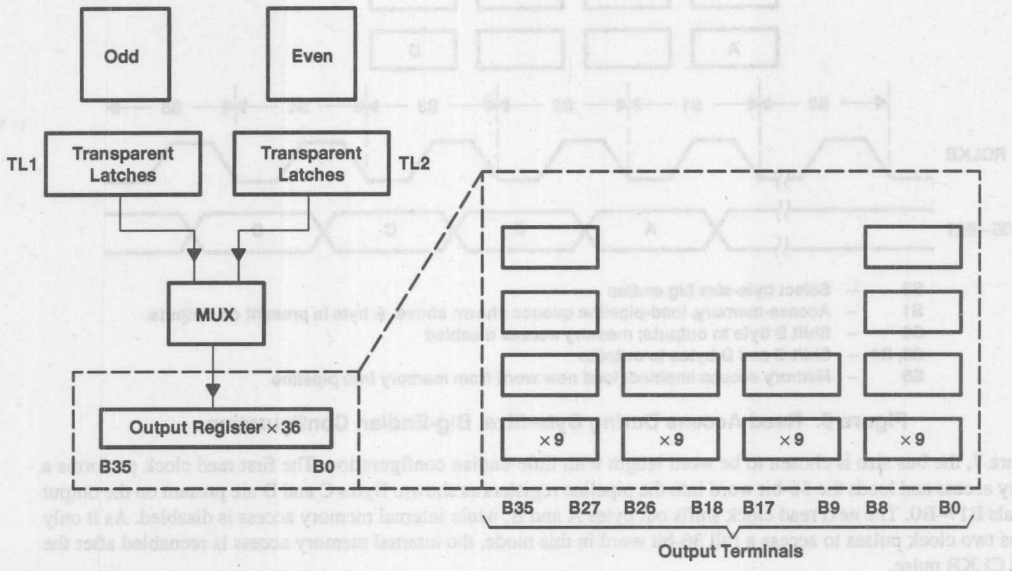
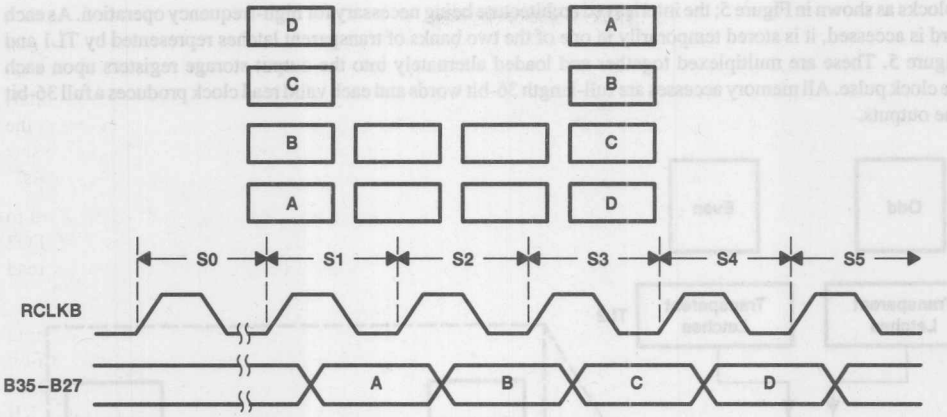


Figure 5. Pipeline Registers

Regardless of bus size, bus swap, or port selection, all internal memory-access operations are based on full 36-bit words and the associated internal flag status also reflects that basis.

To implement bus sizing, the single bank of output storage registers is replaced with multiple queues of 9-bit pipeline registers as shown in Figure 5. When a read access is performed, a full 36-bit word is loaded in groups of nine into these pipeline registers. The location of each byte is specifically loaded and controlled by the state of the port configuration (SIZ0, SIZ1, SW1, SW0, and $\overline{BE}$) terminals. Depending on the size selected, successive read-clock pulses shift out the remaining bytes in each pipeline register. During this time, internal reads from the FIFO1 memory are disabled until the last word or byte is clocked out, which is implemented by a small programmable counter. The counter counts four clock cycles in byte-size mode and two clock pulses when word size is selected. The counter is disabled for normal long-word operation. Figures 6 and 7 show how bus sizing works in practice for read operations on port B.

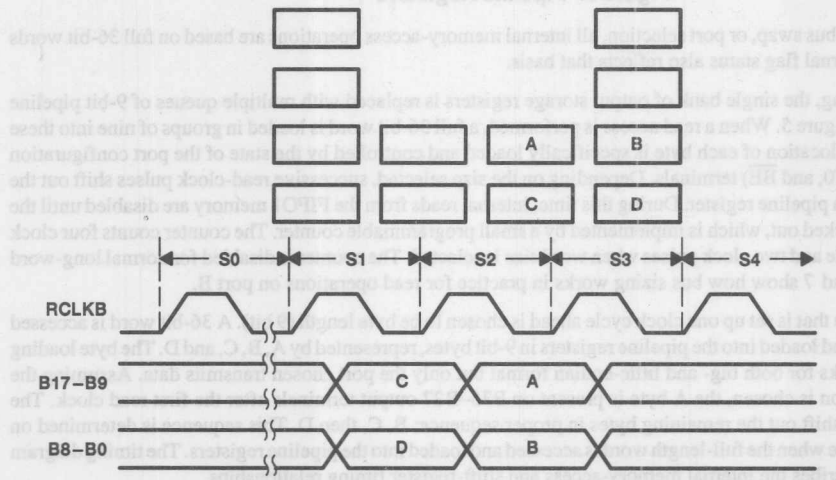
In Figure 6, the bus size that is set up one clock cycle ahead is chosen to be byte length (9 bit). A 36-bit word is accessed from FIFO1 memory and loaded into the pipeline registers in 9-bit bytes, represented by A, B, C, and D. The byte loading shown in Figure 6 works for both big- and little-endian format but only the port chosen transmits data. Assuming the big-endian configuration is chosen, the A byte is present on B35–B27 output terminals after the first read clock. The next three read clocks shift out the remaining bytes in proper sequence; B, C, then D. This sequence is determined on the first read-clock pulse when the full-length word is accessed and loaded into the pipeline registers. The timing diagram shown in Figure 6 describes the internal memory-access and shift-register timing relationships.



S0 – Select byte-size big endian
S1 – Access-memory, load-pipeline queues shown above. A byte is present on outputs.
S2 – Shift B byte to outputs; memory access disabled
S3, S4 – Shift C and D bytes to outputs
S5 – Memory access enabled; load new word from memory into pipeline

Figure 6. Read Access During Byte-Size, Big-Endian Configuration

In Figure 7, the bus size is chosen to be word length with little-endian configuration. The first read clock performs a memory access and loads the 36-bit word into the pipeline registers as shown. Bytes C and D are present on the output terminals B17–B0. The next read clock shifts out bytes A and B, while internal memory access is disabled. As it only requires two clock pulses to access a full 36-bit word in this mode, the internal memory access is reenabled after the second CLKB pulse.



S0 – Select word-size little endian
S1 – Access-memory, load-pipeline queues as shown above. C and D bytes appear on outputs.
S2 – Shift A and B bytes to outputs; memory access disabled
S3 – Memory access enabled; load new word from memory into pipeline

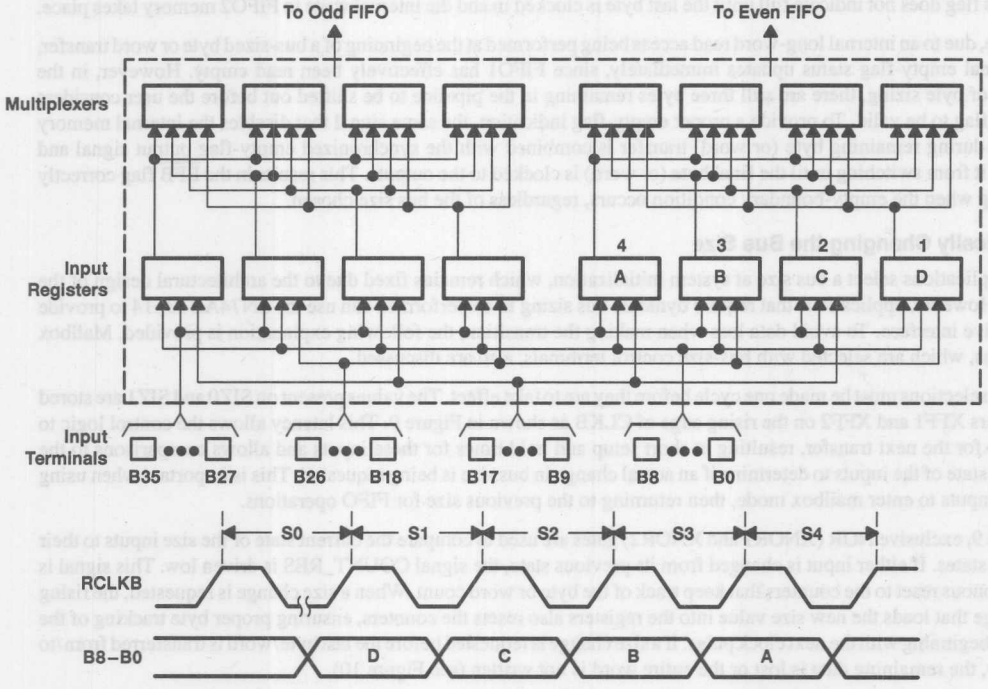
Figure 7. Read Access During Word-Size, Little-Endian Configuration

Write Operation to Port B

When writing to FIFO2, data at the input terminals is stored in one of two sets of input registers on the rising edge of CLKB and transferred into either the odd or even FIFO2 memory array. To accommodate varying bus sizes, each set is divided into four groups of nine registers. Each group of nine can accept input data from any of the nine input terminals as shown in Figure 8. Upon the rising edge of CLKB, data from the selected group of input pins is steered to the appropriate group of nine registers and stored. The group of input pads used and the location in which the successive bytes are stored in the registers are controlled by the state of the port configuration (SIZ0, SIZ1, and $\overline{BE}$) terminals.

Depending on the size selected, either one, two, or four valid CLKB pulses are needed to load a full 36-bit word to memory. Only when the last byte/word is loaded into its group(s) of registers is the full 36-bit word written to the FIFO2 memory array. Until that time, writes to the memory are disabled. A separate counter, similar to the one used for read operations, keeps track of the number of bytes loaded and when to write to the array.

The following example shows how this works in practice: Byte-size and little-endian configurations are selected. Input pads B0–B8 accept data written to FIFO2. Assuming a byte order from MSB to LSB of A, B, C, and D for the full 36-bit word to be written to FIFO2, the bytes need to appear in succession on the active input terminals in the order of D, C, B, and A. Figure 8 shows the position in the groups of registers that each byte occupies when loaded. On the fourth CLKB pulse, which loads the A byte, the data in the four groups of registers is written into FIFO2 memory array.



S0 – Select byte-size little endian
S1 – Write byte D at position 1; writes to FIFO disabled
S2 – Write byte C at position 2; writes to FIFO disabled
S3 – Write byte B at position 3; writes to FIFO disabled
S4 – Write byte A at position 4; load full 36-bit long word to memory

Figure 8. Input Registers and Timing for Write Operation During Byte-Size, Little-Endian Configuration

Effect on Status Flags

Bus sizing affects the operation of the almost-empty ($\overline{AEB}$) and almost-full ($\overline{AFB}$) flags associated with port B and, to some degree, the empty ($\overline{EFB}$) and full ($\overline{FFB}$) flags. The almost-empty and almost-full flags can be programmed to one of the preset values of 4, 8, 12, or 16 during device reset. These depths are based on full 36-bit words. When used with bus sizing, the internal flag still reacts to the programmed depth to a multiple of the byte or word size selected. For example, if a depth of eight long words is programmed and byte sizing is selected, the $\overline{AEB}$ flag indicates when there are 32 bytes remaining to be read from FIFO1 before it goes empty. This results from the internal flag reacting to eight long words remaining in the memory. Due to the byte size being selected, it takes 32 read-clock pulses to unload them. Similarly, if a depth of four long words is programmed and a bus size of 18-bit words is selected, the $\overline{AFB}$ flag reacts when there are eight more valid CLKB pulses before FIFO2 is written full. This is based on the need for two write-clock pulses to load each long word into memory and the internal flag reacting when there are four available locations remaining in the memory.

The empty and full flags for port B still indicate when the associated boundary condition is met during sizing operations because the internal flags for FIFO1 and FIFO2 are based on 36-bit words only. The write to FIFO2 memory during bus-size mode occurs on the last byte or word of the full 36-bit word being loaded. This means $\overline{FFB}$ does not indicate a full condition until all four 9-bit bytes (or both 18-bit words) of the last full long word are clocked into FIFO2. If, for instance, only three of the bytes are loaded during byte sizing, the internal write to memory has not occurred yet, and the status flag does not indicate full until the last byte is clocked in and the internal write to FIFO2 memory takes place.

Likewise, due to an internal long-word read access being performed at the beginning of a bus-sized byte or word transfer, the internal empty-flag status updates immediately, since FIFO1 has effectively been read empty. However, in the instance of byte sizing, there are still three bytes remaining in the pipeline to be shifted out before the user considers the $\overline{EFB}$ flag to be valid. To provide a proper empty-flag indication, the same signal that disables the internal memory accesses during remaining byte (or word) transfer is combined with the synchronized empty-flag output signal and prevents it from switching until the final byte (or word) is clocked to the outputs. This results in the $\overline{EFB}$ flag correctly indicating when the empty-boundary condition occurs, regardless of the bus size chosen.

Dynamically Changing the Bus Size

Many applications select a bus size at system initialization, which remains fixed due to the architectural design of the system. However, applications that require dynamic bus sizing to be performed can use the SN74ABT3614 to provide an effective interface. To avoid data loss when making the transition, the following explanation is provided. Mailbox operations, which are selected with bus-size control terminals, also are discussed.

Bus-size selections must be made one cycle before they are to take effect. The values present on SIZ0 and SIZ1 are stored in registers XFF1 and XFF2 on the rising edge of CLKB as shown in Figure 9. This latency allows the control logic to be set up for the next transfer, resulting in short setup and hold times for these inputs and allows comparisons to the previous state of the inputs to determine if an actual change in bus size is being requested. This is important when using the size inputs to enter mailbox mode, then returning to the previous size for FIFO operations.

In Figure 9, exclusive NOR (XNOR1 and XNOR2) gates are used to compare the current state of the size inputs to their previous states. If either input is changed from its previous state, the signal COUNT_RES is driven low. This signal is a synchronous reset to the counters that keep track of the byte or word count. When a size change is requested, the rising clock edge that loads the new size value into the registers also resets the counters, ensuring proper byte tracking of the new size beginning with the next clock pulse. If a size change is requested before the last byte/word is transferred from/to the FIFO, the remaining data is lost or the entire word is not written (see Figure 10).

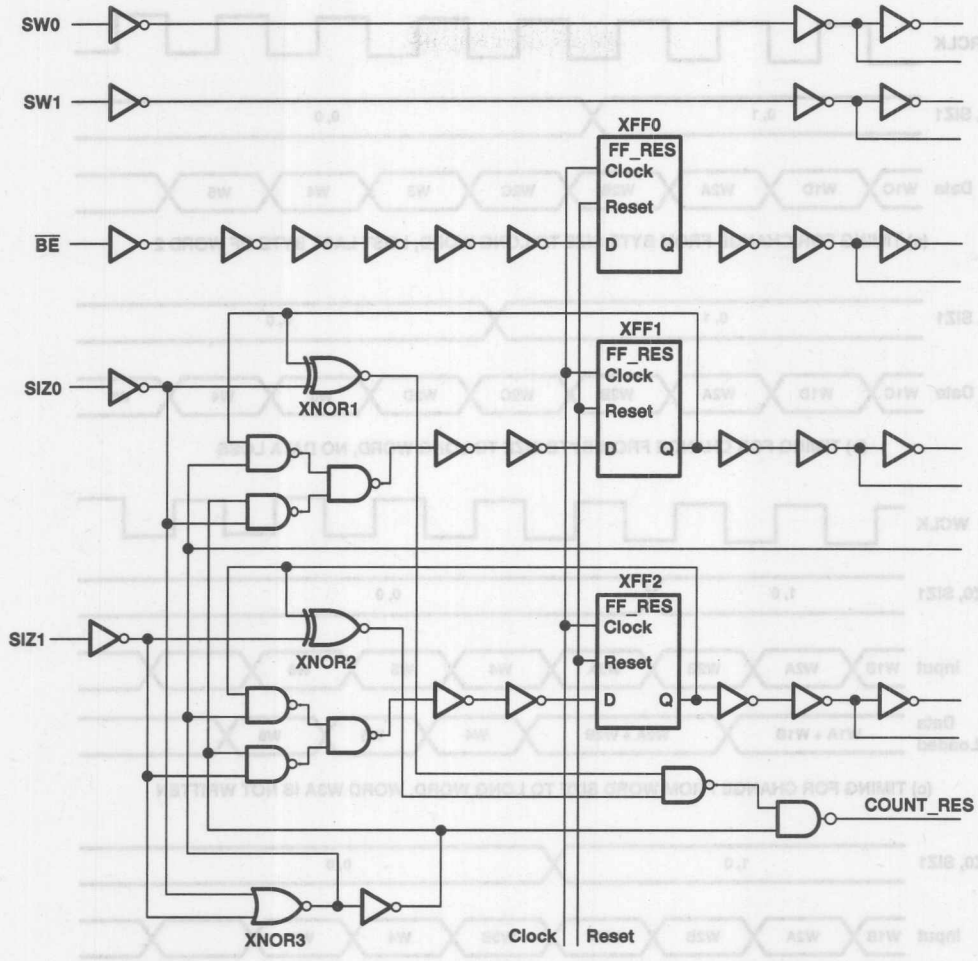


Figure 9. Size-Control Block

In the special case of mailbox operations, which use the size inputs to select mailbox mode on port B, it is essential not to interpret this as a change in bus size. When SIZ1 and SIZ0 inputs are driven high (mailbox mode), COUNT_RES is disabled (along with the counters) and the size registers are not updated (see XNOR2 in Figure 9). This allows mail operations to take place without disturbing any data transfers to/from the FIFO.

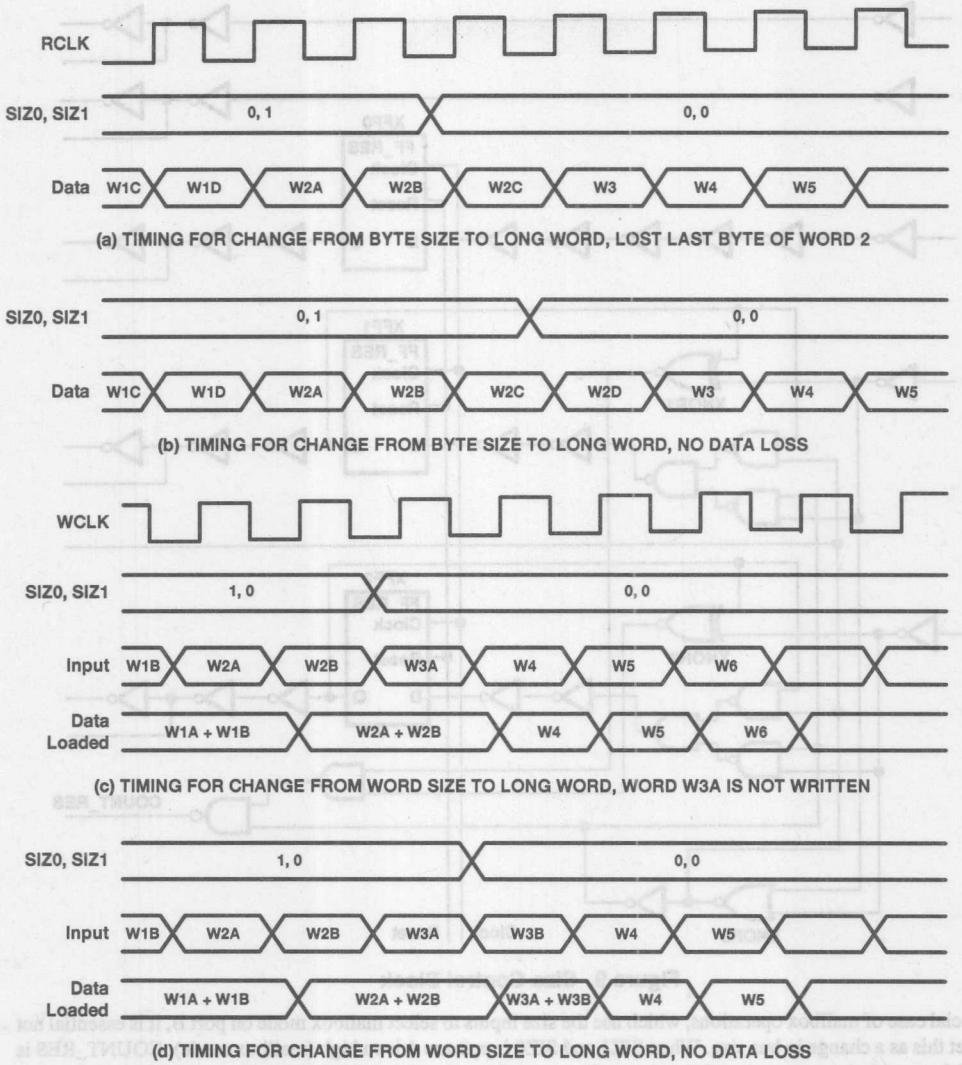


Figure 10. Dynamically Changing Byte-/Word-Size Transfers to Long-Word Data Transfers

Byte Swapping

Four different modes of byte-order arrangement (byte swap, word swap, byte-word swap, and no swap) can be performed with any port-B size selection. When byte swap is performed, the order of the bytes are rearranged within the long word but the bit order remains the same. The port-B swap-select (SW1 and SW0) inputs are used to achieve these byte-order arrangements. Table 2 lists the levels on the SW1 and SW0 input terminals and the respective size implemented. Figure 11 shows the different schemes of byte swap.

Table 2. Control of Byte-Swap Operation on Port B Using SW1 and SW0

SW1	SW0	BUS CONFIGURATION
L	L	No swap
L	H	Byte swap
H	L	Word swap
H	H	Byte-word Swap

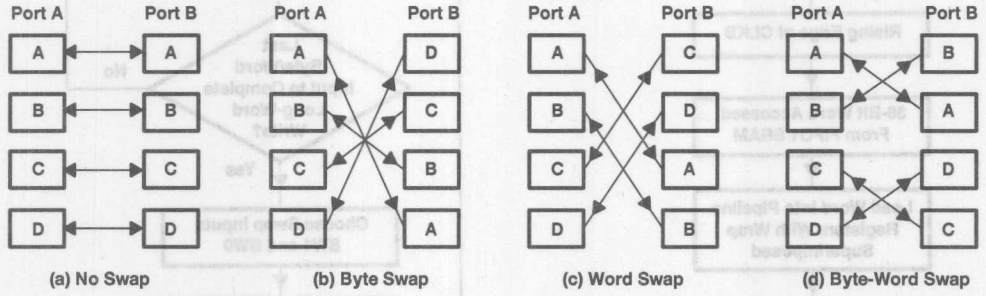


Figure 11. Byte-Swap for Long-Word-Size Data Transfers

The byte swap is performed with any port-B size selection. Byte-order arrangement is implemented by the levels on the port-B swap select inputs on a CLKB rising edge that reads a new long word from FIFO1 or writes a new long word to FIFO2. When long-word-size (36-bit) transfers are selected on port B, the byte-order arrangement can be changed on each clock cycle. On the other hand, when byte (9-bit) or word-size (18-bit) transfers are selected on port B, the byte order chosen on the first byte or word of a new long-word read from FIFO1 or written to FIFO2 is maintained until the entire long word is transferred, regardless of the swap-select input states during subsequent reads or writes. This implies that for byte- or word-sized data transfers, the byte-order arrangement can be changed only on the first byte or word data transfer of a new long-word read. Simultaneously performing a byte swap and bus size on port B results in the sequence of events shown in Figure 12.

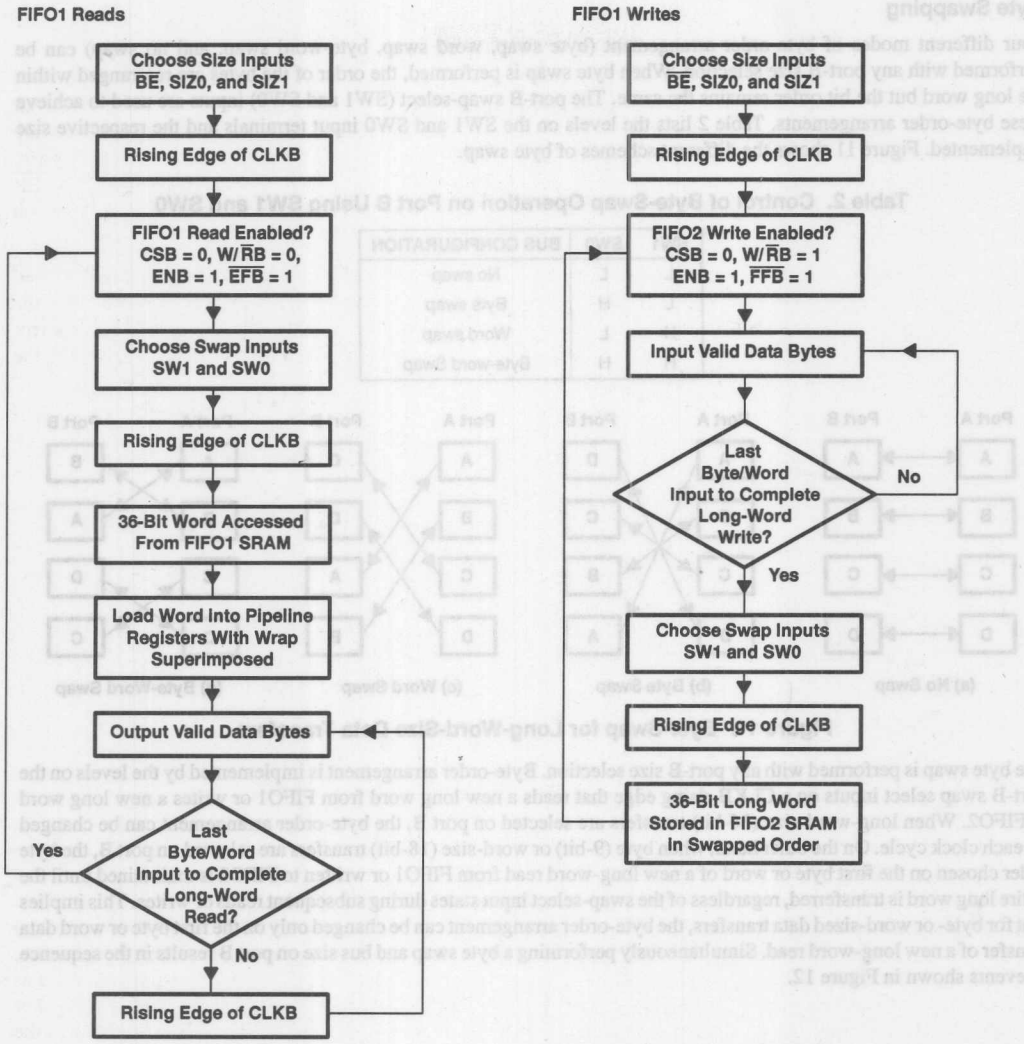


Figure 12. FIFO1 Data-Read and FIFO2 Data-Write Sequence During Simultaneous Bus-Sizing and Byte-Swapping Operations

Parity Generation and Checking

Parity Checking

The odd or even parity-checking function can be selected on both port A and port B using the ODD/$\overline{\text{EVEN}}$ input. Four parity trees examine the parity of incoming or outgoing data bytes on each port as shown in Figure 13. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit used as the parity bit. A parity error on each of these four bytes is indicated internally by a low signal on the individual-error ($\overline{\text{ER}}$) flag. These four $\overline{\text{ER}}$ outputs are combined to output a single parity-error ($\overline{\text{PEFA}}$) flag that indicates an error on one or more bytes on port A.

Similarly, port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit used as the parity bit. Again, a single parity-error ($\overline{\text{PEFB}}$) flag indicates an error on one or more bytes on port B. During the port-B sizing operation, the internal flag output for invalid data bytes is disabled; the parity-error flag indicates an error only on the bytes that are valid for the particular size selected. Parity checking on both ports is a passive operation; the port parity-error flags can be ignored if this feature is not desired.

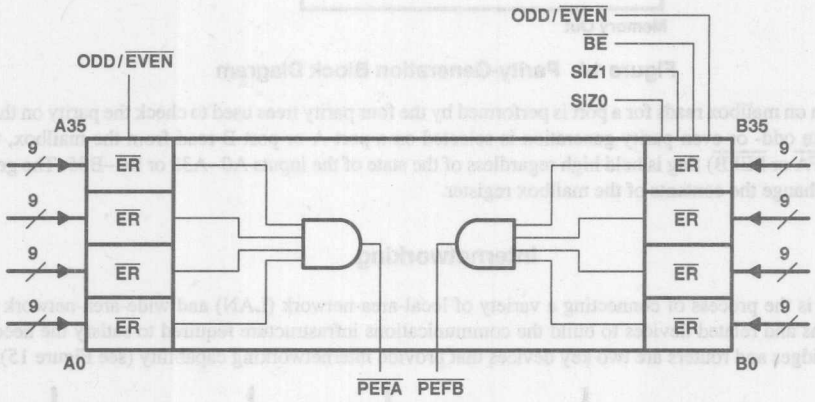


Figure 13. Parity-Checking Block Diagram

Parity Generation

Parity generation for port reads from the FIFO or mailbox can be selected using the parity-generate select-input terminal for that port (PGA or PGB). ODD/$\overline{\text{EVEN}}$ selects the type of parity generated. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit used as the parity bit. A write to the FIFO or mailbox stores all 36 bits regardless of the state of the parity generate select (PGA) input. When data is read from the FIFO, the lower eight bits of each byte are used to generate the parity bit as shown in Figure 14. If parity generation is selected (PGA = 1), the levels originally written to the most significant bits of each byte are substituted by the generated parity bit as the word is read to the outputs. Otherwise, the levels originally written to most significant bit of each byte are output.

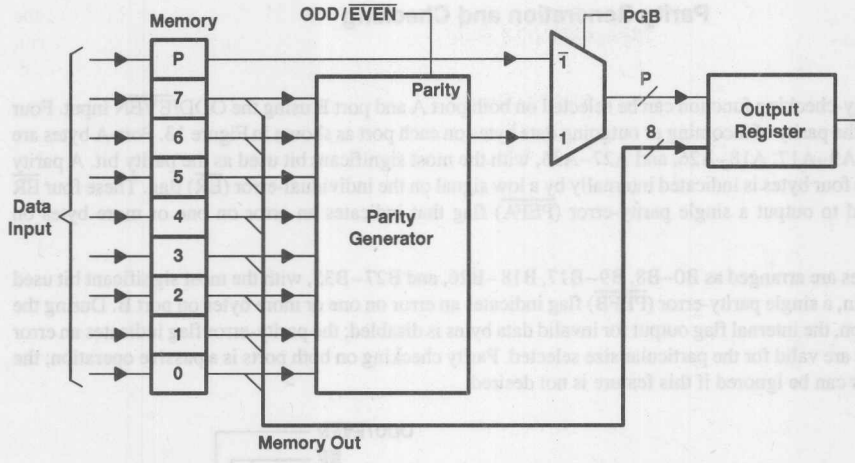


Figure 14. Parity-Generation Block Diagram

Parity generation on mailbox reads for a port is performed by the four parity trees used to check the parity on the inputs to the port. When odd- or even-parity generation is selected on a port-A or port-B read from the mailbox, the port parity-error ($\overline{\text{PEFA}}$ or $\overline{\text{PEFB}}$) flag is held high regardless of the state of the inputs A0–A35 or B0–B35. The generated parity does not change the contents of the mailbox register.

Internetworking

Internetworking is the process of connecting a variety of local-area-network (LAN) and wide-area-network (WAN) computer systems and related devices to build the communications infrastructure required to satisfy the needs of an organization. Bridges and routers are two key devices that provide internetworking capability (see Figure 15).

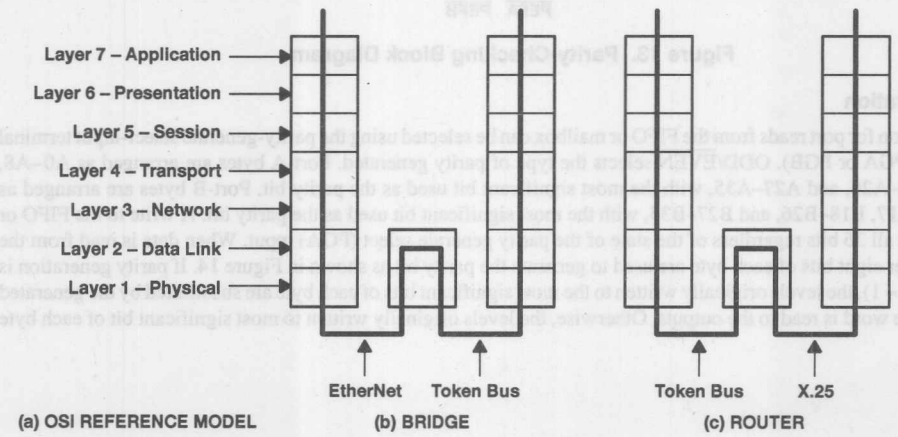


Figure 15. Bridge and Router Devices

Bridge and router designs are critical in meeting the increasing bandwidth requirements and volume of data transfer in existing network elements. The use of FIFOs in these designs provides a viable means for improving the system performance. The FIFOs provide a link between the communications processors and buses operating at different speeds and data widths. The handshaking signals for control can provide operating speeds that match the bus-communication speeds.

A bridge operates at the data-link layer (layer 2) in the OSI model to connect two similar LANs. A bridge reads the destination address contained on each incoming packet and uses the address to transmit the packets or to ignore them. This process is known as address filtering. An example of a bridge design using multiple FIFOs is shown in Figure 16.

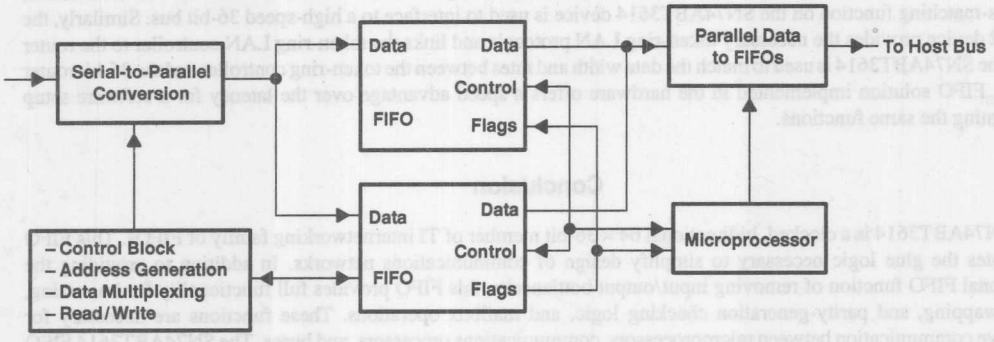


Figure 16. Implementation of a Bridge Using FIFOs

A router, on the other hand, operates at the network layer (layer 3) in the OSI model and can be used to connect two different networks; therefore, a router has the added complexity to perform frame conversion in addition to address filtering.

For example, in the situation where devices on a WAN communicate with the devices on a token-ring LAN, the interconnecting device is required to convert HDLC frames to token-ring frames and vice versa as shown in Figure 17.

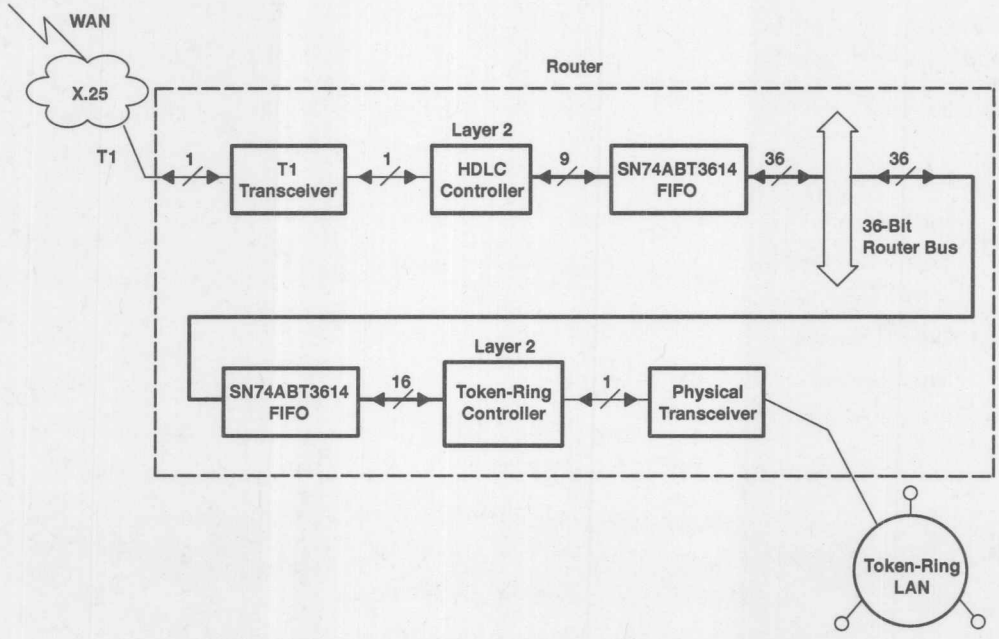


Figure 17. WAN to Token-Ring Router Using SN74ABT3614 FIFO

The layer-2 device provides the functions of flag generation and detection, zero-bit insertion and deletion, cyclic-redundancy-check (CRC) generation and detection, and abort generation and detection. The layer-2 device interfaces with the T1 transceiver on the line side. The SN74ABT3614 FIFO provides a bidirectional buffer between the layer-2 device and the high-speed router bus. In addition, if the layer-2 device has a 36-bit interface on the bus side, the bus-matching function on the SN74ABT3614 device is used to interface to a high-speed 36-bit bus. Similarly, the layer-2 device provides the necessary token-ring LAN protocols and links the token-ring LAN controller to the router bus. The SN74ABT3614 is used to match the data width and rates between the token-ring controller and the 36-bit router bus. A FIFO solution implemented in the hardware offers a speed advantage over the latency for a software setup performing the same functions.

Conclusion

The SN74ABT3614 is a clocked, bidirectional 64 × 36-bit member of TI internetworking family of FIFOs. This FIFO integrates the glue logic necessary to simplify design of communications networks. In addition to providing the traditional FIFO function of removing input/output bottlenecks, this FIFO provides full functionality for bus-sizing, byte-swapping, and parity-generation checking logic, and mailbox operations. These functions are necessary for effective communication between microprocessors, communications processors, and buses. The SN74ABT3614 FIFO can operate at frequencies up to 66 MHz and can provide data access times as fast as 11ns. The FIFO also is available in speed sorts to provide 33-MHz and 50-MHz operation.

High-Speed, High-Drive SN74ABT7819 FIFO

Teruo Ishii and Navid Madani
Advanced System Logic – Semiconductor Group

TEXAS INSTRUMENTS

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Introduction

First-in, first-out (FIFO) memories are used as high-speed data-stream buffers for maximizing throughput between buses having different data-transfer speeds, for example, between multiprocessors or a microprocessor and peripheral circuits. Recently, the processing speed of microprocessors has become so fast that the gap between the speed of the microprocessor and peripheral circuits has widened. As a result, the demand for faster FIFOs that can maximize the use of the microprocessor capabilities has increased. Usually, when a memory integrated circuit drives a heavy-load bus line, external bus buffers are required. FIFO memories, however, help to minimize the design complexity and cycle time by providing the capability to buffer data while at the same time directly driving the bus line.

The Texas Instruments SN74ABT7819 is a high-speed, high-drive, advanced BiCMOS FIFO with operating frequencies up to 80 MHz and a drive capability of $I_{OH}/I_{OL} = -12/24$ mA (see Figure 1).

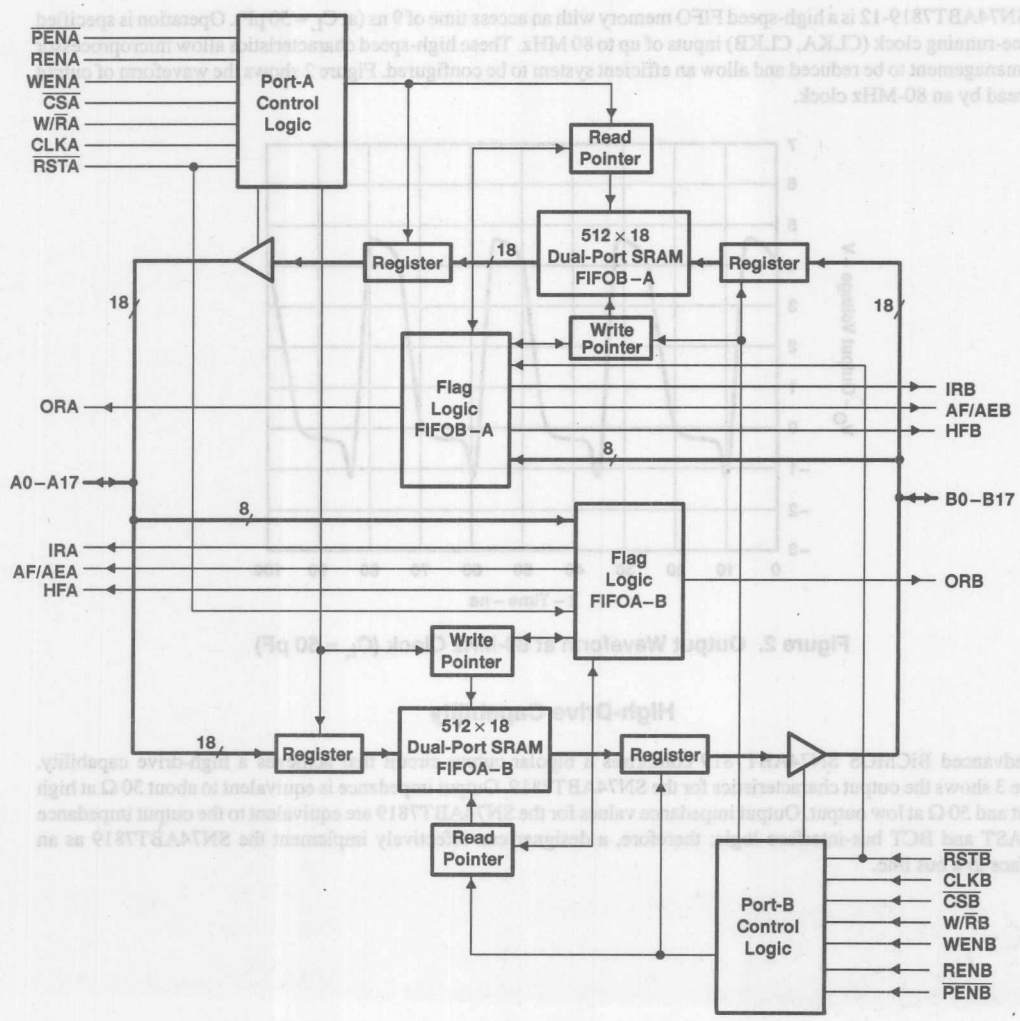


Figure 1. SN74ABT7819 Block Diagram

Structure

The SN74ABT7819 is a 512 × 18 dual-port bidirectional clocked FIFO (see Figure 1). It comprises two SRAMs (FIFOA, FIFOB), specific circuits for controlling these two SRAMs, and I/O registers. Read/write operations are carried out on the SRAMs at the low-to-high transition of their respective free-running clocks, CLKB and CLKA. Read/write operations are synchronized by independent clocks from the system. Likewise, EMPTY and FULL flags are synchronized with independent clocks from the system. Neither an external clock-enable circuit nor an external circuit for synchronizing output flags to the clocks are required. Output data is buffered by output registers and can be enabled at all times. These features facilitate design by eliminating the need for detailed timing considerations, especially in applications requiring high-speed operation.

High-Speed Performance

The SN74ABT7819-12 is a high-speed FIFO memory with an access time of 9 ns (at C_L = 50 pF). Operation is specified for free-running clock (CLKA, CLKB) inputs of up to 80 MHz. These high-speed characteristics allow microprocessor time management to be reduced and allow an efficient system to be configured. Figure 2 shows the waveform of output data read by an 80-MHz clock.

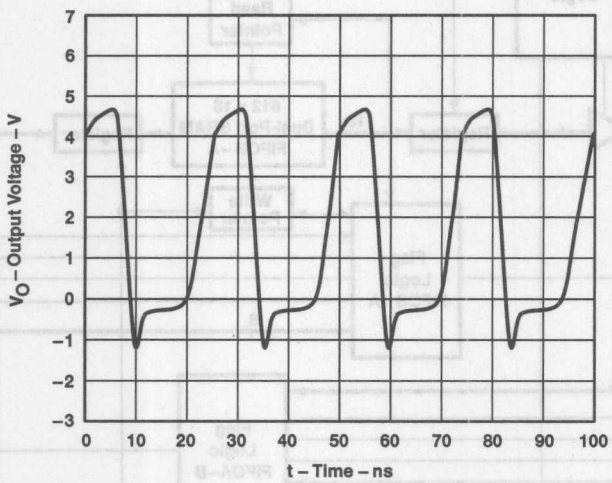


Figure 2. Output Waveform at 80-MHz Clock (C_L = 50 pF)

High-Drive Capability

The advanced BiCMOS SN74ABT7819 comprises a bipolar-output circuit that achieves a high-drive capability. Figure 3 shows the output characteristics for the SN74ABT7819. Output impedance is equivalent to about 30 Ω at high output and 50 Ω at low output. Output impedance values for the SN74ABT7819 are equivalent to the output impedance for FAST and BCT bus-interface logic; therefore, a designer can effectively implement the SN74ABT7819 as an interface to a bus line.

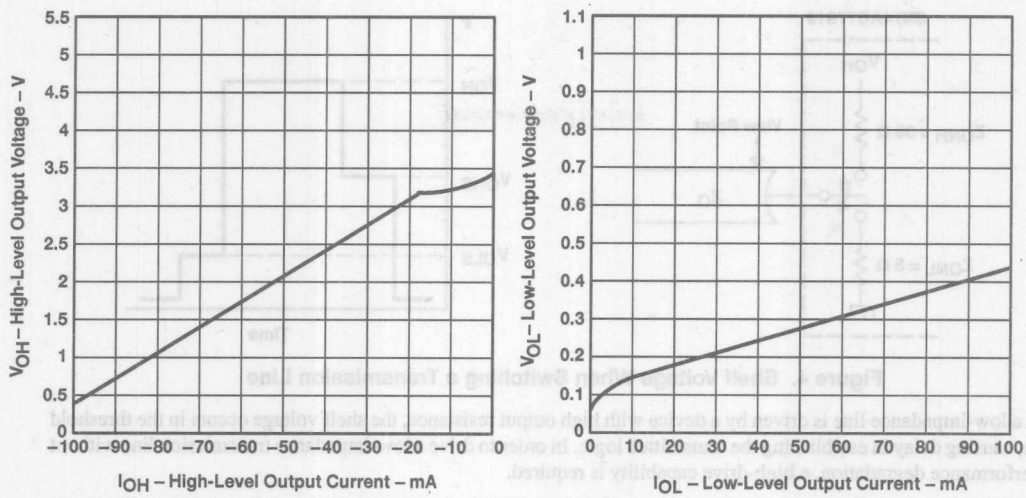


Figure 3. Output Characteristics of the SN74ABT7819 (V_{CC} = 5 V, T_A = 25°C)

Incident-Wave Switching Capability

When specific data (rectangular wave) is carried over the transmission line, data is influenced by the impedance of the transmission line, introducing distortion in the data waveforms. This distortion can cause a mismatch in required data-transfer speed; therefore, the characteristic impedance of the transmission line must be considered in the system design. The following describes the relationship between the output characteristics of the SN74ABT7819 and the transmission line.

The impedance of the transmission line and the drive capability of the device can introduce distortion in the waveforms at the low-to-high and high-to-low transition referred to as shelf voltage. The shelf voltage lowers as the impedance of the transmission line and the drive capability of the device decrease. The shelf voltage is expressed by the following equations and is shown in Figure 4.

$$V_{OHS} = \frac{Z_O}{Z_{ONH} \times Z_O} \times V_{OH} \quad \text{(a low-to-high transition)} \quad (1)$$

$$V_{OLS} = \frac{Z_{ONL}}{Z_O \times Z_{ONL}} \times V_{OH} \quad \text{(a high-to-low transition)} \quad (2)$$

Where:

V_{OHS} = Shelf voltage at the low-to-high transition (V)
V_{OLS} = Shelf voltage at the high-to-low transition (V)
V_{OH} = High output voltage of device (V)
Z_{ONH} = High output on resistance of device (Ω)
Z_{ONL} = Low output on resistance of device (Ω)
Z_O = Impedance of transmission line (Ω)

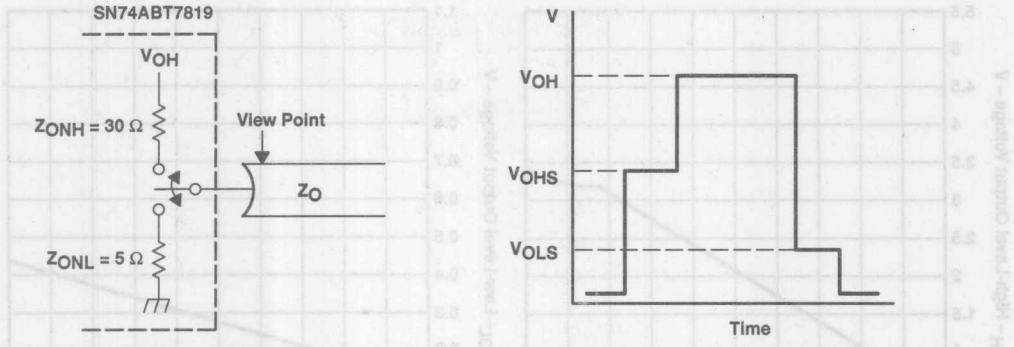


Figure 4. Shelf Voltage When Switching a Transmission Line

When a low-impedance line is driven by a device with high output resistance, the shelf voltage occurs in the threshold region, causing delay in establishing the transmitted logic. In order to drive a low-impedance transmission line without any performance degradation, a high-drive capability is required.

On the bus lines of backplanes or memories, the impedance of the transmission line drops as load capacitance is distributed over the transmission line. Generally, the characteristic impedance and the propagation delay time of the transmission line are shown by the following equations:

$$Z_O = \sqrt{\frac{L_O}{C_O}} \tag{3}$$

$$t_{pd} = \sqrt{C_O \times L_O} \tag{4}$$

Where:

Z_O = Impedance of transmission line (Ω)
L_O = Impedance per unit length (H)
C_O = Capacitance per unit length (F)
t_{pd} = Propagation delay time of transmission line (s/m)

When the load capacitance is applied on the transmission line, the characteristic impedance and the propagation delay time of the transmission line are changed as follows:

$$Z' = \sqrt{\frac{L_O}{C_O + C_l}} + \frac{Z_O}{\sqrt{1 + \frac{C_l}{C_O}}} \tag{5}$$

$$t_{pd}' = \sqrt{L_O \times (C_O + C_l)} = t_{pd}\sqrt{1 + \frac{C_l}{C_O}} \tag{6}$$

Where:

Z' = Impedance after application of capacitance (Ω)
t_{pd}' = Propagation delay time after application of capacitance (s/m)
C_l = Applied capacitance (F)

Example

The effect of loading a $Z_O = 100\ \Omega$ and $t_{pd} = 7$ ns transmission line with 8-pf loads equally spaced at 3-cm intervals is calculated in equations 7 and 8. The high- and low-output impedance necessary to drive the loaded transmission line with no settling time delay is calculated in equations 9 and 10.

From equations 3 and 4:

$$L_O = Z_O \times t_{pd} = 100 \times 7 \times 10^{-9} = 700 \text{ nH/m} = 21 \text{ nH/3cm}$$

$$C_O = t_{pd}/Z_O = 7 \times 10^{-9}/100 = 70 \text{ pF/m} = 2.1 \text{ pF/3cm}$$

Substituting for C_O in equations 5 and 6:

$$Z_O' = \frac{Z_O}{\sqrt{1 + \frac{C_l}{C_O}}} = \frac{100}{\sqrt{1 + \frac{8 \times 10^{-12}}{2.1 \times 10^{-12}}}} = 45.6\ \Omega \quad (7)$$

$$t_{pd}' = t_{pd}\sqrt{1 + \frac{C_l}{C_O}} = 7 \times 10^{-9}\sqrt{1 + \frac{8 \times 10^{-12}}{2.1 \times 10^{-12}}} = 15.4 \text{ ns/m} \quad (8)$$

The values calculated by equations 7 and 8 are $Z_O' = 45.6\ \Omega$ and $t_{pd}' = 15.4$ ns/m, respectively. The propagation delay time of the transmission line is about doubled, and the impedance of the transmission line is about halved. The output impedance required of a device to drive this transmission line without a settling time delay is calculated by the following equations:

(high-output impedance)

$$2 \le \frac{Z_O'}{Z_{ONH} + Z_O} \times V_{OH} \quad (9)$$

$$2 \le \frac{45.6}{Z_{ONH} + 45.6} \times 3.5$$

$$Z_{ONH} \le 34.2\ \Omega$$

(low-output impedance)

$$0.8 \ge \frac{Z_{ONL}}{Z_O' + Z_{ONL}} \times V_{OH} \quad (10)$$

$$0.8 \ge \frac{Z_{ONL}}{45.6 + Z_{ONL}} \times 3.5$$

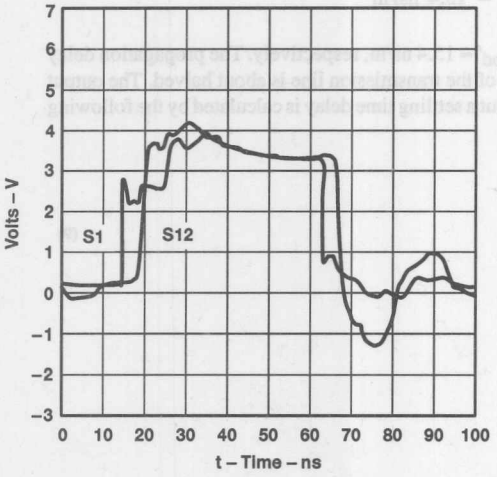
$$Z_{ONL} \le 13.5\ \Omega$$

The transmission line must be driven by a device having an output impedance of 34 Ω or less at high output and 13 Ω at low output; therefore, this transmission line can be driven with the SN74ABT7819.

VME Backplane Drive

Since the drive performance of almost all memory integrated circuits is low, it has been difficult to drive memory lines or backplane buses directly; therefore, external bus buffers have been required to interface a memory to a bus driver. Now the SN74ABT7819 allows direct driving of medium-scale bus lines.

Figure 5 shows the waveform of a 12-slot VME backplane driven by an SN74ABT7819 FIFO from the line end. Although waveform distortion caused by multiple reflection due to the 3-cm stub length and DIN connector occurs, there is no influence of reflection in the threshold region; therefore, when the SN74ABT7819 drives the VME backplane from the end, direct driving is possible. However, when the 12-slot VME bus is driven from the center, the backplane line is regarded as a branch pattern and the impedance becomes one-half the impedance at that point, resulting in generation of a step in the threshold region (see Figure 6). For this reason, a bus buffer having a higher drive capability is required.



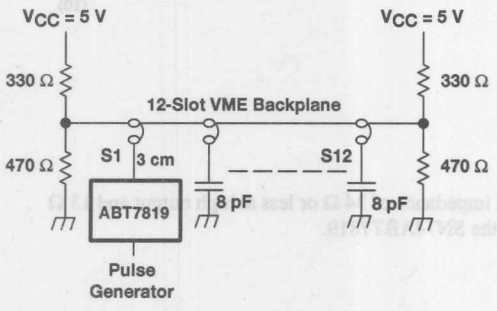
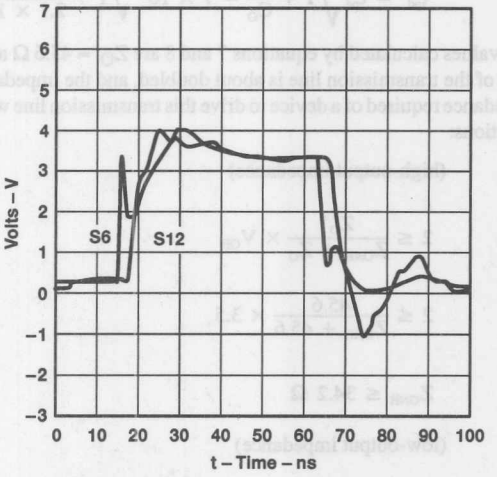


Figure 5. Backplane Driven From End



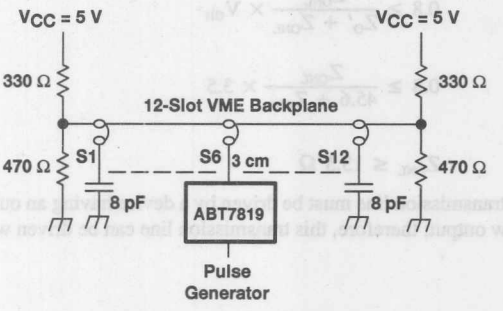


Figure 6. Backplane Driven From Center

Figure 7 shows the stepped levels when the VME bus is driven from the center slot by the SN74ABT7819. The influence of multiple reflections increases and the level of the shelf approaches the threshold region as the number of slots increases (the transmission line of the backplane is optimized corresponding to the number of slots). Based on these results, a design of five or fewer slots is preferable for driving with sufficient margin to preclude unwanted delay and possible data errors.

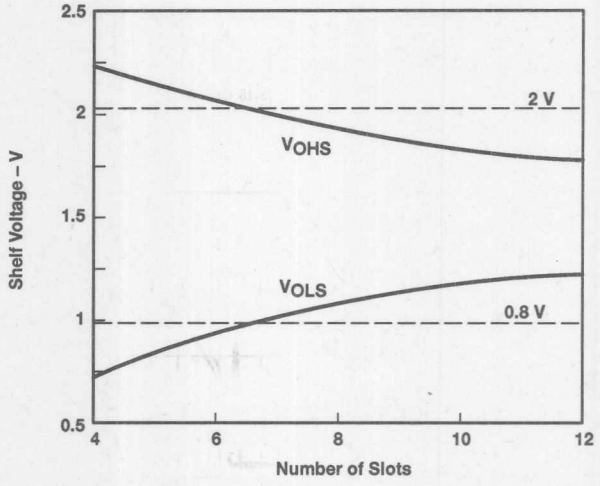


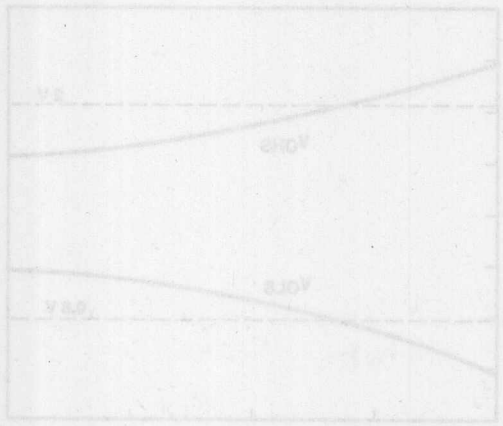
Figure 7. Number of Slots Versus Shelf Voltage (Center Drive)

Summary

The SN74ABT7819 is a high-speed, high-drive capability FIFO memory that meets the high-speed data-transfer rate requirements and drives the bus lines directly. This application report presents the essential points that a designer should consider in using a SN74ABT7819 for high-speed data transfer. The importance of drive capability and the influence of distortion is explained. Comprehending the relationship between drive capability and transmission line characteristics is essential to obtain the best performance of the SN74ABT7819.

Reference

Bus-Interface Circuits Application and Data Book, Texas Instruments Incorporated, 1990



SPARC MBus-to-Futurebus+ Bridge Using the Texas Instruments Futurebus+ Chipset

Robert Gugel
Mixed Signal Product Group

TEXAS INSTRUMENTS

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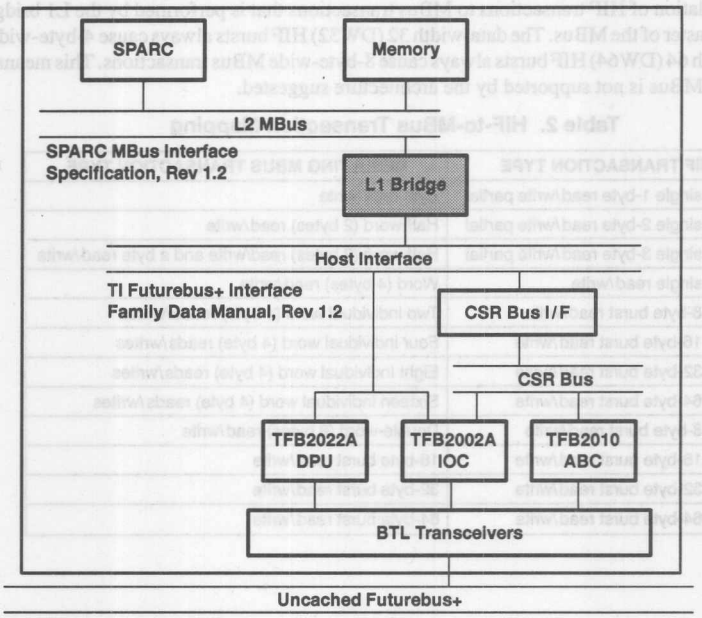
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Introduction

This application report describes the logic necessary to connect the SPARC MBus to the Texas Instruments (TI) Futurebus+ (FB+) chipset host interface (HIF). This logic is a translator of MBus transactions to HIF transactions and vice versa. The MBus-to-HIF bridge described is MBus level-1 compliant. Level-1 transactions are the noncache-coherent subset of MBus level-2 transactions. Even though level-2 transactions are occurring on the MBus, they cannot cross the L1 bridge.

Figure 1 shows a block diagram of a FB+ module featuring a SPARC processor that can access FB+. The MBus-to-HIF bridge block is highlighted. Since knowledge of FB+, the HIF, and MBus is necessary to understand this definition, references to the applicable specifications also are included in Figure 1.



NOTE: Reference IEEE P896.1 and P896.2

Figure 1. SPARC FB+

Transaction Support

A transaction originating on the MBus must be transported to the HIF and then to the FB+. This requires the L1 bridge to be a slave to MBus transactions and a master to HIF transactions. Likewise, a transaction originating from FB+ is transported to HIF and then to the MBus. In this case, the L1 bridge is a slave to HIF transactions and a master of the MBus transactions. Each of the three buses has a set of transactions that must be mapped to each other when crossing bridges.

Table 1 shows the translation of MBus transactions to HIF transaction that is performed by the L1 bridge when it is a slave to the MBus and a master of the HIF..

Table 1. MBus-to-HIF Transaction Mapping

MBUS TRANSACTION TYPE	RESULTING HIF TRANSACTION TYPE
Byte read/write	DW32 single 1-byte read/write partial
Half-word (2 bytes) read/write	DW32 single 2-byte read/write partial
Word (4 bytes) read/write	DW32 single read/write
Double word (8 bytes) read/write	DW64 8-byte burst read/write
16-byte burst read/write	DW64 16-byte burst read/write
32-byte burst read/write	DW64 32-byte burst read/write
64-byte burst read/write	DW64 64-byte burst read/write
128-byte burst read/write	Two DW64 64-byte burst reads/writes chained together with HIF MORE signal

Table 2 shows the translation of HIF transactions to MBus transactions that is performed by the L1 bridge when it is a slave to the HIF and a master of the MBus. The data-width 32 (DW32) HIF bursts always cause 4-byte-wide transactions on MBus, and data-width 64 (DW64) HIF bursts always cause 8-byte-wide MBus transactions. This means that dynamic bus sizing from HIF to MBus is not supported by the architecture suggested.

Table 2. HIF-to-MBus Transaction Mapping

HIF TRANSACTION TYPE	RESULTING MBUS TRANSACTION TYPE
DW32 single 1-byte read/write partial	Byte read/write
DW32 single 2-byte read/write partial	Half-word (2 bytes) read/write
DW32 single 3-byte read/write partial	Half-word (2 bytes) read/write and a byte read/write
DW32 single read/write	Word (4 bytes) read/write
DW32 8-byte burst read/write	Two individual word (4 byte) reads/writes
DW32 16-byte burst read/write	Four individual word (4 byte) reads/writes
DW32 32-byte burst read/write	Eight individual word (4 byte) reads/writes
DW32 64-byte burst read/write	Sixteen individual word (4 byte) reads/writes
DW64 8-byte burst read/write	Double-word (8 bytes) read/write
DW64 16-byte burst read/write	16-byte burst read/write
DW64 32-byte burst read/write	32-byte burst read/write
DW64 64-byte burst read/write	64-byte burst read/write

Bridge Architecture

Figure 2 shows suggested implementation of the MBus to HIF bridge.

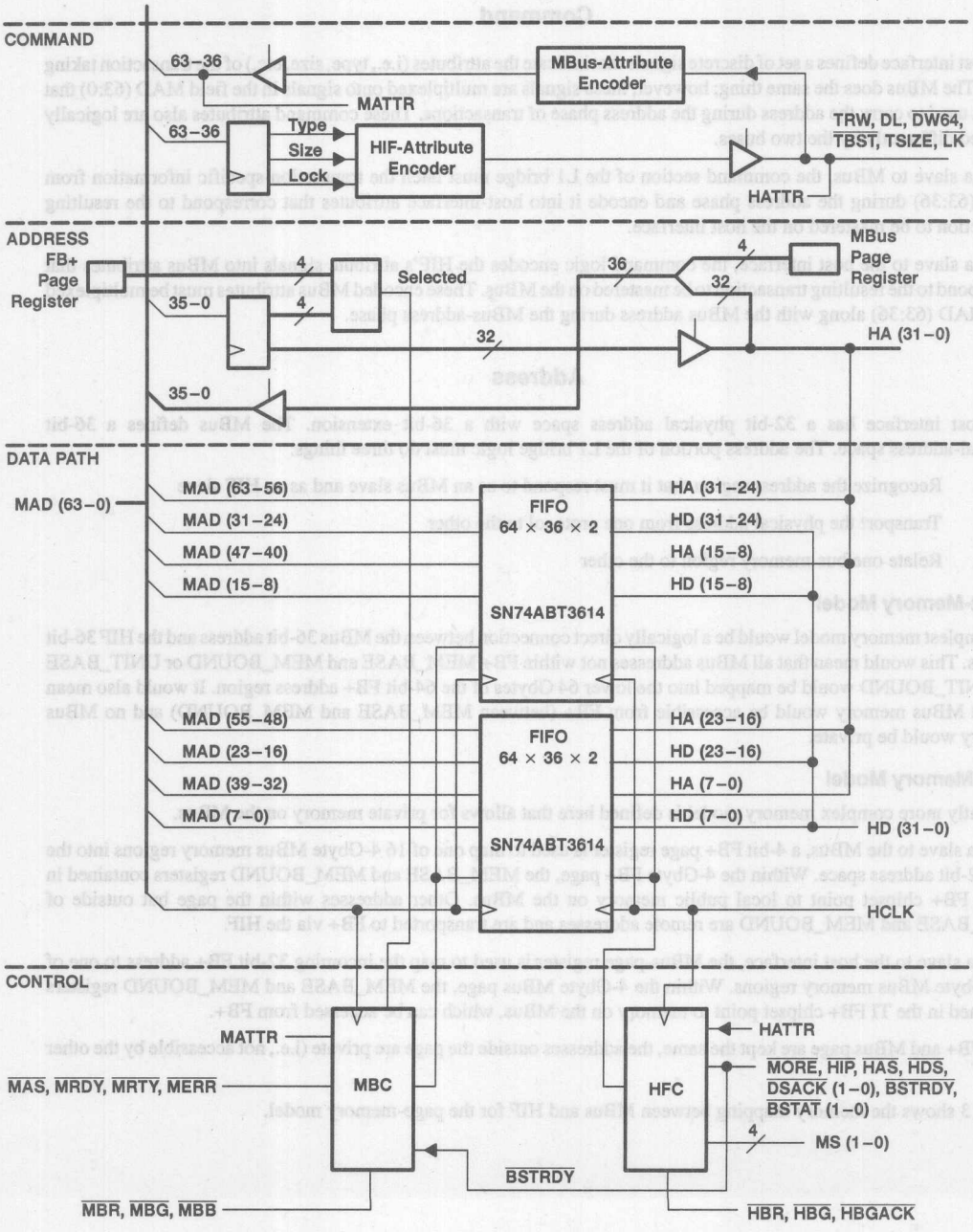


Figure 2. MBus-to-HIF Bridge

A typical bus-bridge implementation consists of command, address, datapath, and control logic. The operations of these sections in this design are as follows:

Command

The host interface defines a set of discrete signals that indicate the attributes (i.e., type, size, etc.) of the transaction taking place. The MBus does the same thing; however, these signals are multiplexed onto signals in the field MAD (63:0) that are not used to carry the address during the address phase of transactions. These command attributes also are logically encoded differently by the two buses.

When a slave to MBus, the command section of the L1 bridge must latch the transaction-specific information from MAD (63:36) during the address phase and encode it into host-interface attributes that correspond to the resulting transaction to be mastered on the host interface.

When a slave to the host interface, the command logic encodes the HIF's attribute signals into MBus attributes that correspond to the resulting transaction to be mastered on the MBus. These encoded MBus attributes must be multiplexed onto MAD (63:36) along with the MBus address during the MBus-address phase.

Address

The host interface has a 32-bit physical address space with a 36-bit extension. The MBus defines a 36-bit physical-address space. The address portion of the L1 bridge logic must do three things:

- Recognize the address region that it must respond to as an MBus slave and as an HIF slave
- Transport the physical address from one protocol to the other
- Relate one bus-memory region to the other

Direct-Memory Model

The simplest memory model would be a logically direct connection between the MBus 36-bit address and the HIF 36-bit address. This would mean that all MBus addresses not within FB+ MEM_BASE and MEM_BOUND or UNIT_BASE and UNIT_BOUND would be mapped into the lower 64 Gbytes of the 64-bit FB+ address region. It would also mean that all MBus memory would be accessible from FB+ (between MEM_BASE and MEM_BOUND) and no MBus memory would be private.

Page-Memory Model

A slightly more complex memory model is defined here that allows for private memory on the MBus.

When a slave to the MBus, a 4-bit FB+ page register is used to map one of 16 4-Gbyte MBus memory regions into the FB+ 32-bit address space. Within the 4-Gbyte FB+ page, the MEM_BASE and MEM_BOUND registers contained in the TI FB+ chipset point to local public memory on the MBus. Other addresses within the page but outside of MEM_BASE and MEM_BOUND are remote addresses and are transported to FB+ via the HIF.

When a slave to the host interface, the MBus-page register is used to map the incoming 32-bit FB+ address to one of 16 4-Gbyte MBus memory regions. Within the 4-Gbyte MBus page, the MEM_BASE and MEM_BOUND registers contained in the TI FB+ chipset point to memory on the MBus, which can be accessed from FB+.

If the FB+ and MBus page are kept the same, the addresses outside the page are private (i.e., not accessible by the other bus).

Figure 3 shows the memory mapping between MBus and HIF for the page-memory model.

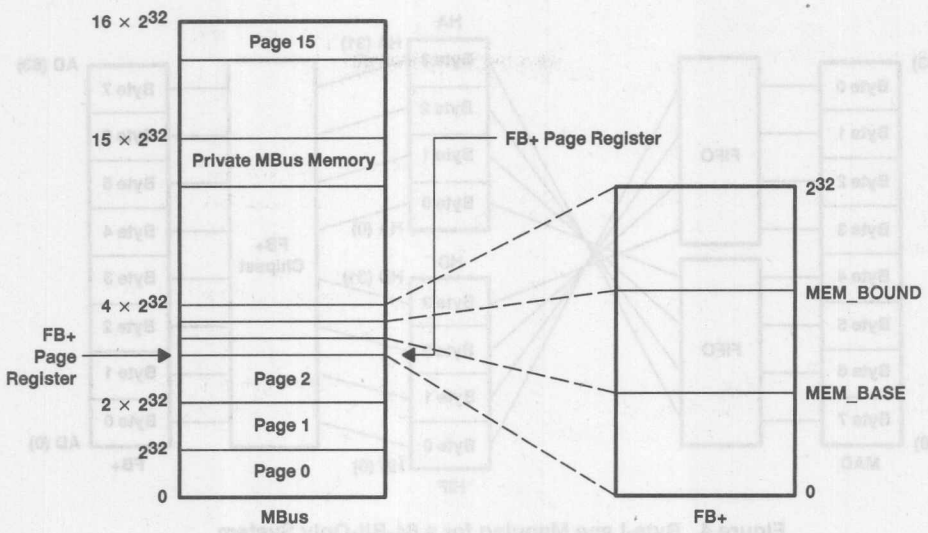


Figure 3. MBus/FB+ Memory Map

Datapath

Considerations

There are several considerations when designing the datapath interface between the MBus and the host interface.

- Since MBus runs at 40 MHz nominally and the HIF at 20–25 MHz, a FIFO is needed to synchronize the two different time domains.
- MBus has a big-endian datapath and requires that words and half words be word and byte aligned. The HIF has no endian preference with the exception of big-endian access to FB+ CSR space.
- MBus always multiplexes address and data on 64 signals; the HIF has demultiplexed address and data when the data width is 32 bits, and multiplexed address and data when the data width is 64 bits.
- MBus does 1-, 2-, 4-, and 8-byte nonburst (word) and 16-, 32-, 64-, and 128-byte burst transactions while the HIF does 1-, 2-, 3-, and 4-byte nonburst (single) and 8-, 16-, 32-, and 64-byte burst transactions. MBus bursts are always of data width 64. HIF bursts can be of data width 32 and 64.
- MBus has no parity protection on its address/data lines. The HIF address/data lines do have parity; however, the TI chipset can generate parity internally and pass it on to FB+ when sourcing data to FB+.

Taking the above considerations into account requires the use of two bidirectional FIFOs capable of being clocked at 40 MHz. These FIFOs need to be 32 bits wide and 64 words deep. They need empty/full flags, clock enables, and port-direction control. A byte-swap function within a 16-bit word also is required. The TI SN74ABT3614 is an ideal candidate.

Byte-Lane Mapping

FB+ systems require address invariant byte-lane mapping. This means that data byte 0 (the byte pointed to by byte address 0) always appears on FB+ AD (7:0). MBus systems require that data transfers of less than a double word (8 bytes) be aligned. Figure 4 shows byte-lane mapping between MBus, the FIFOs, the HIF, and FB+ for a 64-bit implementation only.

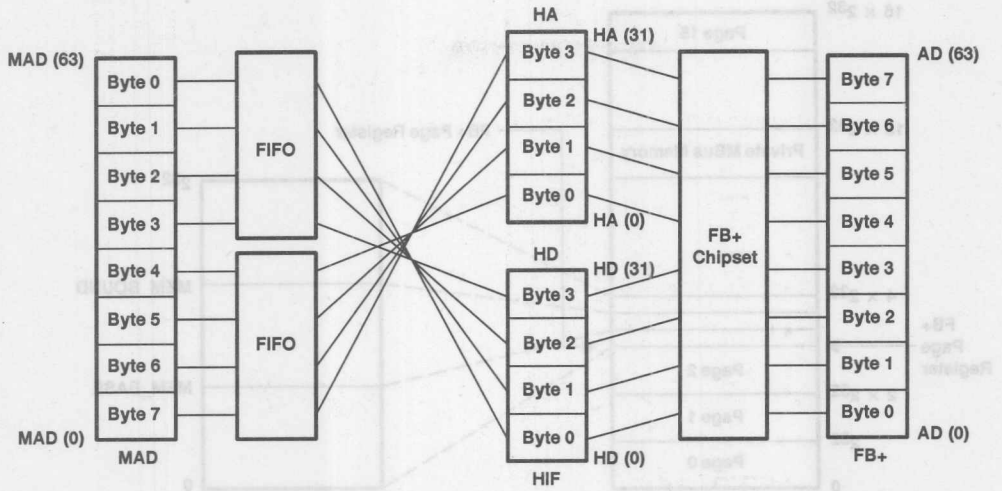


Figure 4. Byte-Lane Mapping for a 64-Bit-Only System

Since 32-bit data transfers can take place on FB+ and the HIF, quadlet (4-byte word) steering is required to correctly align 32-bit data quadlets from the HIF to those of the MBus. Quadlet steering of this type require a cross-point switch with two 32-bit ports on each end. This could be implemented with four pairs of 16-bit Widebus™ transceivers; however, this is expensive in terms of board space and datapath performance. A FIFO with the ability to swap bytes within 16-bit words performs the quadlet-steering function with the byte lanes wired as shown in Figure 5.

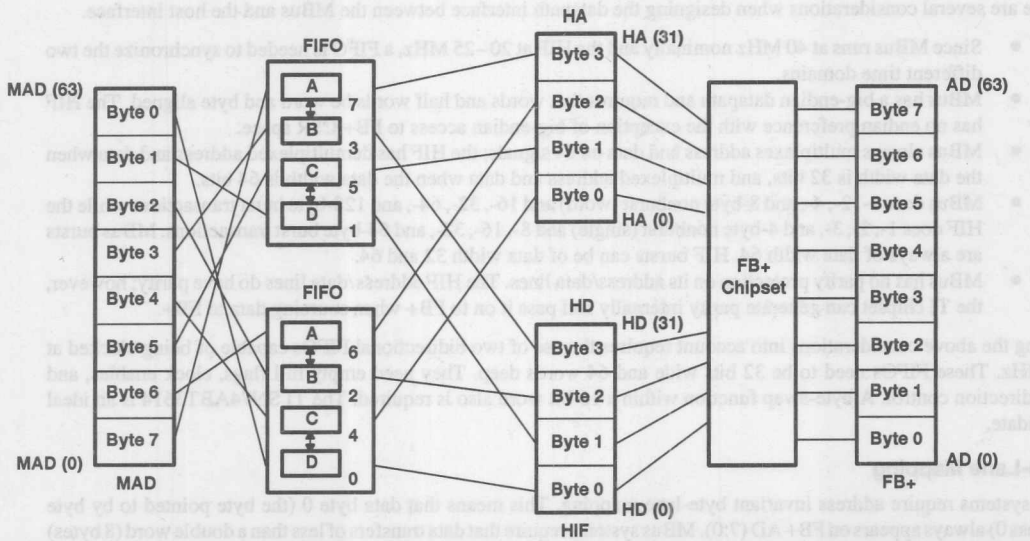


Figure 5. Byte-Lane Mapping for a 64-/32-Bit System

Widebus is a trademark of Texas Instruments Incorporated.

An example of this quadlet steering in action is the following scenario: the TI FB+ chipset is a slave to a single-beat DW64 write transaction on FB+ (8 bytes). The chipset's 64-bit HIF enable bit is not set; therefore, it performs 4-byte-wide, 8-byte burst writes onto the HIF. This HIF burst write contains two 4-byte data phases. The first data is an even-address quadlet and needs to be steered to MAD (63:32). The second data is an odd-address quadlet and needs to be steered to MAD (31:0). Figure 6 shows the datapath for the odd-address quadlet.

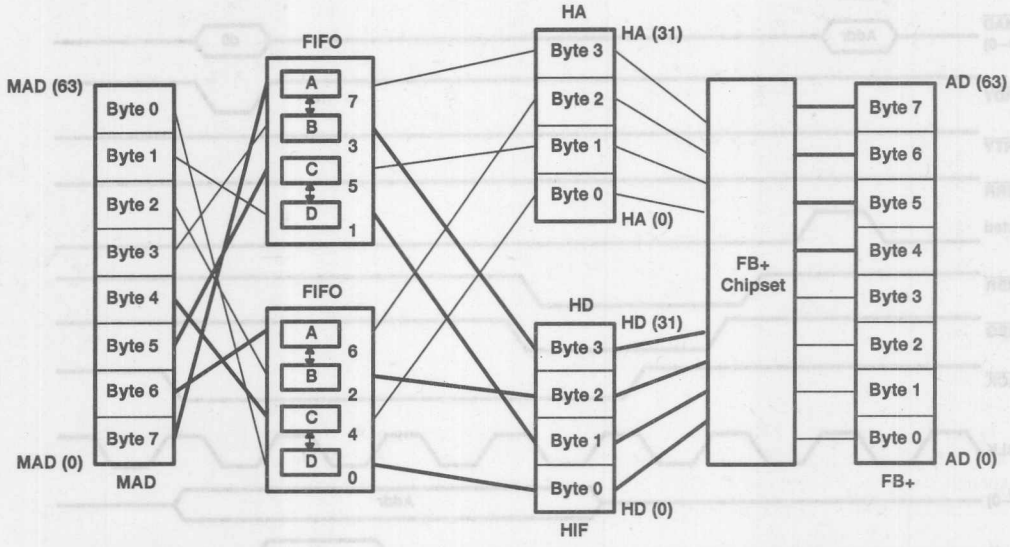


Figure 6. Byte-Lane Mapping Showing Path Taken by Address Quadlet on HD

Control Logic

The MBus controller (MBC) and host interface controller (HIFC) are synchronous state machines that operate in the two clock domains. They handle the protocols of their respective buses. They also handle arbitration protocols when bus mastership is required. These controllers drive the latch enables, 3-state controls, and FIFO control signals of the command, address, and datapath sections of the L1 bridge. They are responsible for coordinating data flow between the two buses that operate at different data rates by using the master hold-off and slave-wait capabilities of their respective buses. They also are responsible for manipulating arbitration protocols in response to locked-transaction requests.

Details of the implementation of these bus controllers is outside the scope of this application report. An example of an MBus-initiated word-read transaction resulting in an HIF single read is shown in Figure 7.

The L1 bridge is a slave to MBus and a master on the host interface. It responds to an MBus address as a selected slave and then arbitrates for HIF mastership.

Likewise , an example of an MBus-initiated word-write transaction resulting in an HIF single write is shown in Figure 8. In this case, the MBus write is acknowledged before the HIF write is complete. If another write occurs to the L1 bridge before the HIF transaction is complete, an MBus relinquish and retry operation must be performed to back off the MBus master until the HIF transaction is finished.

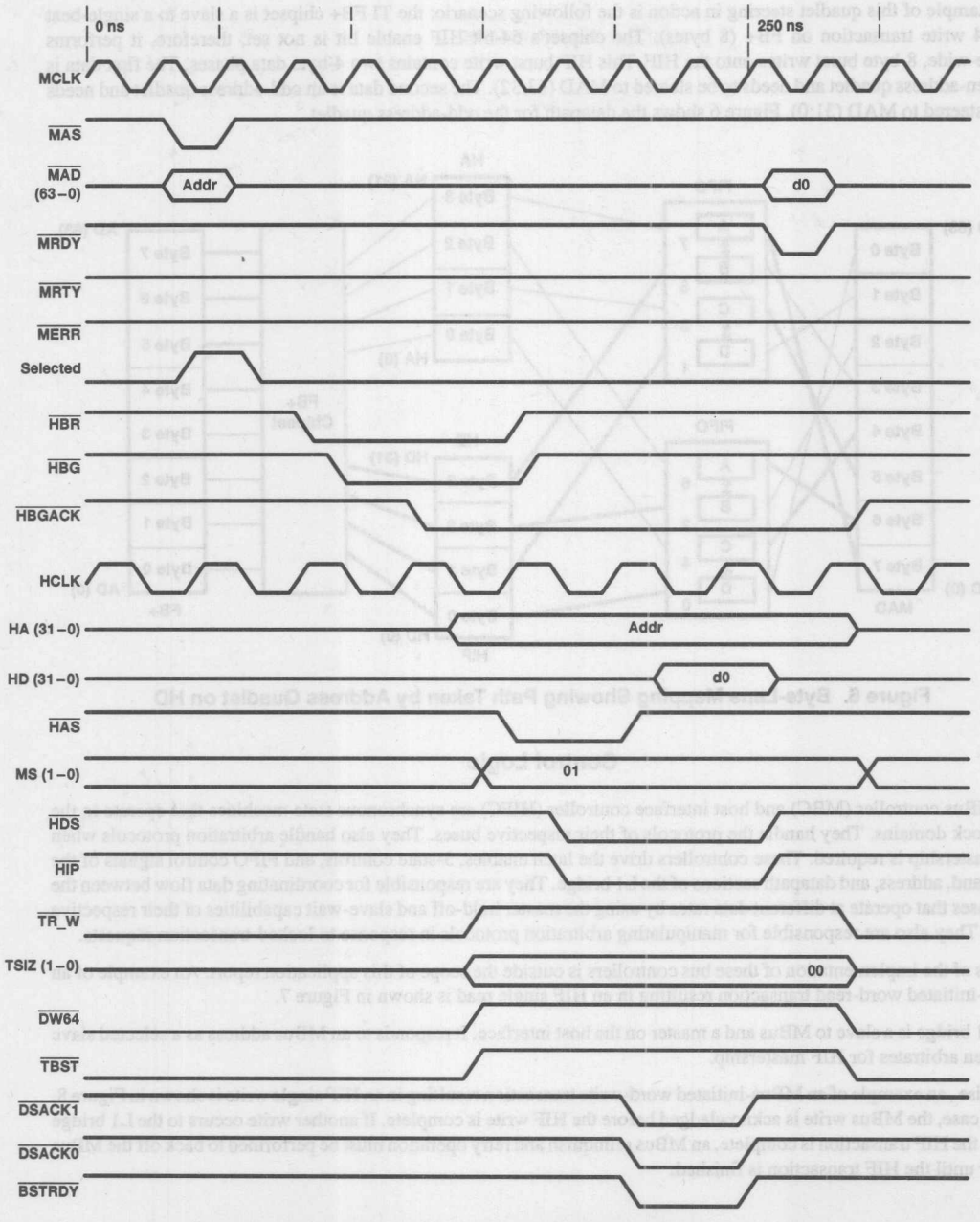


Figure 7. MBus-Word Read to HIF Single-Read Transaction

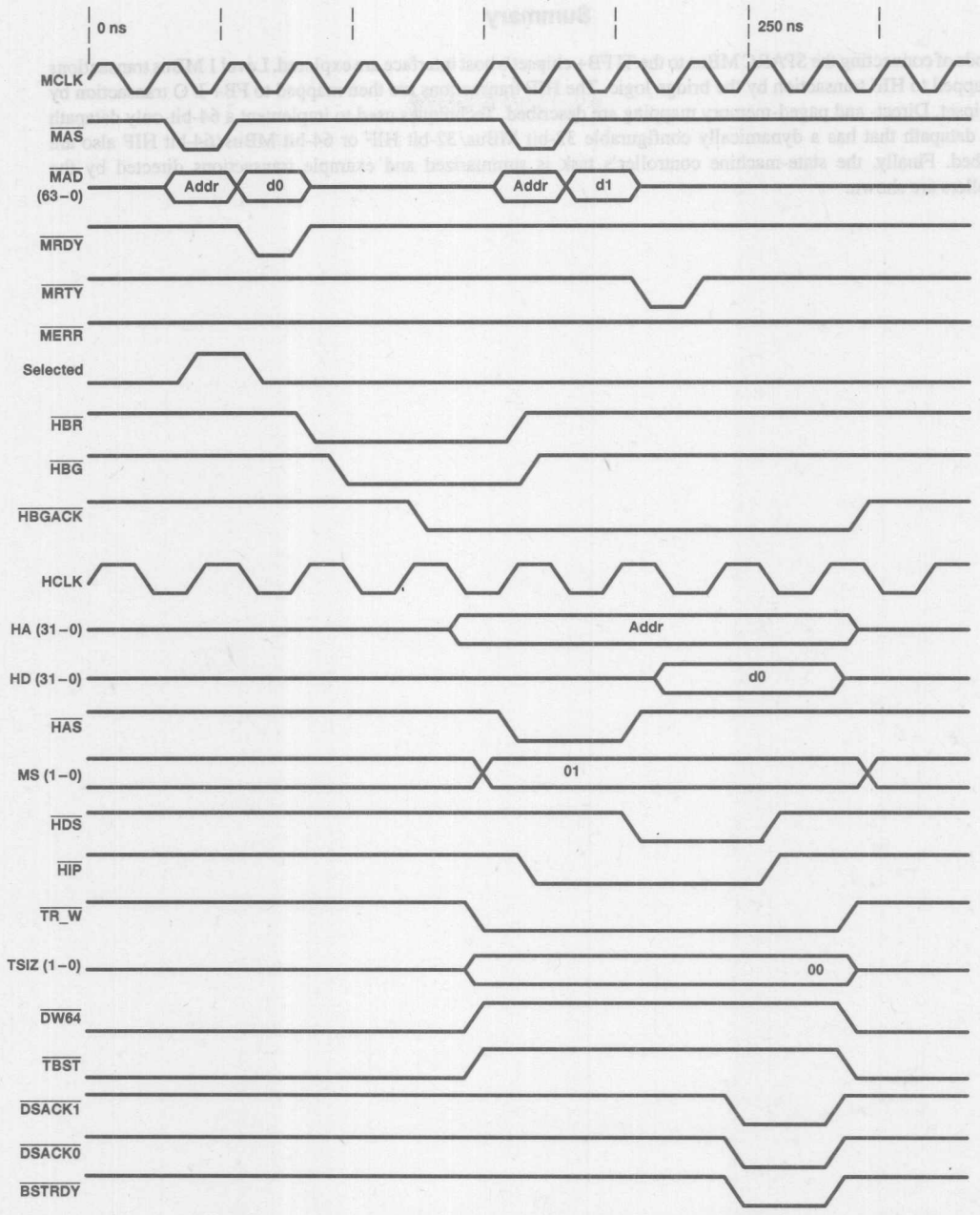
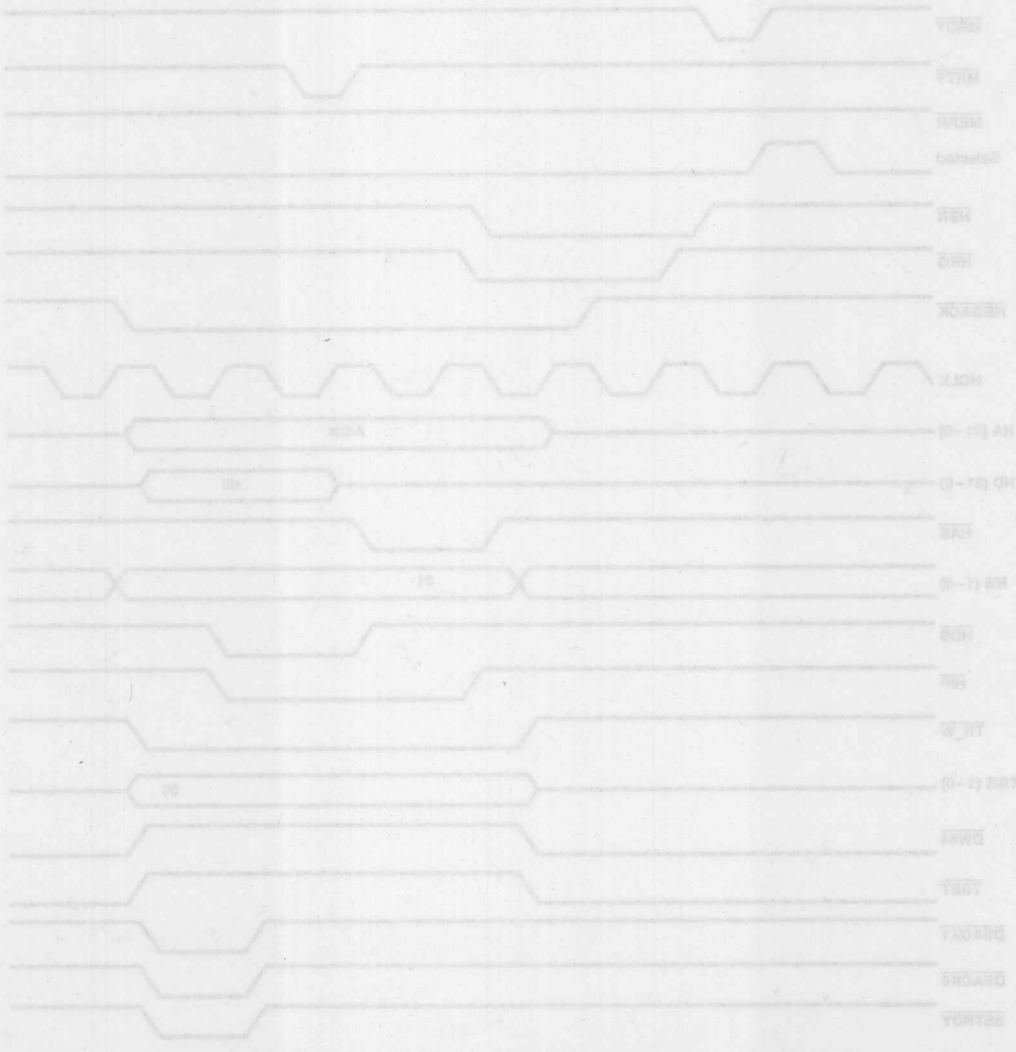


Figure 8. MBus-Word Write to HIF Single-Write Transaction

Summary

Methods of connecting the SPARC MBus to the TI FB+ chipset's host interface are explored. Level 1 MBus transactions are mapped to HIF transaction by the bridge logic. The HIF transactions are then mapped to FB+ I/O transaction by the chipset. Direct- and paged-memory mapping are described. Techniques used to implement a 64-bit-only datapath and a datapath that has a dynamically configurable 32-bit MBus/32-bit HIF or 64-bit MBus/64-bit HIF also are described. Finally, the state-machine controller's task is summarized and example transactions directed by the controllers are shown.



1K × 9 × 2 Asynchronous FIFOs SN74ACT2235 and SN74ACT2236

First-In, First-Out Technology

Kam Kittrell
Advanced System Logic – Semiconductor Group

SCAA010A

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Introduction

Texas Instruments (TI) designed the SN74ACT2235 to meet a variety of synchronous or asynchronous bidirectional applications. Two 1K x 9 first-in, first-out (FIFO) memories are arranged in parallel to buffer data in opposite directions. Data ports also may exchange real-time data. Three-state control (GAB, GBA) and real-time/stored data select (SAB, SBA) match the popular '652 transceiver logic. Produced in TI's EPIC™ CMOS process, the inputs accept TTL-voltage levels. An option to the SN74ACT2235 is the SN74ACT2236, which has '646 transceiver control (DIR, $\overline{G}$). The functional block diagram for the SN74ACT2235 is shown in Figure 1.

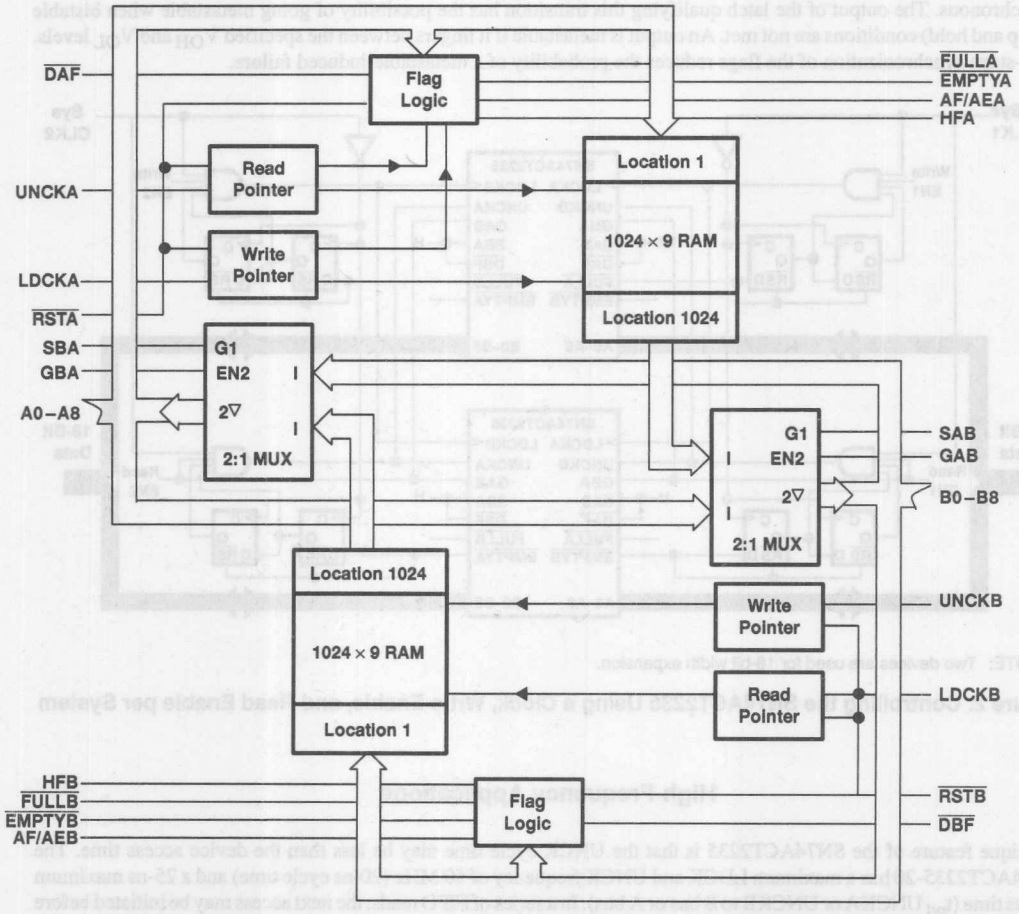


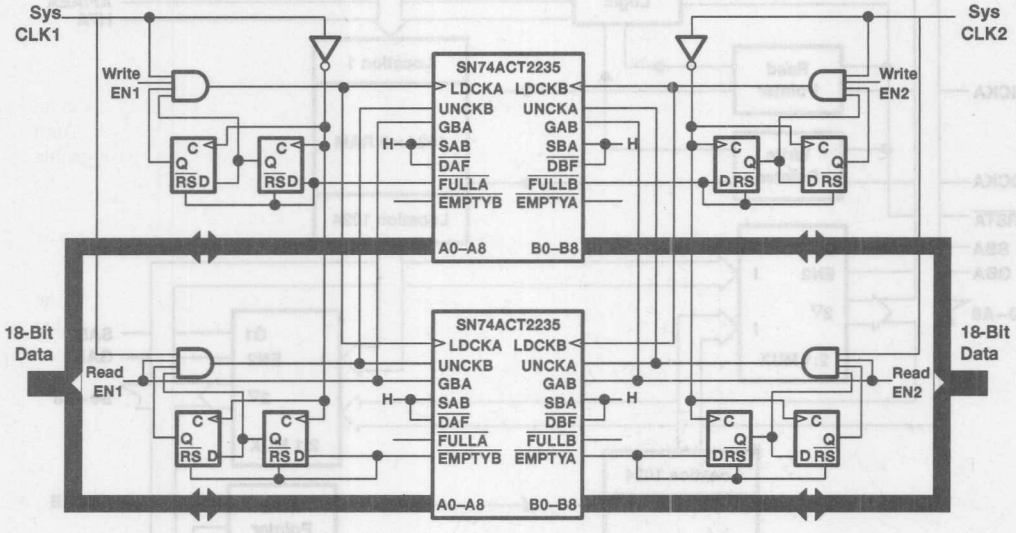
Figure 1. SN74ACT2235 Block Diagram

EPIC is a trademark of Texas Instruments Incorporated.

FIFO Control

The SN74ACT2235 consists of two FIFO memories, FIFOA and FIFOB. Both FIFOs can be accessed from either port A or port B. Four control signal lines (GAB, GBA, SAB, and SBA) control the eight possible data flow paths through the device (these datapaths are illustrated in the device data sheet). Each FIFO has a load clock (LDCK) that writes data into memory and an unload clock (UNCK) that reads the data in the same order it was written. Both clocks are positive-edge-triggered and may operate asynchronously to one another. The first word loaded into an empty FIFO propagates directly to the outputs and the $\overline{\text{EMPTY}}$ flag switches high. $\overline{\text{EMPTY}}$ represents the valid state of data on the outputs (data is valid when $\overline{\text{EMPTY}}$ is high and invalid when $\overline{\text{EMPTY}}$ is low). $\overline{\text{EMPTY}}$ may be used to enable an UNCK pulse when it is synchronized with the bus that reads the data. $\overline{\text{FULL}}$ can qualify a LDCK pulse in the same way.

Figure 2 is an example of an SN74ACT2235 interfacing two asynchronous systems. Each system provides a read enable, write enable, and free-running clock. Synchronization of a flag to the system clock is needed to use it as device-clock control. Although the flag's high-to-low transition is synchronous to the clock it enables, the low-to-high transition is asynchronous. The output of the latch qualifying this transition has the possibility of going metastable when bistable (setup and hold) conditions are not met. An output is metastable if it lingers between the specified V_{OH} and V_{OL} levels. Two-stage synchronization of the flags reduces the probability of a metastable-induced failure.



NOTE: Two devices are used for 18-bit width expansion.

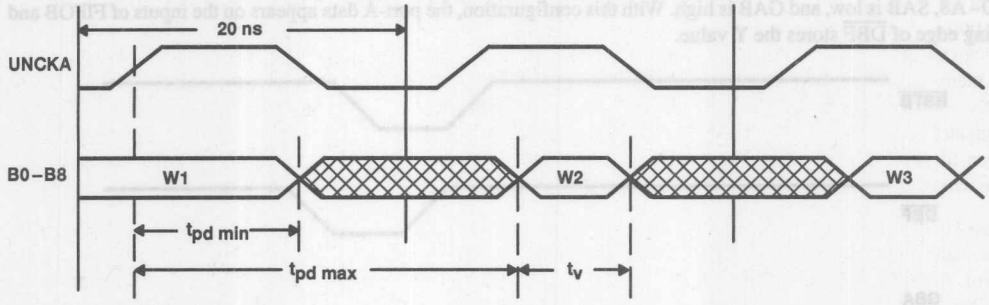
Figure 2. Controlling the SN74ACT2235 Using a Clock, Write Enable, and Read Enable per System

High-Frequency Applications

A unique feature of the SN74ACT2235 is that the UNCK cycle time may be less than the device access time. The SN74ACT2235-20 has a maximum LDCK and UNCK frequency of 50 MHz (20-ns cycle time) and a 25-ns maximum access time (t_{pd} UNCKA or UNCKB to B bus or A bus). In a series of FIFO reads, the next access may be initiated before the present one is complete. The largest concern associated with this technique is the length of time data is assured as valid. Minimum access time from the rising edge of UNCK also may be viewed as minimum data hold time. Timing for this relationship is shown in Figure 3. Valid data time from the SN74ACT2235 over the commercial temperature range and ±10% V_{CC} is given by equation 1:

$$t_v = t_c + t_{pd}\text{min} - t_{pd}\text{max} \quad (1)$$

Data from an SN74ACT2235 operating at a 50-MHz clock frequency is valid for at least 7 ns. This allows a 4-ns setup and 1-ns hold time with a 2-ns tolerance to the next device in the datapath.



For SN74ACT2235-20: $t_{pd\ min}$ = 12 ns, $t_{pd\ max}$ = 25 ns, t_v = 7 ns

Figure 3. Read Operation When Cycle Time Is Less Than Access Time

Programmable Flags

Data is often transmitted in packets, where each packet is a specific number of bytes and must be delivered in an unbroken stream. A FIFO transmitting packeted data needs a flag that shows the number of bytes stored. This keeps from breaking the transmission of a packet due to an empty or full condition. The SN74ACT2235 has a programmable almost-full/almost-empty (AF/AE) flag for this application. The AF/AEA offset value (X) and the AF/AEB offset value (Y) are programmed separately. AF/AEA is high when FIFOA contains X or fewer words or (1024 – X) or more words. It is low when FIFOA contains between (X + 1) and (1023 – X) words. AF/AEB functions in the same manner with its programmed value Y. The programmed or default value of 256 is chosen during a reset of each FIFO.

Flag-programming logic is illustrated in Figure 4. Programming the AF/AE flag value for each FIFO is done with the define-flag ($\overline{DAF}$, $\overline{DBF}$) inputs and resets ($\overline{RSTA}$, $\overline{RSTB}$). Define-flag inputs are negative-edge-triggered clocks that store input data to a register. If $\overline{DAF}$ or $\overline{DBF}$ is low when the rising edge of $\overline{RSTA}$ or $\overline{RSTB}$ occurs, the registered value is used for the FIFO AF/AE flag. The flag uses the default value of 256 if $\overline{DAF}$ or $\overline{DBF}$ is high during the rising edge of $\overline{RSTA}$ or $\overline{RSTB}$.

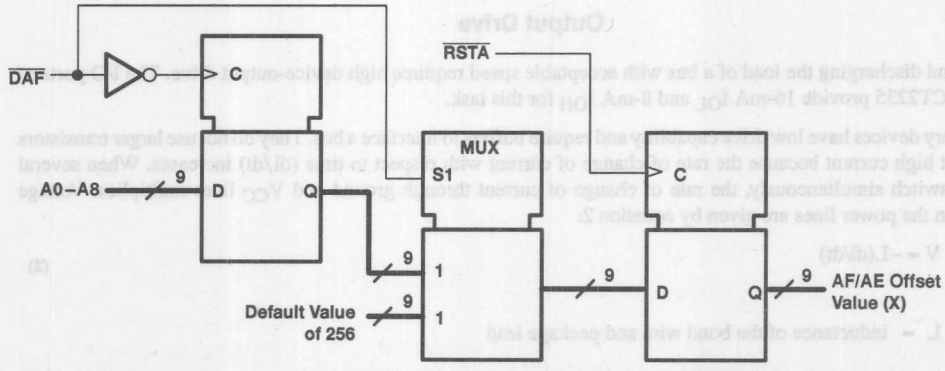


Figure 4. AF/AEA Flag-Programming Logic for FIFOA

Programming both flag offset values from either port is possible using real-time select. Figure 5 is a timing example of programming AF/AEB from port A. To program the AF/AEB offset value (Y) from port A, the binary value for Y is on A0–A8, SAB is low, and GAB is high. With this configuration, the port-A data appears on the inputs of FIFOB and a falling edge of $\overline{DBF}$ stores the Y value.

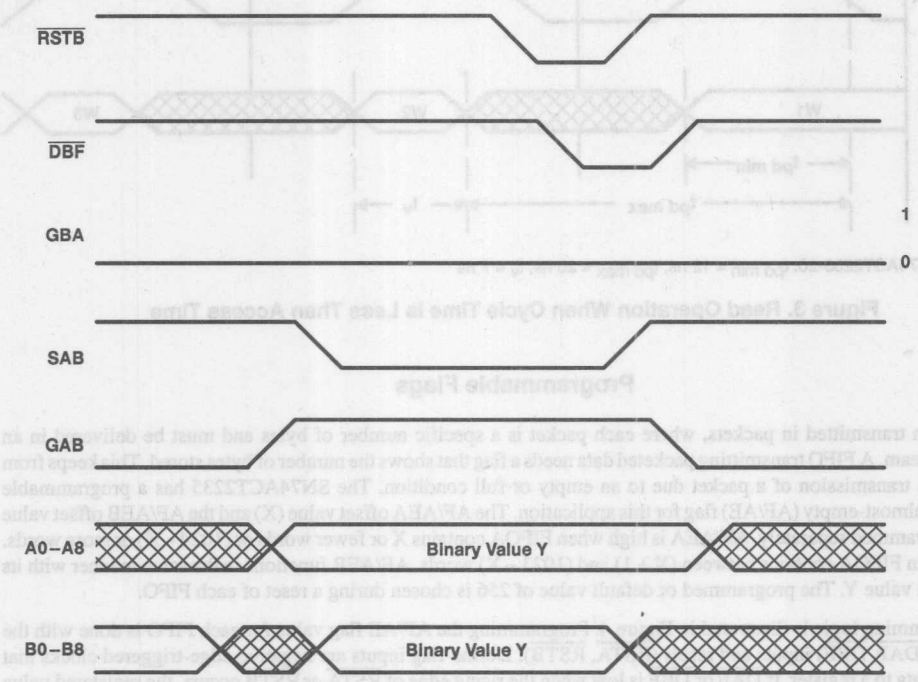


Figure 5. Programming AF/AEB Flag of FIFOB From Port A

Output Drive

Charging and discharging the load of a bus with acceptable speed requires high device-output drive. The I/O ports of the SN74ACT2235 provide 16-mA I_{OL} and 8-mA I_{OH} for this task.

Most memory devices have low drive capability and require buffers to interface a bus. They do not use larger transistors that support high current because the rate of change of current with respect to time (di/dt) increases. When several transistors switch simultaneously, the rate of change of current through ground and V_{CC} lines multiplies. Voltage transients on the power lines are given by equation 2:

$$V = -L(di/dt) \quad (2)$$

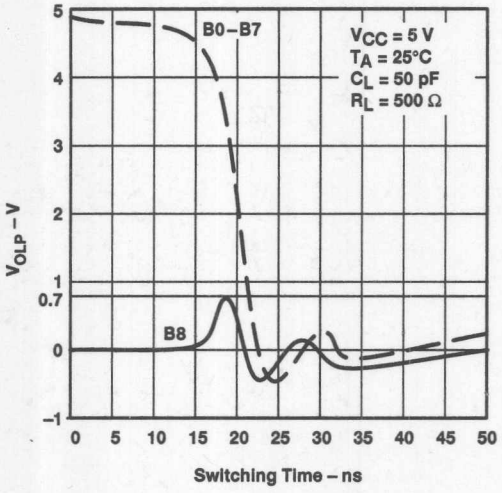
Where:

L = inductance of the bond wire and package lead

The SN74ACT2235 provides a two-fold solution to allow high-output current capability with low noise. One solution is to reduce inductance of ground and V_{CC} lines. The SN74ACT2235 has four GND and two V_{CC} pins in parallel. The resulting ground inductance is about 1/4 that of a single connection and divides V_{CC} inductance in half.

Reducing di/dt per output transistor is another way to minimize voltage transients. TI's patented output-edge-control (OEC™) design divides a large transistor into smaller segments that turn on in series and turn off simultaneously. OEC™ lowers di/dt, maintains a quick voltage transition through threshold, and avoids the high power consumed when gradually turned off .[1]

The result of a V_{OLP} test on the SN74ACT2235 is shown in Figure 6. V_{OLP} is a measurement of ground-voltage noise when all outputs of a bus are switched from high to low. Eight of nine outputs of a bus are switched, and the peak-voltage rise of the steady-state low output is measured. Maximum ground-voltage rise is only 700 mV. The output fall time is less than 3 ns with a 50-pF load.



NOTE: Eight bus outputs switching, one remains low

Figure 6. SN74ACT2235 V_{OLP} Measurement

Conclusion

The SN74ACT2235 and SN74ACT2236 provide several advantages for high-speed asynchronous bus interface. Simple control logic offers great design flexibility. Programmable flags may be used for data flow optimization. High-output drive for bus leading is balanced with noise reduction through package and circuit design.

[1] Advanced CMOS Logic Designer's Handbook, pages 3–1 through 3–12.

OEC is a trademark of Texas Instruments Incorporated.

64-Byte FIFOs
SN74ALS2232A and SN74ALS2233A

First-In, First-Out Technology

Kam Kittrell
Advanced System Logic – Semiconductor Group

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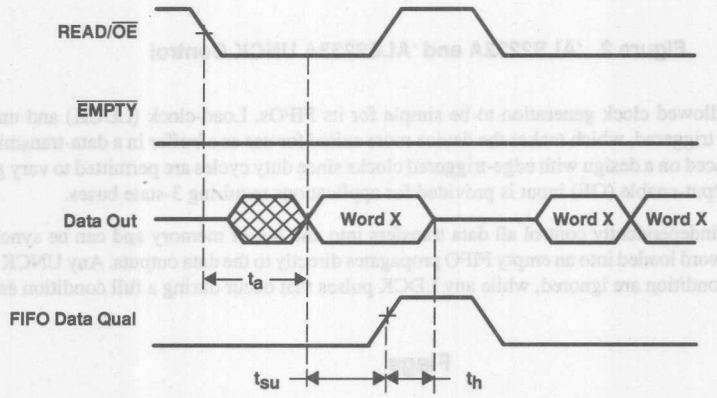
Introduction

First-in, first-out (FIFO) memories are irreplaceable bus logic when interfacing two asynchronous systems. The Texas Instruments SN74ALS2232A 64 × 18 and SN74ALS2233A 64 × 9 FIFOs are ideal solutions for many high-speed buffering needs. These bipolar devices, produced in IMPACT-X technology, come in a 28-pin PLCC and a 24-pin DIP for the 'ALS2232A and 28-pin PLCC and DIP for the 'ALS2233A.

Data is stored in a dual-port SRAM that supports transfer rates up to 40 MHz and maximum access times of 27 ns. Reads are accomplished independent of writes with separate internal addressing.

Clocks

The read enables of many FIFOs also control the active/high-impedance state of the data outputs. FIFOs using this logic must have a read-enable pulse long enough to include an access and hold time before it disables the outputs, which makes high-frequency clock design difficult (see Figures 1 and 2).



t_a = access time maximum
t_{su} = setup time minimum
t_h = hold time minimum

Figure 1. FIFO Read Control With READ/$\overline{OE}$ Logic

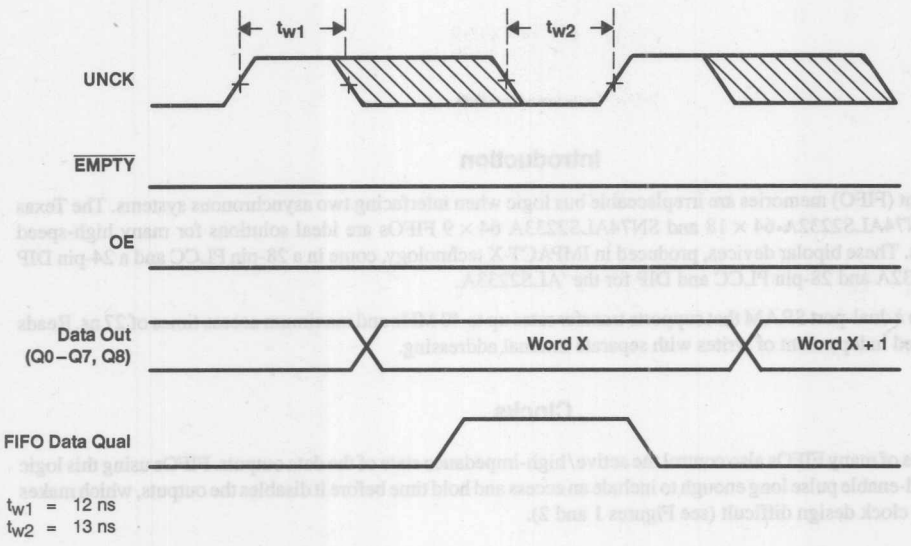


Figure 2. 'ALS2232A and 'ALS2233A UNCK Control

Texas Instruments has allowed clock generation to be simple for its FIFOs. Load-clock (LDCK) and unload-clock (UNCK) inputs are edge triggered, which makes the device more suited for use as a buffer in a data-transmission path. Fewer constraints are placed on a design with edge-triggered clocks since duty cycles are permitted to vary greatly (see Figure 2). A separate output-enable (OE) input is provided for applications requiring 3-state buses.

The LDCK and UNCK independently control all data transfers into and out of memory and can be synchronous or asynchronous. The first word loaded into an empty FIFO propagates directly to the data outputs. Any UNCK pulses that occur during an empty condition are ignored, while any LDCK pulses that occur during a full condition are ignored.

Flags

The 'ALS2232A has two flags to indicate boundary conditions of the memory: $\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$. In addition to these, the 'ALS2233A has the almost-full/almost-empty (AF/AE) and half-full (HF) flags. AF/AE is high when memory contains less than nine words or more than 55 words. To distinguish between an almost-full and an almost-empty state, HF is high when memory contains more than 31 words. The extra flags are provided for applications wherein full and empty conditions should be avoided.

Noise Control

Ground bounce is a result of current surges produced by output switching. Bond wire, lead, and board inductance cause internal ground levels to fluctuate from the current surge (rise above, then dip below 0 V). Extreme ground noise that causes input levels to cross the transition threshold may be detected as clock pulses by high-speed devices. Worst-case conditions for ground bounce are high V_{CC} and outputs switching simultaneously from high to low.

The 'ALS2232A and 'ALS2233A have package-centered V_{CC} and GND pins to combat ground bounce. The shortened bond wire and lead distance reduce package inductance from conventional corner-pin configurations.

Figure 3 shows a large voltage transient that might be measured on the ground pad of any device referenced to a 0-V plane. An input at a steady high or steady low level is likely to cross the transition threshold as a result.

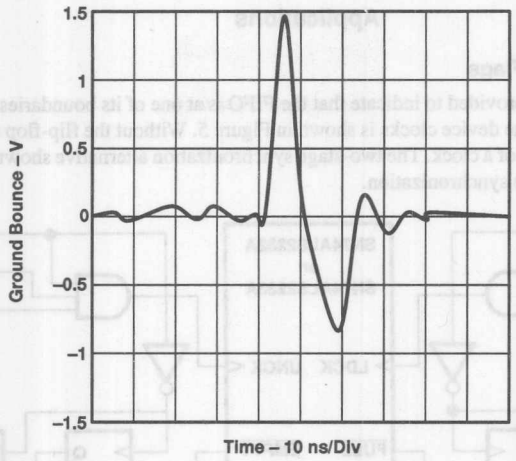


Figure 3. Noise From a GND Pad to a 0-V Plane

Figure 4 is the equivalent circuit of the clock inputs for the 'ALS2232A and 'ALS2233A. This modified RS flip-flop is more likely to pass a very quick high pulse (0 to 5 ns) caused by noise when it is in the steady low state than it is to pass a very quick low pulse when in the steady high state. The clock input one-shot structure is immune to a very quick (0 to 5 ns) low pulse when in the steady high state. For improved noise protection, LDCK and UNCK signals may be generated as inactive high with a low pulse generated for clocking.

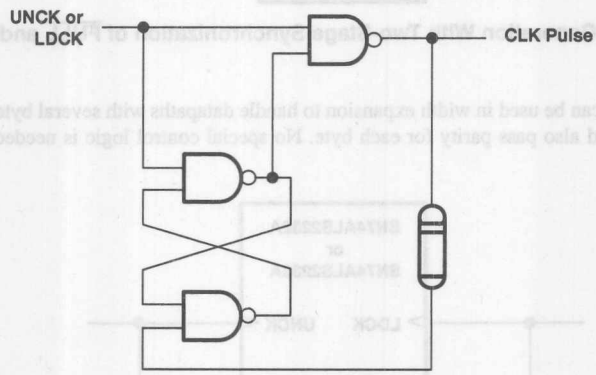


Figure 4. 'ALS2232A and 'ALS2233A Clock Input Circuit

Using the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ Flags

The $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ flags are provided to indicate that the FIFO is at one of its boundaries. An example of how to qualify these flags as enables for the device clocks is shown in Figure 5. Without the flip-flop qualification, a flag can cause the asynchronous generation of a clock. The two-stage synchronization alternative shown reduces the chances of a metastable output from one-stage synchronization.

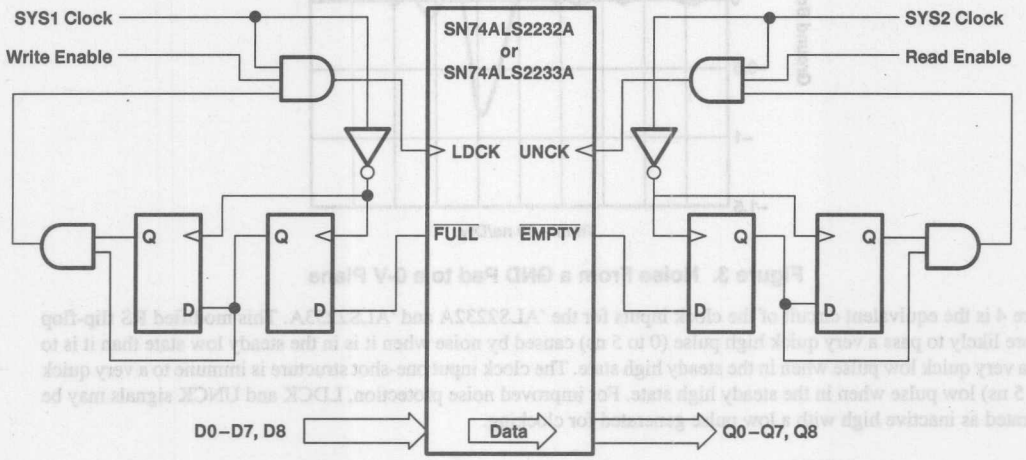


Figure 5. Clock Generation With Two-Stage Synchronization of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$

Width Expansion

Several 'ALS2232A devices can be used in width expansion to handle datapaths with several bytes. The 'ALS2232A can likewise be expanded and also pass parity for each byte. No special control logic is needed to implement this application (see Figure 6).

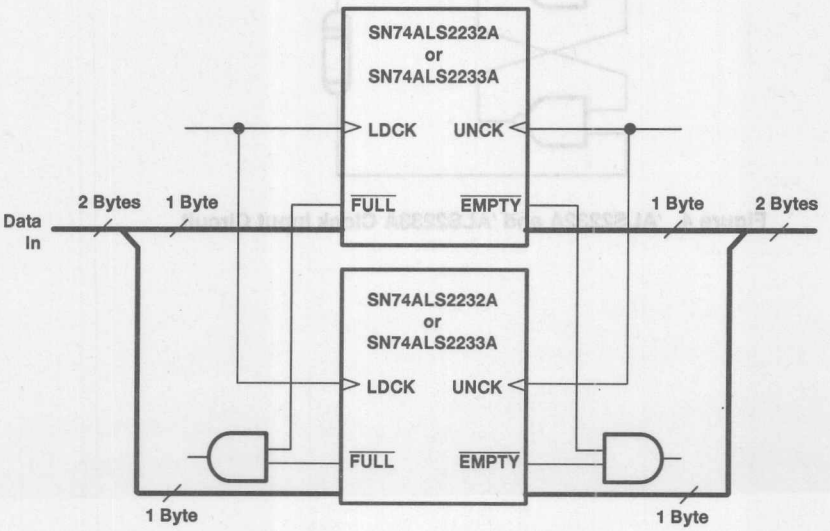


Figure 6. Width Expansion

Bus Conversion

Systems frequently require that data be converted from 1-byte buses to multiple-byte buses operating asynchronously. Figure 7 shows an 18-bit bus folded into a 9-bit bus using the 'ALS2233A. The control logic can be implemented with a TIBPAL20R4.

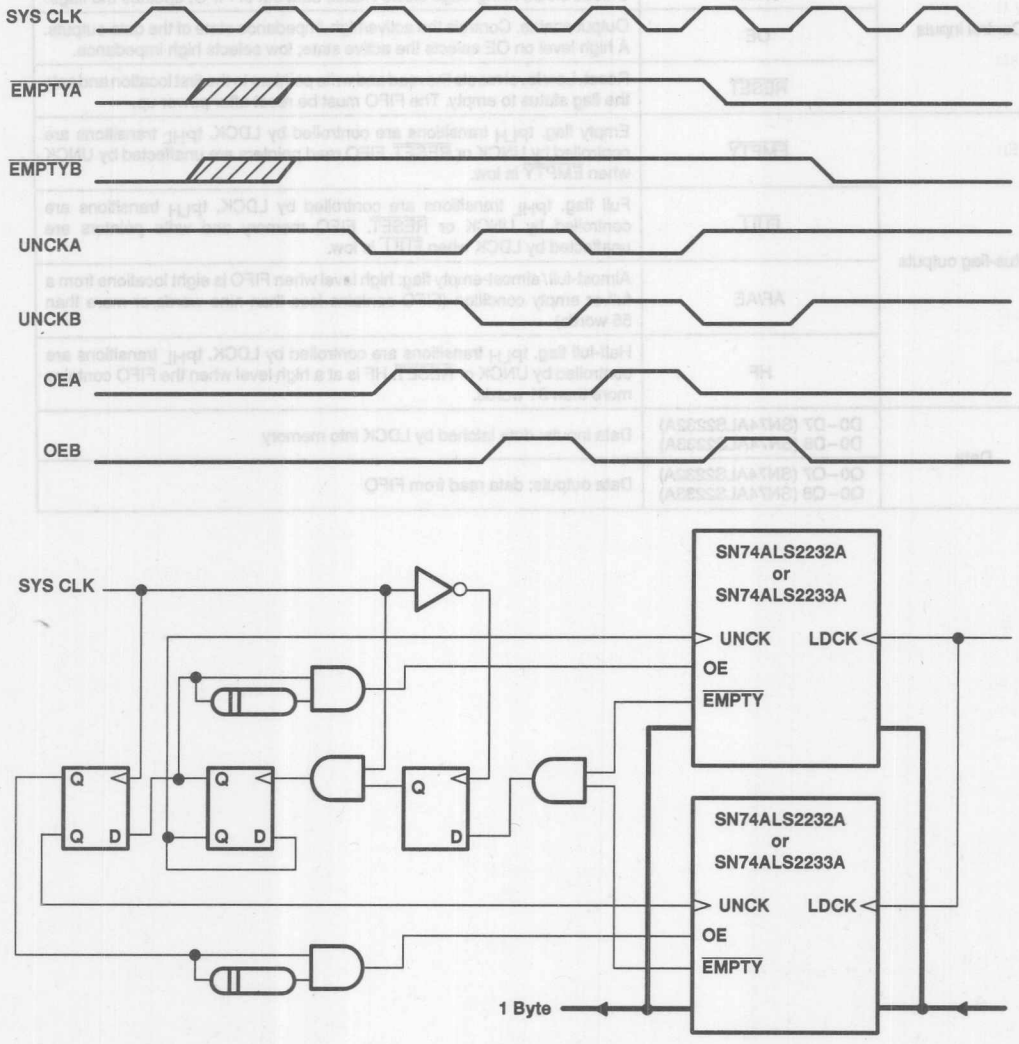
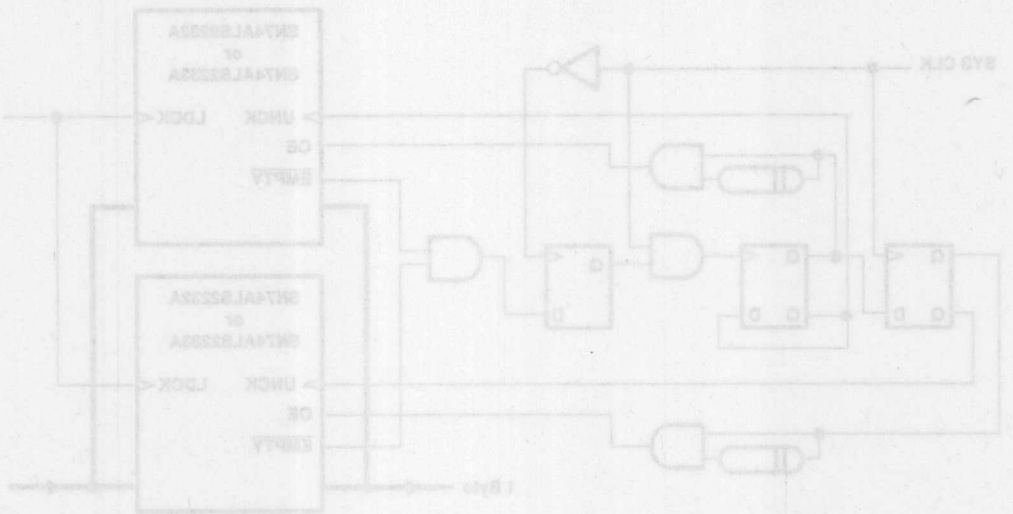


Figure 7. Bus-Folding Logic

Table 1. Terminal Functions

FUNCTION	TERMINAL NAME	DEFINITION
Control inputs	LDCK	Load clock; rising-edge clock. Writes data into the FIFO; updates the flags.
	UNCK	Unload clock; rising-edge clock. Reads data out of FIFO; updates the flags.
	OE	Output enable. Controls the active/high-impedance state of the data outputs. A high level on OE selects the active state; low selects high impedance.
	$\overline{\text{RESET}}$	Reset. Low level resets the read and write pointers to the first location and sets the flag status to empty. The FIFO must be reset after power up.
Status-flag outputs	$\overline{\text{EMPTY}}$	Empty flag. t_{PLH} transitions are controlled by LDCK. t_{PHL} transitions are controlled by UNCK or $\overline{\text{RESET}}$. FIFO read pointers are unaffected by UNCK when $\overline{\text{EMPTY}}$ is low.
	$\overline{\text{FULL}}$	Full flag. t_{PHL} transitions are controlled by LDCK. t_{PLH} transitions are controlled by UNCK or $\overline{\text{RESET}}$. FIFO memory and write pointers are unaffected by LDCK when $\overline{\text{FULL}}$ is low.
	AF/AE	Almost-full/almost-empty flag: high level when FIFO is eight locations from a full or empty condition (FIFO contains less than nine words or more than 55 words)
	HF	Half-full flag. t_{PLH} transitions are controlled by LDCK. t_{PHL} transitions are controlled by UNCK or $\overline{\text{RESET}}$. HF is at a high level when the FIFO contains more than 31 words.
Data	D0–D7 (SN74ALS2232A) D0–D8 (SN74ALS2233A)	Data inputs: data latched by LDCK into memory
	Q0–Q7 (SN74ALS2232A) Q0–Q8 (SN74ALS2233A)	Data outputs: data read from FIFO



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4 Power Considerations

Introduction

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Introduction

This section of the FIFO Designer's Handbook shows typical power characteristics in the form of active supply current versus frequency plots for each of Texas Instruments (TI's) advanced FIFOs. In some cases, plots of idle supply current (I_{CCI}) versus frequency are also included. In addition to the current versus frequency data, sample calculations of power dissipation are included in this section for a representative set of FIFOs. The application report entitled *Power Dissipation Calculations for TI FIFO Products* serves as a guideline for the example calculations. Equations for dynamic, quiescent, and total power dissipation for both ACT and ABT FIFOs are given, along with the idle I_{CC} versus frequency plots required for the sample calculations in this section. These and other key equations that are used in the calculation of power dissipation are repeated below and numbered for convenience.

Key Power-Dissipation Equations for ACT FIFOs

Quiescent

$$P_q = V_{CC} \times [I_{CCI} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] \quad (1)$$

Where:

I_{CCI} = $f_{clock} \times pF_{(clock)}$ = supply current when FIFO is idle
f_{clock} = clock switching frequency
$pF_{(clock)}$ = clock switching power factor (slope of I_{CC} versus f_{clock} curve)
N_{TTL} = number of inputs driven by TTL levels
ΔI_{CC} = increase in supply current for each input at a TTL high level (see data sheet)
DC_{VIH} = percent of TTL signals at a high level of 3.4 V

Dynamic Power

$$P_d = V_{CC} \times [I_{CCf} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] + \Sigma(C_L \times V_{CC}^2 \times f_o) \quad (2)$$

Where:

V_{CC} = supply voltage
I_{CCf} = supply current when FIFO is transferring data
N_{TTL} = number of inputs driven by TTL levels
ΔI_{CC} = increase in supply current for each input at a TTL high level (see data sheet)
DC_{VIH} = percent of TTL signals at a high level of 3.4 V
C_L = load capacitance
f_o = output switching frequency = [1/2 (since maximum data rate is 1/2 clock frequency) × (fraction of outputs switching at a given time) × (frequency of the slowest of the port clocks)]

Total Power

$$P_t = P_d(DC_d) + P_q(1\text{-}DC_d) \quad (3)$$

Where:

P_d = dynamic power dissipation
P_q = quiescent power dissipation
DC_d = duty cycle

Key Power-Dissipation Equations for ABT FIFOs

Quiescent Power

$$P_q = V_{CC} \times [DC_{EN} \times (N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T) + (1\text{-}DC_{EN}) \times I_{CCZ} + I_{CCI}] \quad (4)$$

Where:

V_{CC}	=	supply voltage
I_{CCI}	=	$f_{clock} \times pF_{(clock)}$ = supply current when FIFO is idle
f_{clock}	=	clock switching frequency
$pF_{(clock)}$	=	clock switching power factor (slope of I_{CC} versus f_{clock} curve)
DC_{EN}	=	percent duty cycle enabled
I_{CCH}	=	power supply current when outputs are in the high state (see data sheet)
I_{CCL}	=	power supply current when outputs are in the low state (see data sheet)
I_{CCZ}	=	power supply current when outputs are in the high-impedance state (see data sheet)
N_L	=	number of outputs in low state
N_H	=	number of outputs in high state
N_T	=	total number of outputs

Dynamic Power

$$P_q = V_{CC} \times I_{CCf} + \Sigma[V_{CC} \times C_L \times (V_{OH} - V_{OL}) \times f_o] \quad (5)$$

Where:

V_{CC}	=	supply voltage
I_{CCf}	=	supply current when FIFO is transferring data, active current
f_o	=	output switching frequency = [1/2 (since maximum data rate is 1/2 clock frequency) × (fraction of outputs switching at a given time) × (frequency of the slowest of the port clocks)]
V_{OH}	=	output voltage in high state
V_{OL}	=	output voltage in low state
C_L	=	load capacitance

Total Power

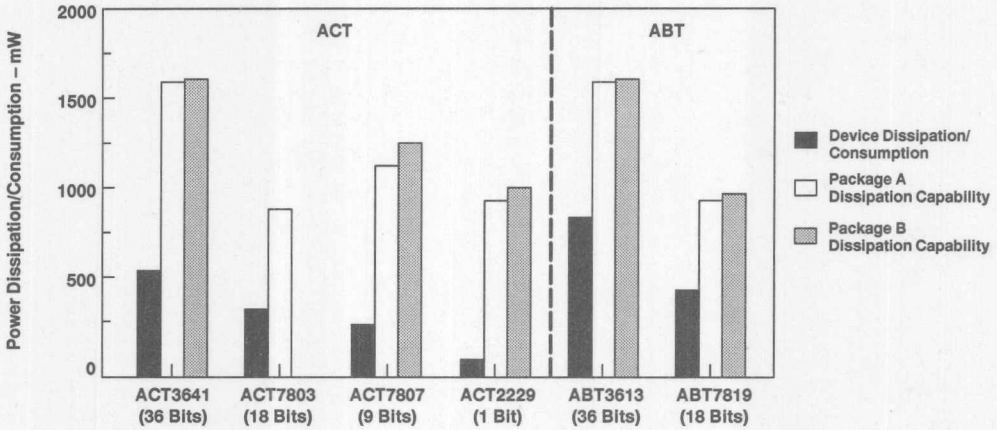
$$P_t = P_d(DC_d) + P_q(1\text{-}DC_d) \quad (6)$$

Where:

P_d	=	dynamic power dissipation
P_q	=	quiescent power dissipation
DC_d	=	duty cycle

In all of the following power calculation examples, the FIFO inputs are being driven by a TTL device. In the case where the inputs are driven by a CMOS device, the ΔI_{CC} term in the power-dissipation equation equals zero and can be ignored. In each calculation, the number of inputs (or outputs) equal to the width of the FIFO are assumed to be switching in order to provide a worst-case solution for the conditions being assumed.

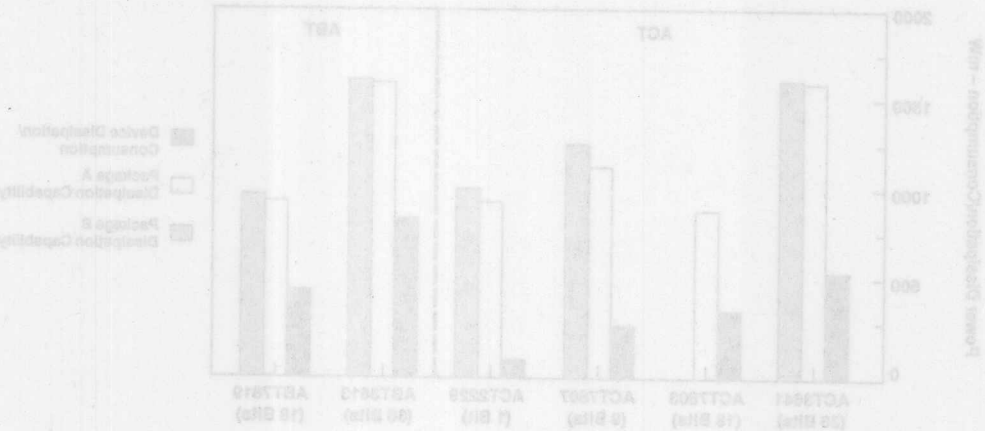
Figure 1 contains the results of the sample power-dissipation calculations. The plot is divided up into results for the ACT FIFOs and results for the ABT FIFOs. Within each of these technologies, the conditions for each sample calculation have been chosen to provide (as much as possible) an apples-to-apples comparison (see individual calculations in this section). As previously noted, the number of bits switching at a given time is assumed to be equal to the width of the FIFO under consideration. In addition to the results of the calculations, the maximum power-dissipation capability of the packages associated with these devices at 70°C with no air flow is also plotted. In every case, the dissipation capability of the package significantly exceeds the power being dissipated by the device, even under the rather severe conditions stated above. The specific packages and their associated dissipation capabilities are listed in Figure 1.



DEVICE	PACKAGE A		PACKAGE B	
	NOMENCLATURE	DISSIPATION CAPABILITY (mW)†	NOMENCLATURE	DISSIPATION CAPABILITY (mW)†
ACT3641	120-pin TQFP (PCB)	1606	132-pin PQFP (PQ)	1610
ACT7803	56-pin SSOP (DL)	851		
ACT7807	64-pin TQFP (PAG)	1121	44-pin PLCC (FN)	1244
ACT2229	24-pin SOIC (DW)	909	28-pin SOIC (DW)	978
ABT3613	120-pin TQFP (PCB)	1606	132-pin PQFP (PQ)	1610
ABT7819	80-pin TQFP (PN)	911	80-pin PQFP (PH)	954

† The conditions of 70°C and no air flow are assumed.

Figure 1. Comparison of Device and Package Power-Dissipation/Consumption Capabilities



DEVICE	PACKAGE A		PACKAGE B	
	NOMENCLATURE	DISSIPATION CAPABILITY (mW)†	NOMENCLATURE	DISSIPATION CAPABILITY (mW)†
ACT3841	28-pin TDFP (PCB)	1808	132-pin PQFP (PQ)	1810
ACT7803	68-pin SSOP (DL)	821		
ACT7807	64-pin TDFP (PAG)	1121	44-pin PLCC (FN)	1244
ACT2229	24-pin SOIC (DW)	909	28-pin SOIC (DW)	978
ABT3813	120-pin TDFP (PCB)	1808	132-pin PQFP (PQ)	1810
ABT7819	68-pin TDFP (PN)	911	80-pin PQFP (PH)	964

† The conditions of 70°C and no air flow are assumed.

Application Report

Power-Dissipation Calculations for TI FIFO Products

Navid Madani
Advanced System Logic – Semiconductor Group

TEXAS INSTRUMENTS

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Abstract

Power consumption has become a major consideration in today's circuit design. Low power consumption is one of the major advantages of Texas Instruments (TI) FIFO products. Power calculations are required to meet the design requirements relating to the chip temperature and system power. The only way that a designer can minimize the power requirements of a board or a system is to understand and control the causes. This application report assists the component and system design engineer to evaluate the power consumption of TI ACT and ABT FIFO products.

Introduction

A simple method of calculating power dissipation for FIFO products under varying conditions is presented in this application report. Power calculations include the power dissipation when a FIFO is transferring data as well as when only clocks are running and no data is being transferred. Power consumption in a FIFO product is dependent on clock switching frequency, data-input switching frequency, data-output switching frequency, and data-output capacitive loading.

In this report, a simplified introduction to the physics of CMOS devices regarding power consumption is presented. In the second part of this application report, power-calculation examples for FIFO products are presented in two subsections. The first subsection includes power-dissipation calculations for advanced CMOS (ACT) FIFO products, including an example using the SN74ACT3632. The second subsection includes power-dissipation calculations for advanced BiCMOS (ABT) FIFO products, including an example using the SN74ABT3614. Appendix A includes several graphs of I_{CC} versus frequency to assist the design engineer with the information required for calculating power consumption. In addition, the graphs of I_{CC} versus frequency assist the designer in selecting a device with the lowest power consumption. Appendix B presents reliability information and a table of maximum power versus ambient temperature for different package types. Finally, the goals, achievements, and results of this application report are included in the summary.

CMOS and BiCMOS Power Basics

Power dissipation is dependent on supply voltage (V_{CC}) and supply current (I_{CC}). It is calculated using the formula:

$$P = V_{CC} \times I_{CC}$$

Any CMOS function can be broken down to a gate-level model. The simplest CMOS circuit is an inverter as shown in Figure 1. When the input voltage is at ground or V_{CC} level, one transistor is fully on and the other transistor is fully off. This results in a negligible I_{CC} that is simply the reverse-leakage current flowing through the nonconducting transistor. Quiescent power is due to this current (referred to as idle I_{CC} in this application report).

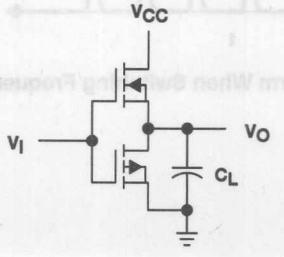


Figure 1. Gate Model of a CMOS Inverter

When the input switches from V_{CC} to ground or vice versa during the transition period, both transistors are on, resulting in current flow from V_{CC} to ground. This current is called through current (referred to as active current in this application report). For many applications using CMOS and BiCMOS devices, switching power accounts for most of the power consumption.

The through-current waveform supplied by V_{CC} to a CMOS gate is shown in Figure 2. As the switching frequency increases, the number of current spikes also increases. For instance, if the switching frequency is doubled, the number of current spikes double. Figure 3 shows the current spikes for the same device at twice the frequency of the signal shown in Figure 2. Since power is directly proportional to the RMS current, the increase in frequency results in increased power dissipation. Power consumption due to the load should also be considered. For a CMOS device with an entirely capacitive load, the transient power due to the load is calculated using the formula:

$$P = C_L \times V_{CC}^2 \times f_o$$

Where:

C_L = load capacitance
V_{CC} = supply voltage
f_o = output switching frequency

Power calculations are presented in more detail in the following sections of this application report.

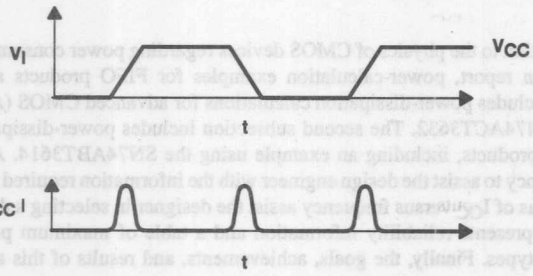


Figure 2. Current Waveform Supplied by V_{CC} to a CMOS Gate

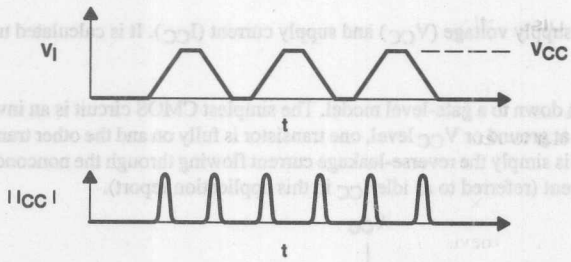


Figure 3. Current Waveform When Switching Frequency Is Doubled

Power Calculation

The total power consumption in the ACT and ABT FIFOs is the sum of the quiescent or nonswitching power (P_q) and dynamic or switching power (P_d):

$$P_T = P_d\,(DC_d) + P_q\,(1 - DC_d)$$

Where:

P_T	=	total power
P_d	=	dynamic or switching power
P_q	=	quiescent or nonswitching power
DC_d	=	% time FIFO is switching
$1 - DC_d$	=	% time FIFO is not switching

Quiescent or Nonswitching Power Dissipation in ACT FIFO Devices (CMOS FIFO products)

The quiescent power consumed by a CMOS device is given by the formula:

$$P_q = V_{CC} \times I_{CC}\,(\text{total})$$

Where V_{CC} is the supply voltage and I_{CC} (total) includes the increase in I_{CC} due to inputs being driven by TTL devices. This is calculated as:

$$I_{CC}\,(\text{total}) = [N_{TTL} \times \Delta I_{CC} \times DC_{VIH}] + I_{CCI}$$

Where:

I_{CCI}	=	$f_{clock} \times pF_{(clock)}$ = supply current when FIFO is idle (the clocks are running but no data is written to or read from the FIFO)
f_{clock}	=	clock switching frequency
$pF_{(clock)}$	=	clock switching power factor, the slope of I_{CC} versus f_{clock} curve (see data sheet)
N_{TTL}	=	number of inputs driven by TTL levels
ΔI_{CC}	=	increase in supply current for each input at a TTL high level (see data sheet)
DC_{VIH}	=	% of TTL signals at a high level of 3.4 V

Therefore, the quiescent power is calculated by:

$$P_q = V_{CC} \times [I_{CCI} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})]$$

Dynamic or Switching Power Dissipation in ACT FIFO Devices (CMOS FIFO products)

For most applications, dynamic power accounts for most of the total power dissipation of a CMOS device. Dynamic power is dependent on the load capacitance, output switching frequency, input switching frequency, and the power-dissipation capacitance of the device. The following equation is typically used to calculate power consumption in a CMOS device (refer to *Texas Instruments Advanced CMOS Logic Designer's Handbook*, literature number SCAA001A).

$$P_d = (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

The value C_{pd} is not provided for most FIFO devices. It is more accurate to calculate power of a FIFO device by obtaining active I_{CC} versus frequency curves, I_{CCf} (supply current when the FIFO is transferring data) and the slope of the I_{CC} versus frequency curve (which essentially display the same information). Consequently, dynamic power includes the power dissipation due to active I_{CC} without the output load and power dissipation due to the output load current.

$$P_d = V_{CC} \times I_{CC}\,(\text{total}) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

Where:

$V_{CC} \times I_{CC}$ (total)	=	device switching power without load
I_{CC} (total)	=	$[I_{CCf} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})]$
$\Sigma(C_L \times V_{CC}^2 \times f_o)$	=	power due to output switching frequency and load capacitance

Therefore, dynamic power consumption is calculated by:

$$P_d = V_{CC} \times [I_{CCf} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

Where:

V_{CC} = supply voltage
I_{CCf} = supply current when the FIFO is transferring data (see active I_{CC} versus frequency plot in data sheet)
N_{TTL} = number of inputs driven by TTL levels
ΔI_{CC} = increase in supply current for each input at a TTL high level (see data sheet)
DC_{VIH} = % of inputs at a TTL high level
C_L = load capacitance
f_o = output switching frequency

Example 1

This example shows how to calculate the power dissipation for an SN74ACT3632 bidirectional FIFO used in a system under the following conditions:

- Data input lines (A0–A35) are driven by a TTL device.
- Control signals (CLKA, CLKB, $\overline{CSA}$, $\overline{CSB}$, W/$\overline{RA}$, $\overline{W}$/RB, $\overline{RST1}$, $\overline{RST2}$, ENA, ENB, MBA, MBB, FSO, FS1) are driven by a CMOS device.
- The output of the FIFO is fed to a memory device.
- Only 3/4 of the inputs (or outputs) are switching at a given time.
- The port-B clock rate is 33.3 MHz and the port-A clock rate is 40 MHz.
- The SN74ACT3632 is only used about 1/3 of the time by the system.
- The load capacitance on each output is about 30 pF, and the supply voltage is set at 5 V.
- The SN74ACT3632 is used equally in both directions.

The following parametric values are needed to calculate power dissipation:

Where:

V_{CC} = supply voltage = 5 V
DC_d = % time FIFO is switching = 1/3
$1 - DC_d$ = % time FIFO is not switching = 2/3
f_{clockA} = clock switching frequency of port A = 40 MHz
f_{clockB} = clock switching frequency of port B = 33.3 MHz
pF = clock switching power factor, the slope of I_{CC} versus f_{clock} curve (see data sheet)
= 0.184 mA/MHz
I_{CCI} = $I_{CLKA} + I_{CLKB} = (f_{clockA} \times pF) + (f_{clockB} \times pF)$
= (40 MHz + 33.3 MHz) × 0.184 mA/MHz = 13.4872 mA
N_{TTL} = number of inputs driven by TTL levels = 36
I_{CCf} = active supply current when FIFO is transferring data from the curve if I_{CC} versus frequency = 115 mA @ 33.3 MHz
ΔI_{CC} = increase in supply current for each input at a TTL high level (see data sheet)
= 0 mA if $\overline{CSA} = V_{IH}$ or $\overline{CSB} = V_{IH}$
= 1 mA if $\overline{CSA} = V_{IL}$ or $\overline{CSB} = V_{IL}$
= 1 mA for all other inputs (see data sheet)

In this example (ΔI_{CC} = 1 mA is assumed):

DC_{VIH} = 3/4
C_L = load capacitance = 30 pF
f_o = output switching frequency = 1/2 (since maximum data rate is 1/2 clock frequency)
× 3/4 (since 3/4 of the outputs are switching at a given time)
× 33.3 (slowest of the two clock frequencies, f_{clockA} or f_{clockB}) = 12.4875 MHz

I_{CCf} and I_{CCI} are taken from graphs of I_{CC} versus clock frequency. In the case of SN74ACT3632, I_{CCI} is taken for either of the two clocks while only one clock is switching. All other inputs are tied to 0 or to V_{CC} – 0.2 V and all the outputs are disconnected. Later, I_{CCf} is measured while simultaneously reading and writing a FIFO with both CLKA and CLKB set to f_{clock}.

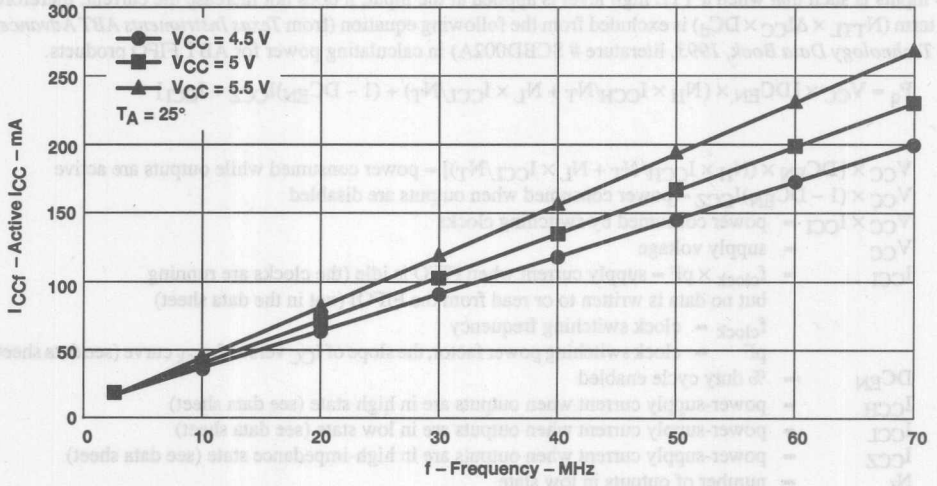


Figure 4. SN74ACT3632 Active I_{CC} Versus Frequency

Solution

$$\begin{aligned} P_T &= P_T \text{ (from A to B)} + P_T \text{ (from B to A)} \\ &= P_q \text{ (from A to B)} + P_q \text{ (from B to A)} + P_d \text{ (from A to B)} + P_d \text{ (from B to A)} \\ &= P_q + P_d \end{aligned}$$

Where P_q and P_d include power from A to B and from B to A directions.

Quiescent Power

$$\begin{aligned} P_q &= V_{CC} \times [I_{CCI} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] \\ &= 5 \times [13.4872 \text{ mA} + (36 \times 1 \text{ mA} \times 3/4)] = 202.436 \text{ mW} \end{aligned}$$

Dynamic Power

$$\begin{aligned} P_d &= V_{CC} \times [I_{CCf} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] + \Sigma(C_L \times V_{CC}^2 \times f_o) \\ &= 5 \times [115 \text{ mA} + (36 \times 1 \text{ mA} \times 3/4)] + [36 \times 30 \text{ pF} \times (5 \text{ V})^2 \times 12.4875 \text{ MHz}] \\ &= 710 \text{ mW} + 337.1625 \text{ mW} = 1047.1625 \text{ mW} \end{aligned}$$

Total Power

$$\begin{aligned} P_T &= P_d (DC_d) + P_q (1 - DC_d) \\ &= 1047.1625 \text{ mW} \times 1/3 + 202.436 \text{ mW} \times 2/3 = 484.0115 \text{ mW} \end{aligned}$$

Therefore, total power is approximately:

$$P_T = 484 \text{ mW}$$

The SN74ACT3632 is available in 120-pin TQFP and 132-pin PQFP packages (refer to Appendix B for the maximum power curve calculated for reliability purposes). At maximum ambient temperature (70°C) and no air flow for 132-pin PQFP and 120-pin TQFP packages, the maximum power that the packages can dissipate to free air is 1610 mW and 1606 mW, respectively. The SN74ACT3632, in this example, meets the reliability requirement since 484 mW is much less than 1610 mW or 1606 mW.

Quiescent or Nonswitching Power Dissipation in ABT FIFO Devices (BiCMOS FIFO products)

Unlike CMOS devices that have a single value for I_{CC}, BiCMOS devices have varying static current levels depending on the state of the output (I_{CCL}, I_{CCH}, I_{CCZ}). Quiescent power includes the power consumed while outputs are active, the power consumed when outputs are disabled, and the power consumed by the switching clocks. The design of the BiCMOS inputs is such that when a TTL high level is applied at the input, it does not increase the current; therefore, the ΔI_{CC} term ($N_{TTL} \times \Delta I_{CC} \times DC_d$) is excluded from the following equation (from *Texas Instruments ABT Advanced BiCMOS Technology Data Book, 1993,* literature # SCBD002A) in calculating power for ABT FIFO products.

$$P_q = V_{CC} \times [DC_{EN} \times (N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T) + (1 - DC_{EN})I_{CCZ} + I_{CCI}]$$

Where:

$V_{CC} \times [DC_{EN} \times (N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T)]$ = power consumed while outputs are active
$V_{CC} \times (1 - DC_{EN})I_{CCZ}$ = power consumed when outputs are disabled
$V_{CC} \times I_{CCI}$ = power consumed by switching clocks
V_{CC} = supply voltage
I_{CCI} = $f_{clock} \times pF$ = supply current when FIFO is idle (the clocks are running but no data is written to or read from the FIFO) (not in the data sheet)
f_{clock} = clock switching frequency
pF = clock switching power factor, the slope of I_{CC} versus f_{clock} curve (see data sheet)
DC_{EN} = % duty cycle enabled
I_{CCH} = power-supply current when outputs are in high state (see data sheet)
I_{CCL} = power-supply current when outputs are in low state (see data sheet)
I_{CCZ} = power-supply current when outputs are in high-impedance state (see data sheet)
N_L = number of outputs in low state
N_H = number of outputs in high state
N_T = total number of outputs

Dynamic or Switching Power Dissipation in ABT FIFO Devices (BiCMOS FIFO products)

For most applications, dynamic power accounts for most of the total power consumption of a BiCMOS device. Dynamic power consumption includes the device switching power consumed without the load, as well as the power consumed due to the capacitive load.

$$P_d = V_{CC} \times I_{CCf} + \Sigma[V_{CC} \times C_L \times (V_{OH} - V_{OL}) \times f_o]$$

Where:

$V_{CC} \times I_{CCf}$ = device switching power without the load
$\Sigma[V_{CC} \times C_L \times (V_{OH} - V_{OL}) \times f_o]$ = power consumed due to the output switching frequency and the load capacitance
V_{CC} = supply voltage
I_{CCf} = supply current when FIFO is transferring data, active current (see active I_{CC} versus frequency plot in data sheet)
f_o = output switching frequency
V_{OH} = output voltage in high state
V_{OL} = output voltage in low state
C_L = load capacitance

Example 2

This example shows how to calculate the power dissipation for an SN74ABT3614 bidirectional FIFO used in a system under the following conditions:

- Data input lines (A0–A35) and the control signals (CLKA, CLKB, $\overline{CSA}$, $\overline{CSB}$, W/$\overline{RA}$, W/$\overline{RB}$, ENA, ENB, MBA, $\overline{BE}$, $\overline{RST}$, SIZ0, SIZ1, ODD/$\overline{EVEN}$, SW0, SW1, PGA, PGB) are driven by a CMOS device.
- Only 2/3 of the inputs (or outputs) are switching at a given time.
- The output of the FIFO is fed to a memory device.
- The port-B clock rate is 33.3 MHz and the port-A clock rate is 40 MHz.
- The SN74ABT3614 is only used 60% of the time by the system.
- The load capacitance of each output is about 50 pF, and the supply voltage is set to 5 V.
- During the FIFO active period, the bus is enabled 75% of the time.
- When the bus is enabled, the output is in the high state 80% of the time.
- The SN74ABT3614 is used equally in both directions.

Figures 5 through 7 and included information are needed to calculate power dissipation:

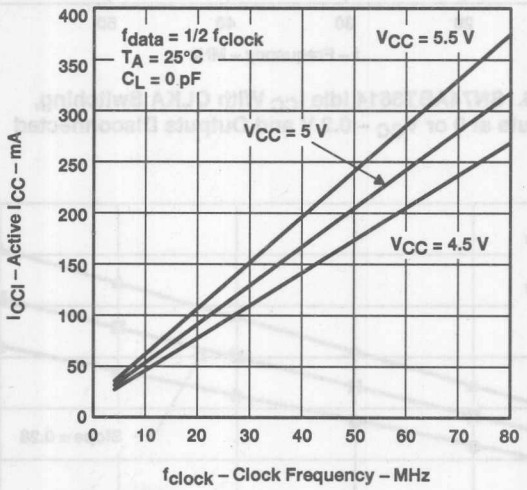


Figure 5. SN74ABT3614 Active I_{CC} With CLKA and CLKB Switching, Simultaneous Read/Write and CLKB as Data Output

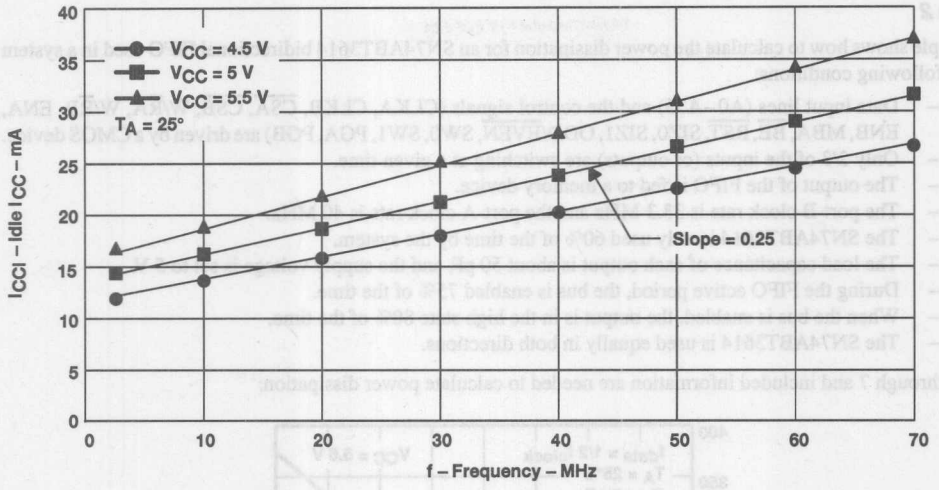


Figure 6. SN74ABT3614 Idle I_{CC} With CLKA Switching, Other Inputs at 0 or V_{CC} – 0.2 V and Outputs Disconnected

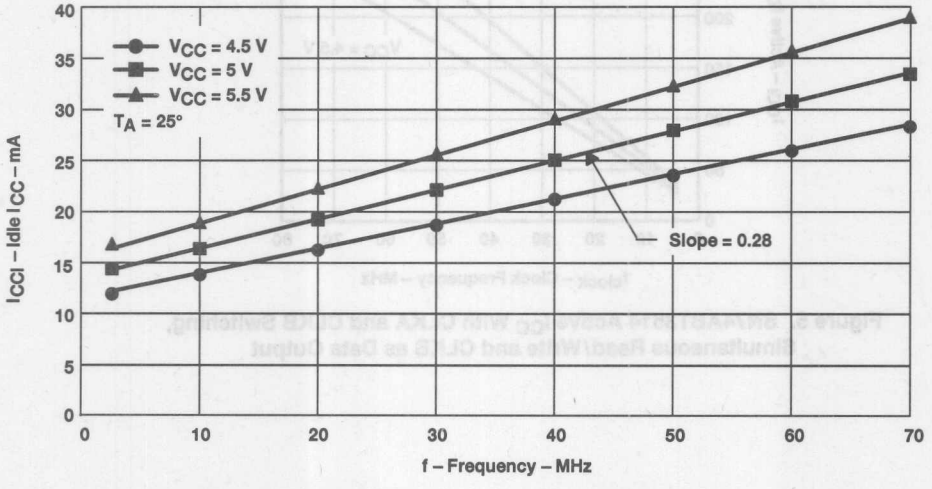


Figure 7. SN74ABT3614 Idle I_{CC} With CLKB Switching, Other Inputs at 0 or V_{CC} – 0.2 V and Outputs Disconnected

The following parametric values are needed to calculate power dissipation:

V_{CC} = supply voltage = 5 V
V_{OH} = V_{CC} – 1.3 V
V_{OL} = 0.3 V
DC_d = % time FIFO is switching = 0.6
$1 - DC_d$ = % time FIFO is not switching = 0.4
f_{clockA} = clock switching frequency of port A = 40 MHz
f_{clockB} = clock switching frequency of port B = 33.3 MHz
pF(A) = clock-A switching power factor, the slope of I_{CC} versus f_{clock} curve (see data sheet) = 0.25
pF(B) = clock-B switching power factor, the slope of I_{CC} versus f_{clock} curve (see data sheet) = 0.28
DC_{EN} = % duty cycle enabled = 0.75
I_{CCI} = $[f_{clockA} \times pF(A) + [f_{clockB} \times pF(B) = (40 \times 0.25) + (33.3 \times 0.28) = 19.32$ mA
I_{CCf} = idle supply current when FIFO is transferring data = 136.26 mA
I_{CCH} = active supply current when outputs are in high state (see data sheet) = 30 mA
I_{CCL} = power supply current when outputs are in low state (see data sheet) = 130 mA
I_{CCZ} = power supply current when outputs are in high-impedance state (see data sheet) = 30 mA
N_L/N_T = ratio of number of outputs in low state to total number of outputs = 0.2
N_H/N_T = ratio of number of outputs in high state to total number of outputs = 0.8
C_L = load capacitance = 50 pF
f_o = 1/2 (since maximum data rate is 1/2 clock frequency) × 2/3
(since 2/3 of the outputs are switching at a given time) × 33.3 MHz
(slowest of the the two clock frequencies, f_{clockA} or f_{clockB}) = 11.1 MHz

Solution

$$P_T = P_T \text{ (from A to B)} + P_T \text{ (from B to A)}$$
$$= P_q \text{ (from A to B)} + P_q \text{ (from B to A)} + P_d \text{ (from A to B)} + P_d \text{ (from B to A)}$$
$$= P_q + P_d$$

Where P_q and P_d include power from A to B and from B to A directions.

Quiescent Power

$$P_q = V_{CC} \times [DC_{EN} \times (N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T) + (1 - DC_{EN})I_{CCZ} + I_{CCI}]$$
$$= 5 \text{ V} \times [0.75 \times (0.8 \times 30 \text{ mA} + 0.2 \times 130 \text{ mA}) + (1 - 0.75)\ 30 \text{ mA} + 19.32 \text{ mA}]$$
$$= 5 \text{ V} \times [37.5 \text{ mA} + 7.5 \text{ mA} + 19.32 \text{ mA}] = 321.6 \text{ mW}$$

Dynamic Power

$$P_d = V_{CC} \times I_{CCf} + \Sigma[V_{CC} \times C_L \times (V_{OH} - V_{OL}) \times f_o]$$
$$= 5 \text{ V} \times 136.25 \text{ mA} + \Sigma[5 \times 50 \text{ pF} \times (5 \text{ V} - 1.3 - 0.3 \text{ V}) \times (11.1 \text{ MHz})]$$
$$= 681.25 \text{ mW} + (36 \times 9.44 \text{ mW}) = 681.25 \text{ mW} + 339.66 \text{ mW} = 1020.91 \text{ mW}$$

Total Power

$$P_T = P_d\ (DC_d) + P_q\ (1 - DC_d)$$
$$= 1020.91 \text{ mW} \times 0.6 + 321.6 \times 0.4 = 741.19 \text{ mW}$$

Therefore, total power is approximately:

$$P_T = 741.19 \text{ mW}$$

The SN74ABT3614 is available in 120-pin TQFP and 132-pin PQFP packages (refer to Appendix B for the maximum power curve calculated for reliability purposes). At maximum ambient temperature (70°C) and no air flow for the 132-pin PQFP and 120-pin TQFP packages, the maximum power that the package can dissipate to free air is 1610 mW and 1606 mW, respectively. The SN74ABT3614, in this example, meets the reliability requirement since 741.19 mW is much less than 1610 mW or 1606 mW.

Summary

Power-dissipation calculations are essential to meet the design requirements related to the chip temperature and the system power. In this application report, a simple method of calculating power is provided to assist the design engineer with power-dissipation calculations for TI CMOS and BiCMOS FIFO products. Total power includes quiescent power and dynamic power. For most applications using CMOS and BiCMOS FIFOs, dynamic power accounts for most of the power requirement. Examples of power-dissipation calculations are provided to show the practical use of this application report. In each example, the reliability of the chip was tested against the absolute maximum power dissipation in free air. For example, the total calculated power consumption for the SN74ACT3632 and SN74ABT3614 examples resulted in 484 mW and 741 mW, respectively. These values are much less than the maximum power dissipation of the 120-pin TQFP (1606 mW) or 132-pin PQFP (1610 mW) packages in still air. I_{CC} versus frequency curves are provided in Appendix A. These graphs assist the design engineer in the search for the FIFO device with the minimum power consumption. After total power is calculated for a system, the design engineer can ensure that this value does not exceed the maximum power capability of the package type. The table of maximum power versus ambient temperature for different package options are included in Appendix B.

Acknowledgements

The author would like to express her appreciation to Kam Kittrell for his editorial comments and Al Sawyer for his assistance in providing the I_{CC} versus frequency curves in Appendix A.

Appendix A
Graphs of I_{CC} Versus Frequency

The following information is provided to assist the designer with the power-consumption calculations. Graphs of I_{CC} versus frequency are shown for the SN74ACT7803, SN74ACT7811, SN74ACT3641, SN74ACT7807, and SN74ABT7819. While the FIFOs were idle, data was taken on five units on an automatic test machine (HP 82000). Five readings were taken for each frequency and the average was used to plot the graphs. The tests were done by setting V_{IL} and V_{IH} as shown below:

V_{IL} = 0 V
V_{IH} = V_{CC} – 0.2 V

For each of the FIFOs, two graphs are provided for idle I_{CC}. One graph shows the I_{CC} versus frequency when WRTCLK is running, whereas the other graph shows the I_{CC} versus frequency when RDCLK is running. The slope of the 5-V supply voltage curve is calculated for both graphs and the largest of the two slopes is used as the power factor for power calculations.

The slopes of the I_{CCI} versus frequency graphs in the tests performed were 0.09 (SN74ACT7807), 0.12 (SN74ACT7803, SN74ACT7811), 0.2 (SN74ACT3641), and 0.28 (SN74ABT3614); therefore, if the slope of the I_{CCI} versus frequency plot is not readily available, it is appropriate to estimate the slope as 0.2.

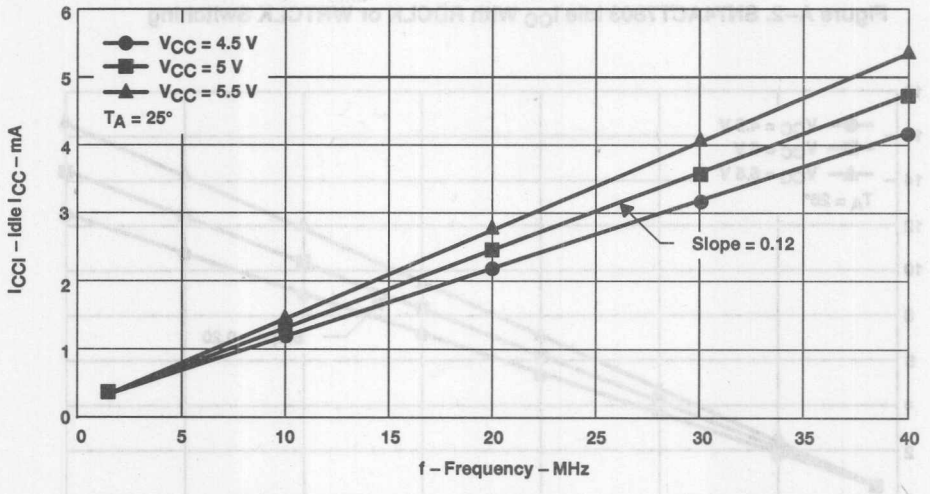


Figure A–1. SN74ACT7811 Idle I_{CC} With RDCLK or WRTCLK Switching

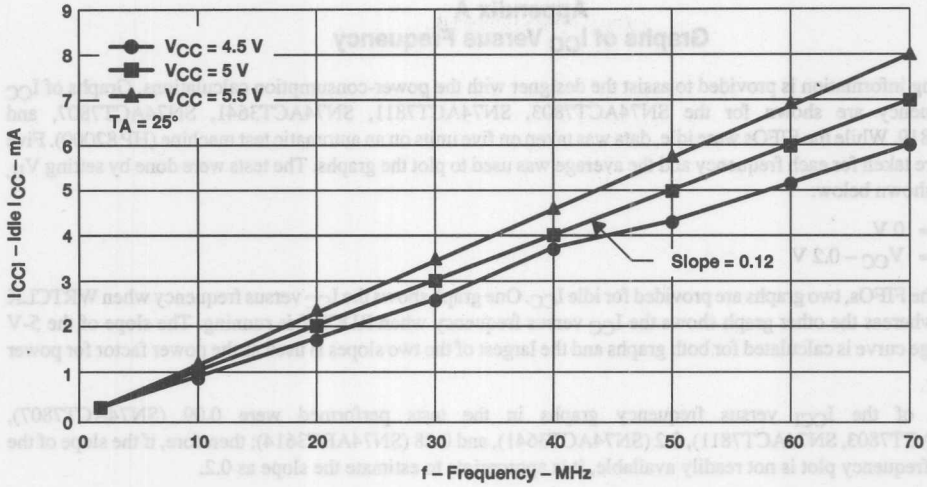


Figure A–2. SN74ACT7803 Idle I_{CC} With RDCLK or WRTCLK Switching

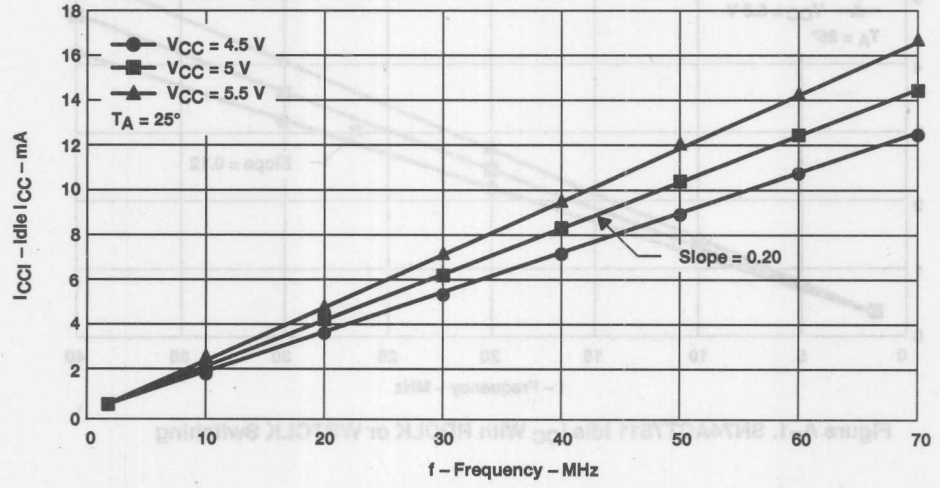


Figure A–3. SN74ACT3641 Idle I_{CC} With CLKA Switching

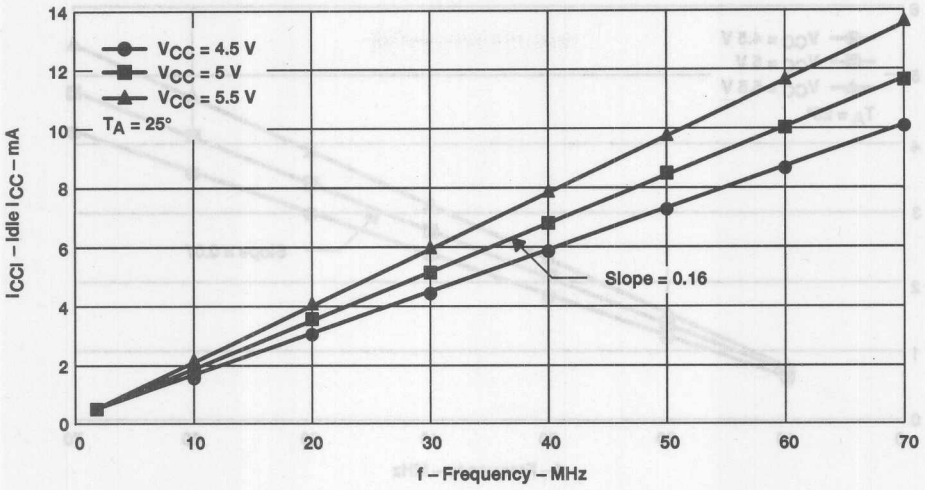


Figure A–4. SN74ACT3641 Idle I_{CC} With CLKB Switching

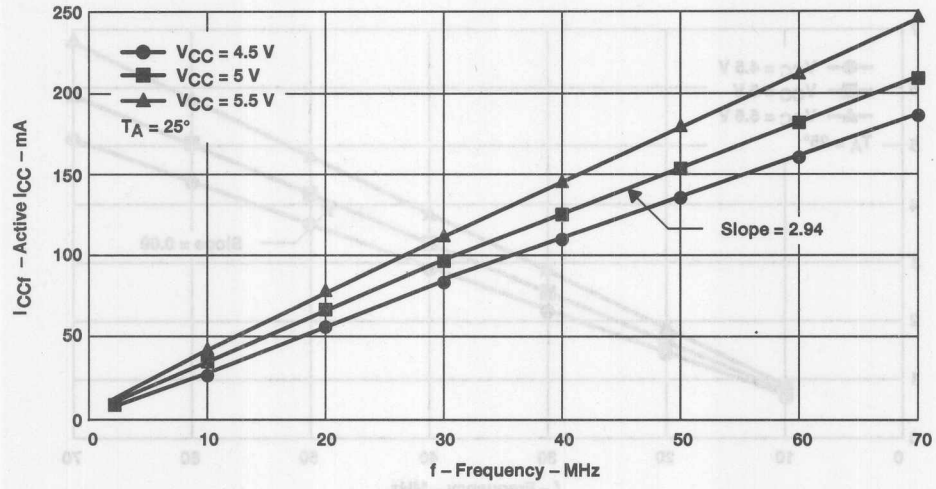


Figure A–5. SN74ACT3641 Active I_{CC} With CLKA and CLKB Switching, Simultaneous Read/Write and CLKB as Data Output

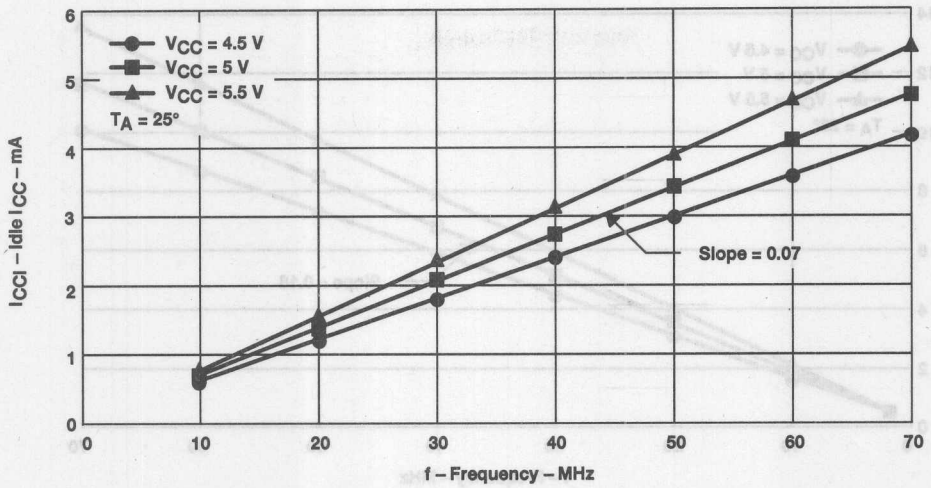


Figure A–6. SN74ACT7807 Idle I_{CC} With WRTCLK Switching, Other Inputs at 0 or V_{CC} – 0.2 V and Outputs Disconnected

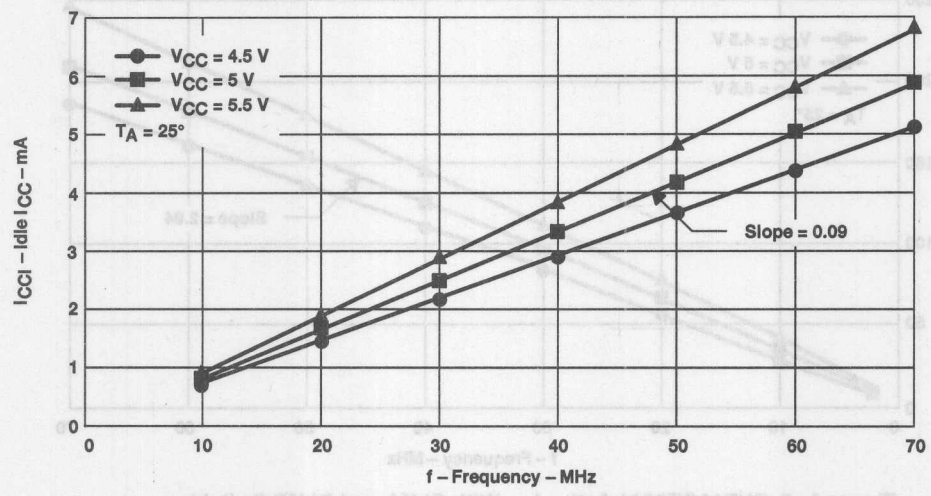


Figure A–7. SN74ACT7807 Idle I_{CC} With RDCLK Switching, Other Inputs at 0 or V_{CC} – 0.2 V and Outputs Disconnected

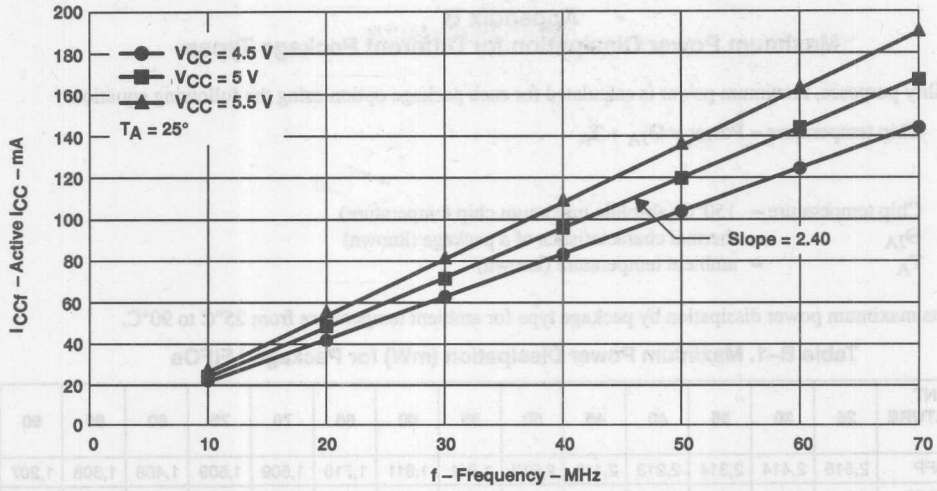


Figure A–8. SN74ACT7807 Active I_{CC} With Simultaneous Read/Write

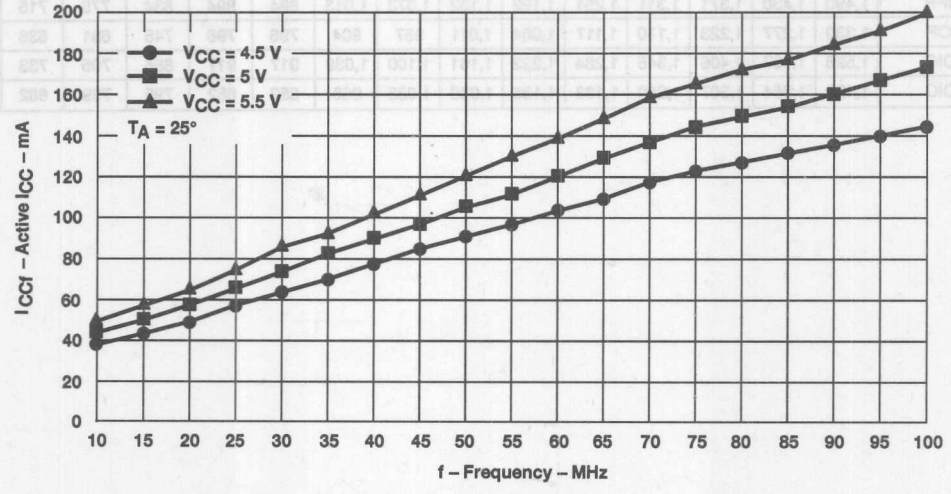


Figure A–9. SN74ABT7819 Active I_{CC} Versus Frequency

Appendix B
Maximum Power Dissipation for Different Package Types

For reliability purposes, maximum power is calculated for each package option using the following equation:

$$\text{Chip temperature} = \text{Power} \times \Theta_{JA} + T_A$$

Where:

Chip temperature = 150°C (absolute maximum chip temperature)
Θ_{JA} = thermal characteristics of a package (known)
T_A = ambient temperature (known)

Table 1 lists maximum power dissipation by package type for ambient temperature from 25°C to 90°C.

Table B–1. Maximum Power Dissipation (mW) for Packaged FIFOs

AMBIENT TEMPERATURE (°C)	25	30	35	40	45	50	55	60	65	70	75	80	85	90
PQ132 PQFP	2,515	2,414	2,314	2,213	2,113	2,012	1,911	1,811	1,710	1,509	1,509	1,408	1,308	1,207
PCB120 TQFP	2,510	2,410	2,309	2,209	2,108	2,008	1,908	1,807	1,707	1,505	1,505	1,406	1,305	1,205
PN80 TQFP	1,424	1,367	1,310	1,253	1,196	1,139	1,082	1,025	968	854	854	797	740	683
PM64 TQFP	1,351	1,297	1,243	1,189	1,135	1,081	1,027	973	919	811	811	757	703	649
PH80 PQFP	1,490	1,430	1,371	1,311	1,251	1,192	1,132	1,073	1,013	894	894	834	775	715
DL56 SSOP	1,330	1,277	1,223	1,170	1,117	1,064	1,011	957	904	798	798	745	691	638
DW28 SOIC	1,528	1,467	1,406	1,345	1,284	1,222	1,161	1,100	1,039	917	917	856	795	733
DW24 SOIC	1,420	1,364	1,307	1,250	1,193	1,136	1,080	1,023	966	852	852	795	739	682

Single-Bit FIFOs

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Sample Power-Dissipation Calculations for SN74ACT2229

This example shows power-dissipation calculations for the SN74ACT2229 FIFO used in a system under the conditions below. On board the SN74ACT2229 are two separate and independent FIFOs. The calculation below is for only one FIFO: FIFO1 is assumed active and FIFO2 is assumed idle.

Assumed Conditions

- Data input line (1D) is driven by a TTL device.
- Control signals (1WRTCLK, 1RDCLK, 1$\overline{\text{RESET}}$, 1WRTEN, 1OE, 1RDEN) are driven by a CMOS device.
- The input (or output) is switching at a given time.
- The RDCLK clock rate is 33.3 MHz and the WRTCLK clock rate is 40 MHz.
- The SN74ACT2229 is used about 1/3 of the time by the system.
- The load capacitance on each output is about 30 pF, and the supply voltage is 5 V.

The following parametric values are needed to calculate power dissipation:

V_{CC}	=	5 V (assumed condition)
DC_d	=	1/3 (assumed condition)
f_{WRTCLK}	=	40 MHz (assumed condition)
f_{RDCLK}	=	33.3 MHz (assumed condition)
pF	=	0.2 mA/MHz (worst-case approximation)
I_{CCI}	=	$(f_{WRTCLK} + f_{RDCLK}) \times pF = 14.7$ mA (calculated, see equation 2 in the introduction to Section 4)
N_{TTL}	=	1 (assumed condition)
I_{CCF}	=	20 mA @ 33.3 MHz (from active I_{CC} versus frequency plot)
ΔI_{CC}	=	1 mA (see data sheet)
DC_{VIH}	=	1 (assumed condition)
C_L	=	30 pF (assumed condition)
f_o	=	$(0.5) \times (1) \times (33.3 \text{ MHz}) = 16.7$ MHz (calculated, see equation 4 in the introduction to Section 4)

Solution

Quiescent Power

$$\begin{aligned} P_T &= V_{CC} \times [I_{CCI} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] \\ &= 5 \text{ V} \times [14.7 \text{ mA} + (1 \times 1 \text{ mA} \times 1)] \\ &= 78.3 \text{ mW} \end{aligned} \quad (1)$$

Dynamic Power

$$\begin{aligned} P_q &= V_{CC} \times [I_{CCf} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] + \Sigma(C_L \times V_{CC}^2 \times f_o) \\ &= 5 \text{ V} \times [20 \text{ mA} + (1 \times 1 \text{ mA} \times 1)] + [30 \text{ pF} \times (5 \text{ V})2 \times 16.7 \text{ MHz}] \\ &= 117.5 \text{ mW} \end{aligned} \quad (2)$$

Total Power

$$\begin{aligned} P_T &= (P_d \times DC_d) + [P_q \times (1\text{-}DC_d)] \\ &= (117.5 \text{ mW} \times 1/3) + (78.3 \text{ mW} \times 2/3) \\ &= 91.4 \text{ mW} \end{aligned} \quad (3)$$

Therefore, the total power is approximately 91 mW.

Power Characteristics

The SN74ACT2229 is available in the 24-pin SOIC and 28-pin SOIC packages. The maximum power-dissipation capabilities of these packages for varying ambient temperatures and air flows can be found in Section 5 of this handbook. At an ambient temperature of 70°C with no air flow, the maximum power that each of these packages can dissipate to free air is 909 mW and 978 mW, respectively. The total power dissipation of the SN74ACT2229 with one input (or output) switching falls well within the thermal budget of either of these packages.

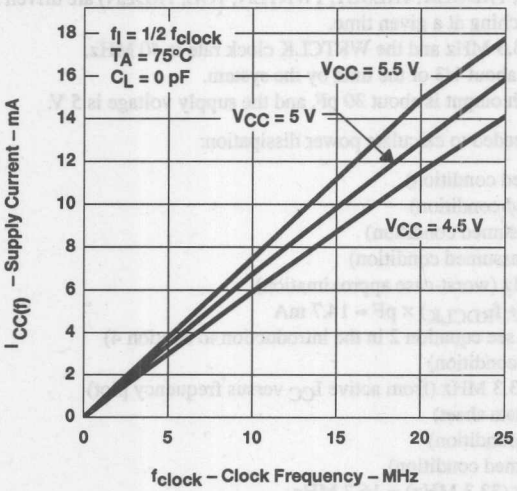


Figure 1. SN74ACT2226 and SN74ACT2228 Single FIFO Supply Current Versus Clock Frequency

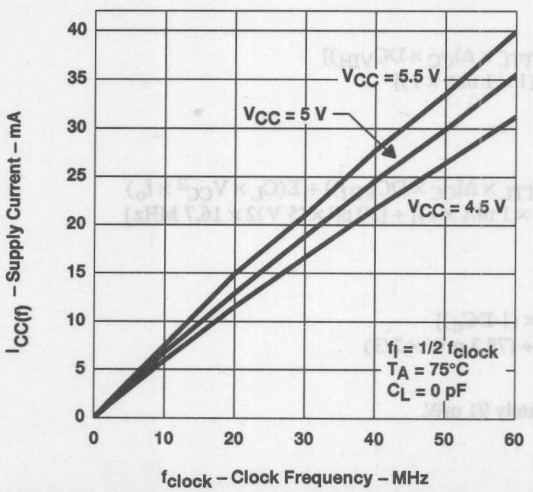


Figure 2. SN74ACT2227 and SN74ACT2229 Single FIFO Supply Current Versus Clock Frequency

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Sample Power-Dissipation Calculations for SN74ABT3613

This example shows the power-dissipation calculations for the SN74ABT3613 unidirectional FIFO used in a system under the following conditions.

Assumed Conditions

- Data input (A0–A35) and control signals (CLKA, CLKB, $\overline{CSA}$, $\overline{CSB}$, ENA, ENB, FSO, FS1, MBA, $\overline{RST}$, ODD/$\overline{EVEN}$, W/$\overline{RA}$, W/$\overline{RB}$, $\overline{BE}$, SIZ0, SIZ1, SW0, SW1, PGA, PGB) are driven by a CMOS device.
- 36 inputs (or 36 outputs) are switching at a given time.
- The port-B clock rate is 33.3 MHz and the port-A clock rate is 40 MHz.
- The SN74ABT3613 is used about 60% of the time by the system.
- The load capacitance on each output is about 50 pF and the supply voltage is 5 V.
- During the FIFO active period, the bus is enabled 75% of the time.
- When the bus is enabled, the output is in the high state 80% of the time.

The following parametric values are needed to calculate power dissipation:

V_{CC} = 5 V (assumed condition)
V_{OH} = V_{CC} – 1.3 V
V_{OL} = 0.3 V
DC_d = 0.6 (assumed condition)
f_{CLKA} = 40 MHz (assumed condition)
f_{CLKB} = 33.3 MHz (assumed condition)
pF = 0.265 mA/MHz (assumption based on data for the SN74ABT3614)
DC_{EN} = 0.75 (assumed condition)
I_{CCI} = $(f_{CLKA} + f_{CLKB}) \times pF$ = 19.4 mA
(calculated, see equation 7 in the introduction to Section 4)
I_{CCF} = 136 mA @ 33.3 MHz (from active I_{CC} versus frequency plot)
I_{CCH} = 30 mA (see data sheet)
I_{CCL} = 130 mA (see data sheet)
I_{CCZ} = 30 mA (see data sheet)
N_L/N_T = 0.2 (assumed condition)
N_H/N_T = 0.8 (assumed condition)
C_L = 50 pF (assumed condition)
f_o = $(0.5) \times (1) \times (33.3\ MHz)$ = 16.7 MHz
(calculated, see equation 9 in the introduction to Section 4)

Solution

Quiescent Power

$$P_q = V_{CC} \times [DC_{EN} \times (N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T) + (1\text{-}DC_{EN}) \times I_{CCZ} + I_{CCI}] \quad (1)$$
$$= 5\ V \times [0.75\ mA \times (0.8 \times 30\ mA + 0.2 \times 130\ mA) + (0.25) \times 30\ mA + 19.4\ mA]$$
$$= 322\ mW$$

Dynamic Power

$$P_q = V_{CC} \times I_{CCf} + \Sigma[V_{CC} \times C_L \times (V_{OH} \times V_{OL}) \times f_o] \quad (2)$$
$$= 5\ V \times 136\ mA + (36 \times 5\ V \times 50\ pF \times (5\ V - 1.3\ V - 0.3\ V) \times 16.7\ MHz)$$
$$= 1191\ mW$$

Total Power

$$P_T = (P_d \times DC_d) + [P_q \times (1\text{-}DC_d)] \quad (3)$$
$$= (1191\ mW)\ (0.6) + (322\ mW)\ (0.4)$$
$$= 843.4\ mW$$

Therefore, the total power is approximately 843 mW.

Power Characteristics

The SN74ABT3613 is available in the 120-pin TQFP and 132-pin PQFP packages. The maximum power-dissipation capabilities of these packages for varying ambient temperatures and air flows can be found in Section 5 of this handbook. At an ambient temperature of 70°C with no air flow, the maximum power that each of these packages can dissipate to free air is 1606 mW and 1610 mW, respectively. The total power dissipation of the SN74ABT3613, under the rather severe conditions of 36 inputs (or 36 outputs) switching simultaneously, falls well within the thermal budget of either of these packages.

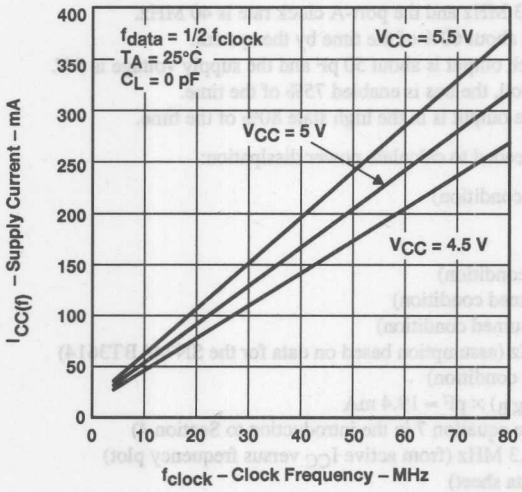


Figure 1. SN74ABT3611 Supply Current Versus Clock Frequency

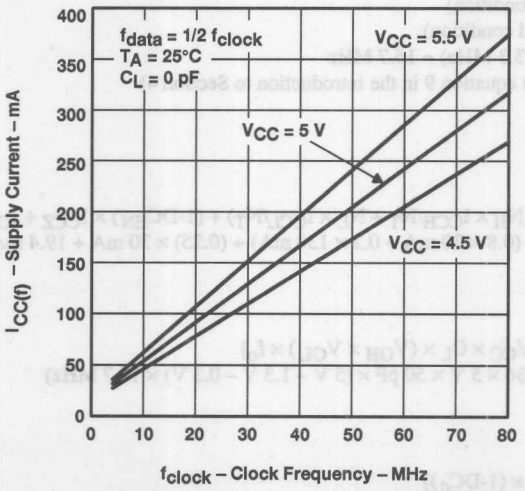


Figure 2. SN74ABT3612 Supply Current Versus Clock Frequency

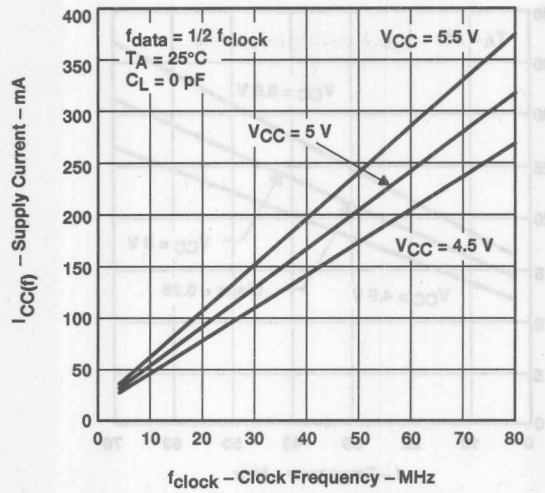


Figure 3. SN74ABT3613 Supply Current Versus Clock Frequency

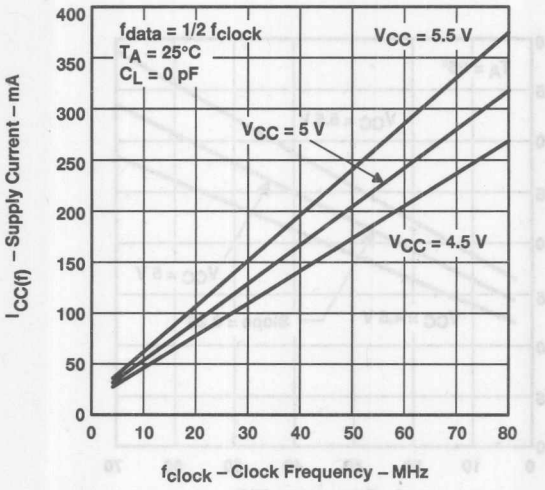


Figure 4. SN74ABT3614 Supply Current Versus Clock Frequency

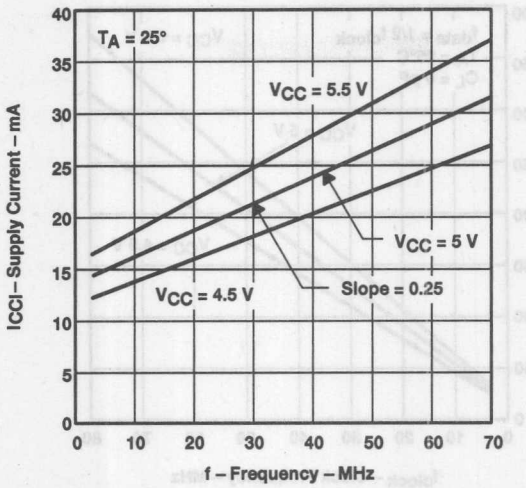


Figure 5. SN74ABT3614 Idle Current With CLKA Switching, Other Inputs at 0 or V_{CC} – 0.2 V and Outputs Disconnected

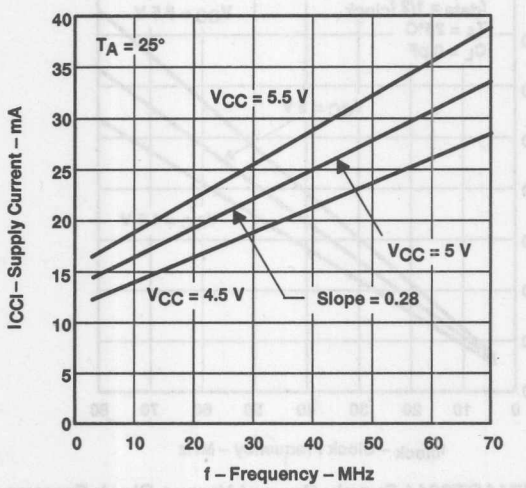


Figure 6. SN74ABT3614 Idle Current With CLKB Switching, Other Inputs at 0 or V_{CC} – 0.2 V and Outputs Disconnected

Sample Power-Dissipation Calculations for SN74ACT3641

This example shows power-dissipation calculations for the SN74ACT3641 unidirectional FIFO used in a system under the following conditions.

Assumed Conditions

- Data input (A0–A35) are driven by a TTL device.
- Control signals (CLKA, CLKB, $\overline{\text{CSA}}$, $\overline{\text{CSB}}$, ENA, ENB, FSO, FS1, MBA, MBB, RFM, RTM, $\overline{\text{RST}}$, W/$\overline{\text{R}}$A, $\overline{\text{W}}$/RB) are driven by a CMOS device.
- 36 inputs (or 36 outputs) are switching at a given time.
- The port-B clock rate is 33.3 MHz and the port-A clock rate is 40 MHz.
- The SN74ACT3641 is used about 1/3 of the time by the system.
- The load capacitance on each output is about 30 pF, and the supply voltage is 5 V.

The following parametric values are needed to calculate power dissipation:

V_{CC} = 5 V (assumed condition)
DC_d = 1/3 (assumed condition)
f_{CLKA} = 40 MHz (assumed condition)
f_{CLKB} = 33.3 MHz (assumed condition)
pF(A) = 0.20 mA/MHz (from idle I_{CC} versus frequency plot, CLKA switching)
pF(B) = 0.16 mA/MHz (from idle I_{CC} versus frequency plot, CLKB switching)
DC_{EN} = 0.75 (assumed condition)
I_{CCI} = $[f_{CLKA} \times pF(A)\} + [f_{CLKB} \times pF(B)]$ = 13.3 mA
(calculated, see equation 2 in the introduction to Section 4)
N_{TTL} = 36 (assumed condition)
I_{CCf} = 100 mA @ 33.3 MHz (from active I_{CC} versus frequency plot)
I_{CC} = 1 mA (assumed condition)
C_L = 30 pF (assumed condition)
f_o = (0.5) × (1) × (33.3 MHz) = 16.7 MHz
(calculated, see equation 4 in the introduction to Section 4)

Solution

Quiescent Power

$$P_q = V_{CC} \times [I_{CCI} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] \quad (1)$$
$$= 5\text{ V} \times [13.3\text{ mA} + 36 \times 1\text{ mA} \times 1)]$$
$$= 246.5\text{ mW}$$

Dynamic Power

$$P_d = V_{CC} \times [I_{CCf} + (NTTL \times \Delta I_{CC} \times DC_{VIH})] + \Sigma[C_L \times (V_{CC}^2 \times f_o)] \quad (2)$$
$$= 5\text{ V} \times [100\text{ mA} + (36 \times 1\text{ mA} \times 1)] + [36 \times 30\text{ pF} \times (5\text{ V})^2 \times 16.7\text{ MHz})$$
$$= 1130.9\text{ mW}$$

Total Power

$$P_T = (P_d \times DC_d) + [P_q \times (1\text{-}DC_d)] \quad (3)$$
$$= (1130.9\text{ mW} \times 1/3) + (246.5\text{ mW} \times 2/3)$$
$$= 541.3\text{ mW}$$

Therefore, the total power is approximately 541 mW.

Power Characteristics

The SN74ACT3641 is available in the 120-pin TQFP and 132-pin PQFP packages. The maximum power-dissipation capabilities of these packages for varying ambient temperatures and air flows can be found in Section 5 of this handbook. At an ambient temperature of 70°C with no air flow, the maximum power that each of these packages can dissipate to free air is 1606 mW and 1610 mW, respectively. The total power dissipation of the SN74ACT3641, under the rather severe conditions of 36 inputs (or 36 outputs) switching simultaneously, falls well within the thermal budget of either of these packages.

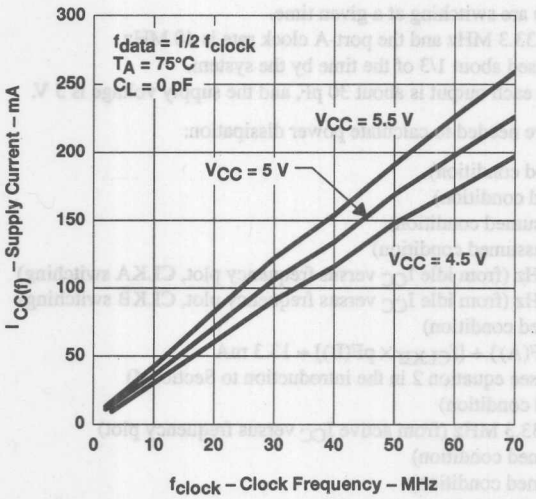


Figure 1. SN74ACT3632 Supply Current Versus Clock Frequency

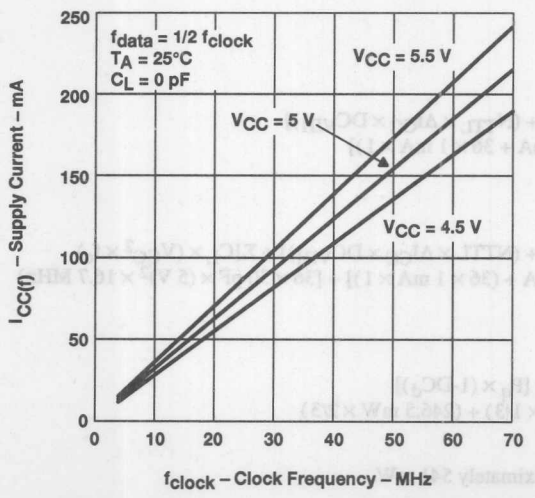


Figure 2. SN74ACT3638 Supply Current Versus Clock Frequency

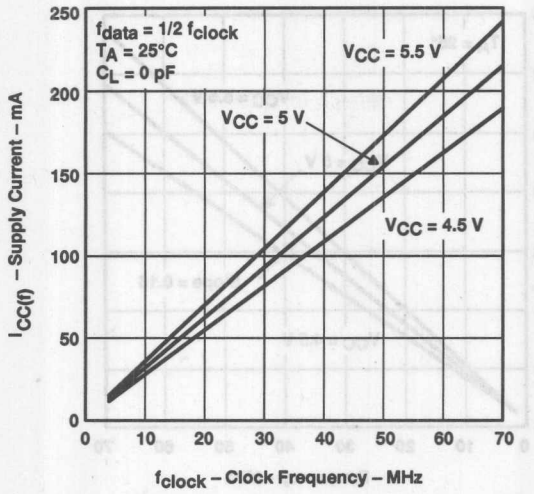


Figure 3. SN74ACT3631 and SN74ACT3641 Supply Current Versus Clock Frequency

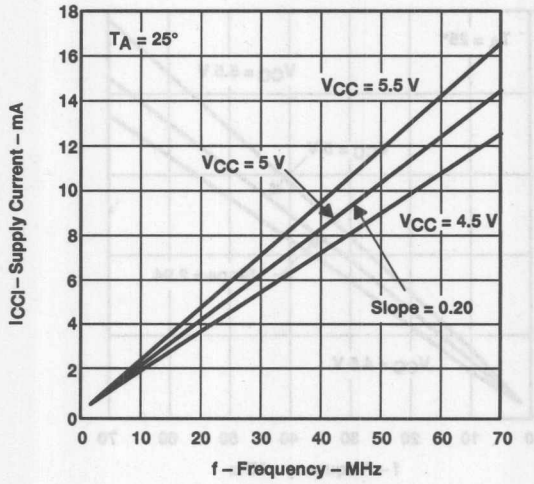


Figure 4. SN74ACT3641 Idle Current With CLKA Switching

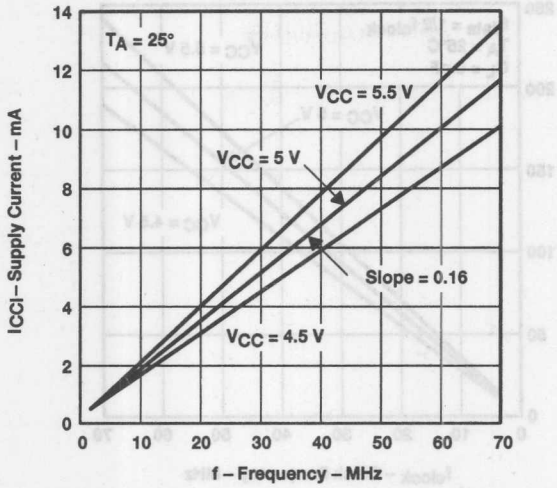


Figure 5. SN74ACT3641 Idle Current With CLKB Switching

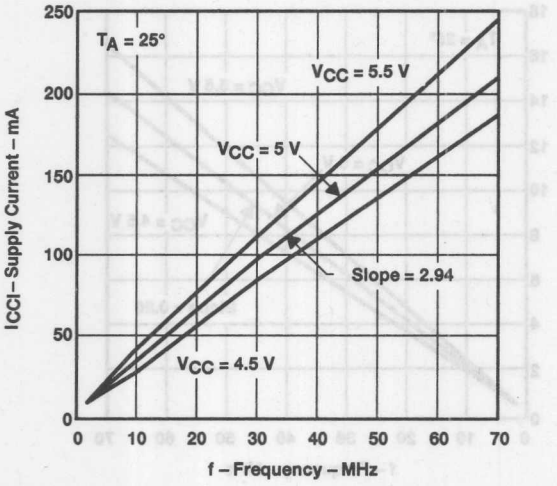


Figure 6. SN74ACT3641 Active Current With CLKA and CLKB Switching, Simultaneous Read/Write and CLKB as Data Output

18-Bit Clocked/Strobed FIFOs

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Sample Power-Dissipation Calculations for SN74ABT7819

This example shows power-dissipation calculations for the SN74ABT7819 unidirectional FIFO used in a system under the following conditions.

Assumed Conditions

- Data input lines (A0–A17) and control signals (CLKA, CLKB, $\overline{\text{CSA}}$, $\overline{\text{CSB}}$, RENA, RENB, WENA, WENB, $\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$, $\overline{\text{PENA}}$, $\overline{\text{PENB}}$, W/$\overline{\text{RA}}$, W/$\overline{\text{RB}}$) are driven by a CMOS device.
- 18 inputs (or 18 outputs) are switching at a given time.
- The port-B clock rate is 33.3 MHz and the port-A clock rate is 40 MHz.
- The SN74ABT7819 is used about 60% of the time by the system.
- The load capacitance on each output is about 50 pF, and the supply voltage is 5 V.
- During the FIFO active period, the bus is enabled 75% of the time.
- When the bus is enabled, the output is in the high state 80% of the time.

The following parametric values are needed to calculate power dissipation:

V_{CC} = 5 V (assumed condition)
V_{OH} = V_{CC} – 1.3 V
V_{OL} = 0.3 V
DC_d = 0.6 (assumed condition)
f_{CLKA} = 40 MHz (assumed condition)
f_{CLKB} = 33.3 MHz (assumed condition)
pF = 0.2 mA/MHz (worst-case assumption)
DC_{EN} = 0.75 (assumed condition)
I_{CCI} = $(f_{CLKA} + f_{CLKB}) \times pF$ = 14.7 mA
(calculated, see equation 7 in the introduction to Section 4)
I_{CCf} = 75 mA @ 33.3 MHz (from active I_{CC} versus frequency plot)
I_{CCH} = 15 mA (see data sheet)
I_{CCL} = 95 mA (see data sheet)
I_{CCZ} = 15 mA (see data sheet)
N_L/N_T = 0.2 (assumed condition)
N_H/N_T = 0.8 (assumed condition)
C_L = 50 pF (assumed condition)
f_o = $(0.5) \times (1) \times (33.3 \text{ MHz})$ = 16.7 MHz
(calculated, see equation 9 in the introduction to Section 4)

Solution

Quiescent Power

$$P_q = V_{CC} \times [DC_{EN} \times (N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T) + (1 - DC_{EN}) \times I_{CCZ} + I_{CCI}] \quad (1)$$
$$= 5 \text{ V} \times [0.75 \times (0.8 \times 15 \text{ mA} + 0.2 \times 95 \text{ mA}) + (0.25) \times 15 \text{ mA} + 14.7 \text{ mA}]$$
$$= 208.5 \text{ mW}$$

Dynamic Power

$$P_d = V_{CC} \times I_{CCf} + \Sigma[V_{CC} \times C_L \times (V_{OH} - V_{OL}) \times f_o] \quad (2)$$
$$= 5 \text{ V} \times [100 \text{ mA} + (36 \times 1 \text{ mA} \times 1)] + [36 \times 30 \text{ pF} \times (5 \text{ V})^2 \times 16.7 \text{ MHz}]$$
$$= 630.5 \text{ mW}$$

Total Power

$$P_T = (P_d \times DC_d) + [P_q \times (1\text{-}DC_d)] \quad (3)$$
$$= (630.5 \text{ mW})\ (0.6) + (208.5 \text{ mW})\ (0.4)$$
$$= 461.7 \text{ mW}$$

Therefore, the total power is approximately 462 mW.

Power Characteristics

The SN74ABT7819 is available in the 80-pin TQFP and 80-pin PQFP packages. The maximum power-dissipation capabilities of these packages for varying ambient temperatures and air flows can be found in Section 5 of this handbook. At an ambient temperature of 70°C with no air flow, the maximum power that each of these packages can dissipate to free air is 911 mW and 954 mW, respectively. The total power dissipation of the SN74ABT7819, under the rather severe conditions of 18 inputs (or 18 outputs) switching simultaneously, falls well within the thermal budget of either of these packages.

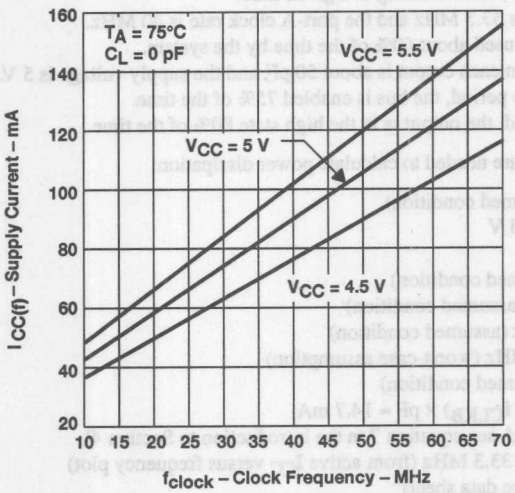


Figure 1. SN74ABT7819 Supply Current Versus Clock Frequency

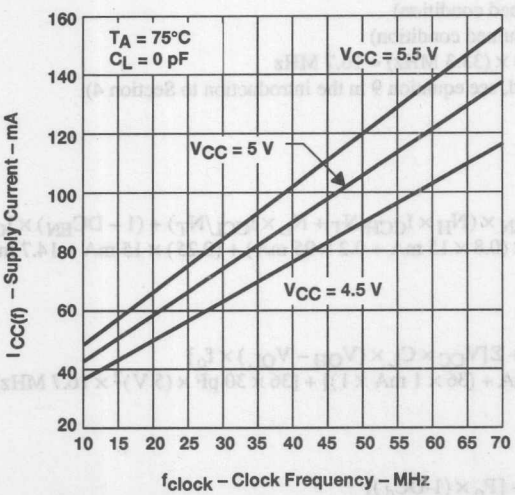


Figure 2. SN74ABT7820 Supply Current Versus Clock Frequency

Sample Power-Dissipation Calculations for SN74ACT7803

This example shows power-dissipation calculations for the SN74ACT7803 unidirectional FIFO used in a system under the following conditions.

Assumed Conditions

- Data input lines (D0–D17) are driven by a TTL device.
- Control signals (WRTCLK, RDCLK, $\overline{\text{RESET}}$, WRTEN1, $\overline{\text{WRTEN2}}$, $\overline{\text{OE1}}$, $\overline{\text{OE2}}$, $\overline{\text{RDEN}}$, $\overline{\text{PEN}}$) are driven by a CMOS device.
- 18 inputs (or 18 outputs) are switching at a given time.
- The RDCLK clock rate is 33.3 MHz and the WRTCLK clock rate is 40 MHz.
- The SN74ACT7803 is used about 1/3 of the time by the system.
- The load capacitance on each output is about 30 pF, and the supply voltage is 5 V.

The following parametric values are needed to calculate power dissipation:

V_{CC} = 5 V (assumed condition)
DC_d = 1/3 (assumed condition)
f_{WRTCLK} = 40 MHz (assumed condition)
f_{RDCLK} = 33.3 MHz (assumed condition)
pF = 0.12 mA/MHz (from idle I_{CC} versus frequency plot)
DC_{EN} = 0.75 (assumed condition)
I_{CCI} = $(f_{WRTCLK} + f_{RDCLK}) \times pF = 8.8$ mA
(calculated, see equation 2 in the introduction to Section 4)
N_{TTL} = 18 (assumed condition)
I_{CCf} = 75 mA @ 33.3 MHz (from active I_{CC} versus frequency plot)
ΔI_{CC} = 1 mA (see data sheet)
I_{CCL} = 95 mA (see data sheet)
DC_{VIH} = 1 mA (see data sheet)
C_L = 30 pF (assumed condition)
f_o = $(0.5) \times (1) \times (33.3 \text{ MHz}) = 16.7$ MHz
(calculated, see equation 4 in the introduction to Section 4)

Solution

Quiescent Power

$$P_q = V_{CC} \times [I_{CCI} + N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] \quad (1)$$
$$= 5 \text{ V} \times [0.75 \times (8.8 \text{ mA} + (18 \times 1 \text{ mA} \times 1)]$$
$$= 134 \text{ mW}$$

Dynamic Power

$$P_d = V_{CC} \times [I_{CCf} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] + \Sigma(C_L \times V_{CC}^2 \times f_o) \quad (2)$$
$$= 5 \text{ V} \times [75 \text{ mA} + (18 \times 1 \text{ mA} \times 1)] + [18 \times 30 \text{ pF} \times (5 \text{ V})^2 \times 16.7 \text{ MHz}]$$
$$= 690.5 \text{ mW}$$

Total Power

$$P_T = (P_d \times DC_d) + [P_q \times (1\text{-}DC_d)] \quad (3)$$
$$= (690.5 \text{ mW} \times 1/3) + (134 \text{ mW} \times 2/3)$$
$$= 319.5 \text{ mW}$$

Therefore, the total power is approximately 320 mW.

Power Characteristics

The SN74ACT7803 is available in the 56-pin SSOP package. The maximum power-dissipation capabilities of these packages for varying ambient temperatures and air flows can be found in Section 5 of this handbook. At an ambient temperature of 70°C with no air flow, the maximum power that the 56-pin SSOP package can dissipate to free air is 851 mW. The total power dissipation of the SN74ACT7803, under the rather severe conditions of 18 inputs (or 18 outputs) switching simultaneously, falls well within the thermal budget of either of this package.

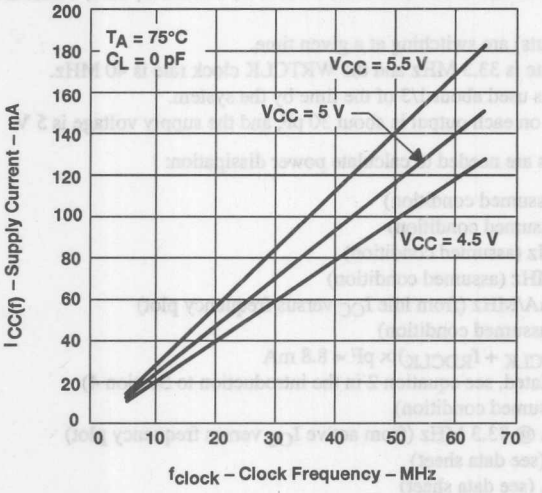


Figure 1. SN74ACT7804 Supply Current Versus Clock Frequency

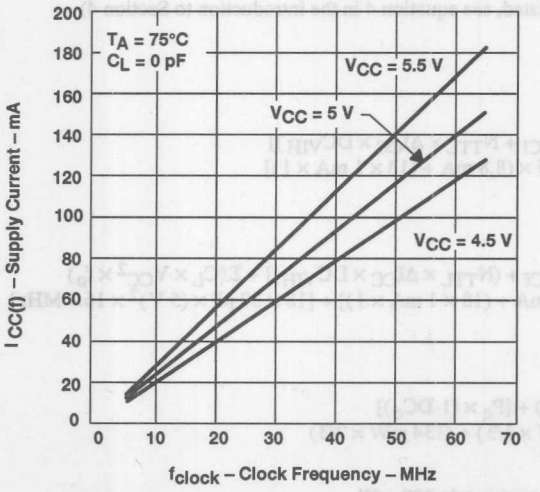


Figure 2. SN74ACT7806 Supply Current Versus Clock Frequency

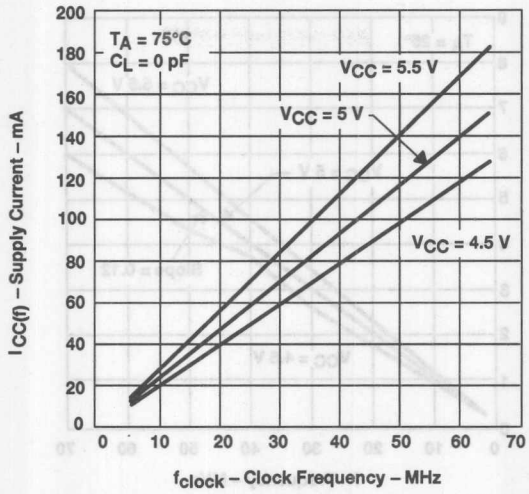


Figure 3. SN74ACT7814 Supply Current Versus Clock Frequency

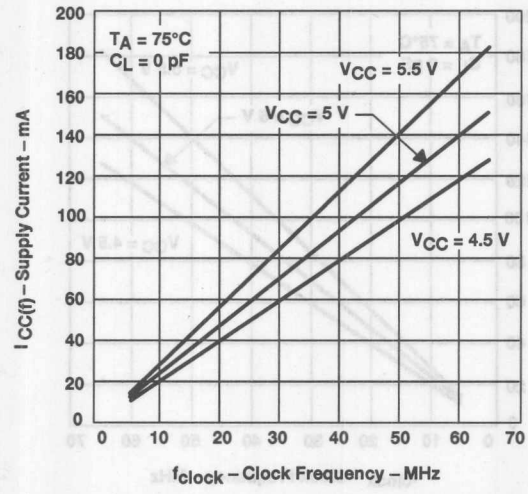


Figure 4. SN74ACT7803 Supply Current Versus Clock Frequency

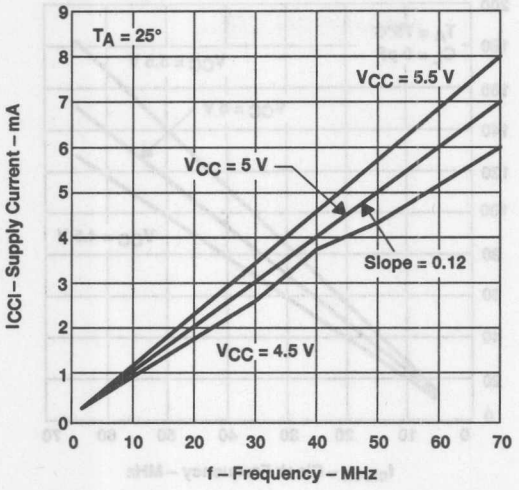


Figure 5. SN74ACT7803 Idle Current With RDCLK or WRTCLK Switching

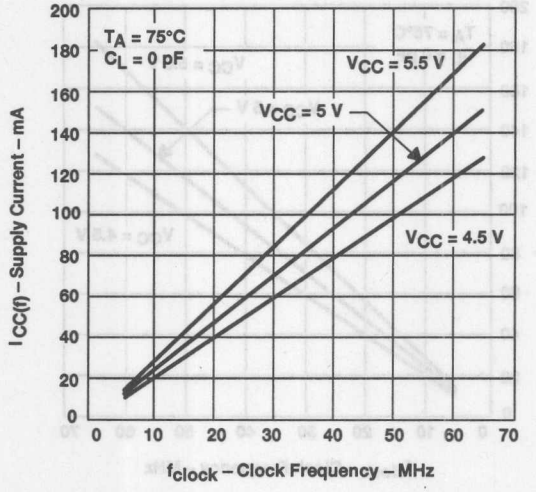


Figure 6. SN74ACT7805 Supply Current Versus Clock Frequency

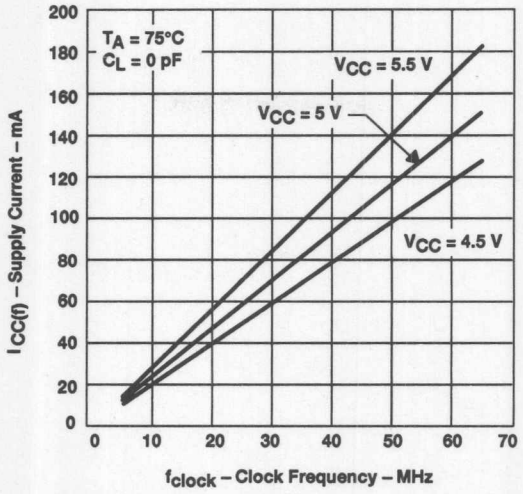


Figure 7. SN74ACT7813 Supply Current Versus Clock Frequency

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Sample Power-Dissipation Calculations for SN74ACT7807

This example shows power-dissipation calculations for the SN74ACT7807 unidirectional FIFO used in a system under the following conditions.

Assumed Conditions

- Data input lines (D0–D8) are driven by a TTL device.
- Control signals (WRTCLK, RDCLK, $\overline{\text{RESET}}$, WRTEN1, WRTEN2, OE, RDEN1, RDEN2, $\overline{\text{PEN}}$) are driven by a CMOS device.
- Nine inputs (or nine outputs) are switching at a given time.
- The RDCLK clock rate is 33.3 MHz and the WRTCLK clock rate is 40 MHz.
- The SN74ACT7807 is used about 1/3 of the time by the system.
- The load capacitance on each output is about 30 pF, and the supply voltage is 5 V.

The following parametric values are needed to calculate power dissipation:

V_{CC}	=	5 V (assumed condition)
DC_d	=	1/3 (assumed condition)
f_{WRTCLK}	=	40 MHz (assumed condition)
f_{RDCLK}	=	33.3 MHz (assumed condition)
$pF_{(WRTCLK)}$	=	0.07 mA/MHz (from idle I_{CC} versus frequency plot)
$pF_{(RDCLK)}$	=	0.09 mA/MHz (from idle I_{CC} versus frequency plot)
DC_{EN}	=	0.75 (assumed condition)
I_{CCI}	=	$(f_{WRTCLK} \times pF_{(WRTCLK)}) + (f_{RDCLK} \times pF_{(RDCLK)})$ = 5.8 mA (calculated, see equation 2 in the introduction to Section 4)
N_{TTL}	=	9 (assumed condition)
I_{CCf}	=	65 mA @ 33.3 MHz (from active I_{CC} versus frequency plot)
ΔI_{CC}	=	1 mA (assumed, from data sheet)
I_{CCL}	=	95 mA (see data sheet)
DC_{VIH}	=	1 mA (assumed condition)
C_L	=	30 pF (assumed condition)
f_o	=	$(0.5) \times (1) \times (33.3\text{ MHz})$ = 16.7 MHz (calculated, see equation 4 in the introduction to Section 4)

Solution

Quiescent Power

$$\begin{aligned} P_q &= V_{CC} \times [I_{CCI} + N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] \\ &= 5\text{ V} \times [5.8\text{ mA} + (9 \times 1\text{ mA} \times 1)] \\ &= 74\text{ mW} \end{aligned} \quad (1)$$

Dynamic Power

$$\begin{aligned} P_d &= V_{CC} \times [I_{CCf} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] + \Sigma(C_L \times V_{CC}^2 \times f_o) \\ &= 5\text{ V} \times [65\text{ mA} + (9 \times 1\text{ mA} \times 1)] + [9 \times 30\text{ pF} \times (5\text{ V})^2 \times 16.7\text{ MHz}] \\ &= 482.7\text{ mW} \end{aligned} \quad (2)$$

Total Power

$$\begin{aligned} P_T &= (P_d \times DC_d) + [P_q \times (1\text{-}DC_d)] \\ &= (482.7\text{ mW} \times 1/3) + (74\text{ mW} \times 2/3) \\ &= 210.2\text{ mW} \end{aligned} \quad (3)$$

Therefore, the total power is approximately 210 mW.

Power Characteristics

The SN74ACT7807 is available in the 64-pin TQFP and 44-pin PLCC packages. The maximum power-dissipation capabilities of these packages for varying ambient temperatures and air flows can be found in Section 5 of this handbook. At an ambient temperature of 70°C with no air flow, the maximum power that each of these packages can dissipate to free air is 1121 mW and 1244 mW, respectively. The total power dissipation of the SN74ACT7807, under the rather severe conditions of nine inputs (or nine outputs) switching simultaneously, falls well within the thermal budget of either of these packages.

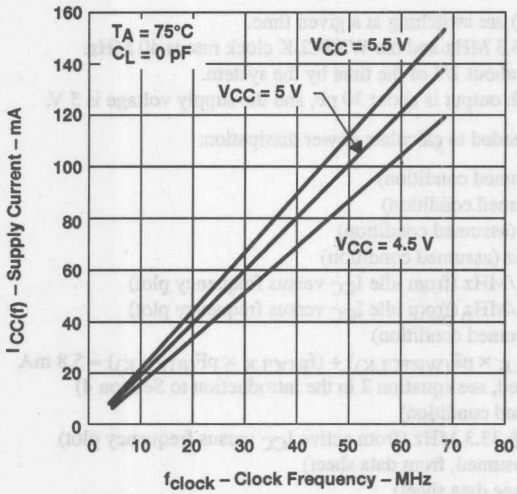


Figure 1. SN74ACT7807 Supply Current Versus Frequency

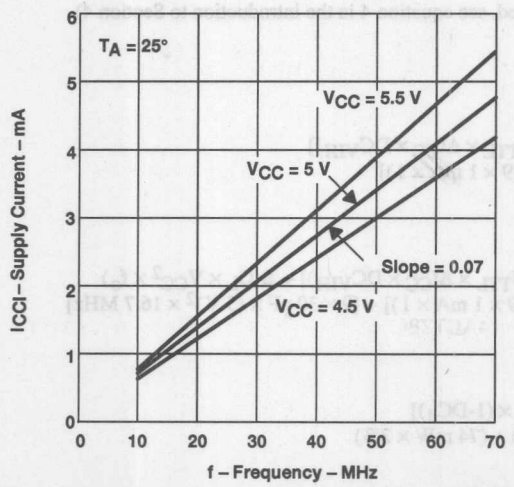


Figure 2. SN74ACT7807 Idle Current With WRTCLK Switching, Other Inputs at 0 or V_{CC} – 0.2 V and Outputs Disconnected

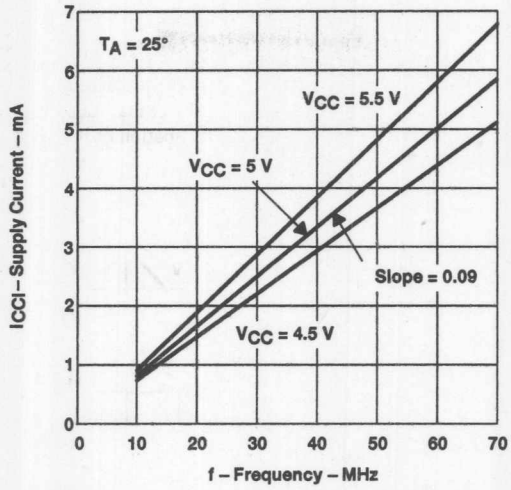


Figure 3. SN74ACT7807 Idle Current With RDCLK Switching, Other Inputs at 0 or V_{CC} – 0.2 V and Outputs Disconnected

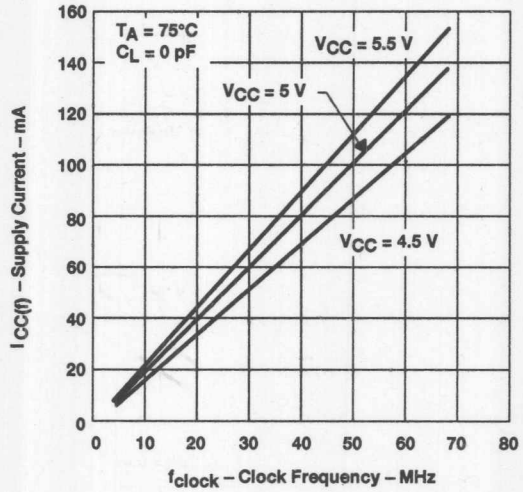
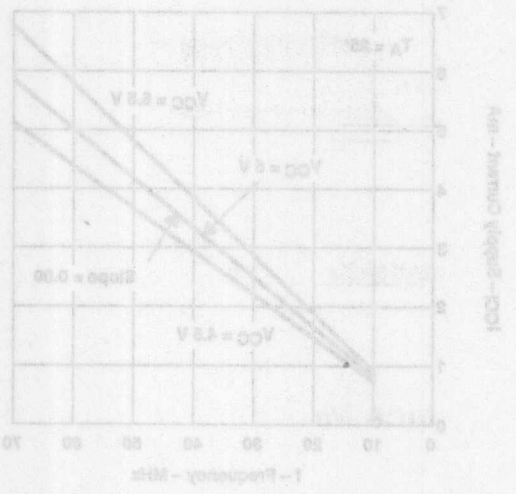
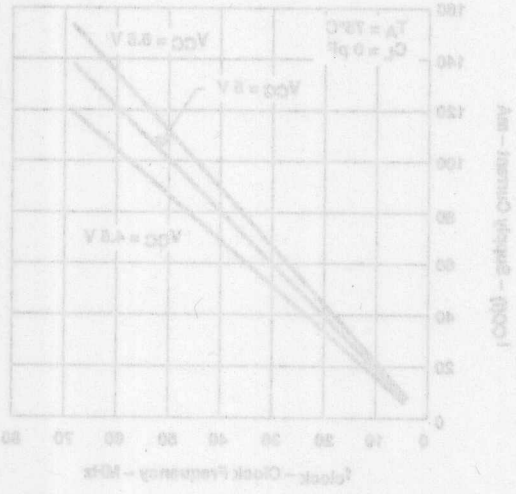


Figure 4. SN74ACT7808 Supply Current Versus Frequency





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5 Mechanical and Thermal Information

Comparison Summary of Advanced Packaging Derating Curves (in Still Air)

Introduction

This section of the FIFO Designer's Handbook contains mechanical and thermal information and data relating to the packages used for Texas Instruments (TI) FIFOs. A series of application reports and papers that address such issues as package thermal resistance, package moisture sensitivity, fine-pitch packaging manufacturability, and measurement procedures of thermal resistance are included in this section. One of these papers, *More Power in Less Space: A Thermal-Enhancement Solution for Thin Packages*, was published in *TI Technical Journal, Volume 11, Number 4 (July-August 1994)*. The paper discusses the design and development of the thermally enhanced thin quad flat package (TQFP TEP) that is capable of dissipating 2.4 watts of power in a 256-mm^2 board area. The thermally enhanced, fine-pitch package is the result of the efforts of a cross-functional team at TI that included resources from package design, chip design, package assembly, reliability, and device testing.

Following the application reports is the mechanical and thermal data for each FIFO package. The mechanical data consists of outline drawings of each package annotated with critical dimensions. Accompanying each package drawing is the associated thermal data. This data consists of measured thermal resistances and derating curves of maximum power dissipation versus ambient temperature for varying air flows.

Figure 1 is a summary plot of the still-air derating curves for the advanced FIFO packaging options. The 120-pin TQFP TEP and the 132-pin PQFP packages are nearly equivalently capable of dissipating more power for a given ambient temperature than any of the other packages considered.

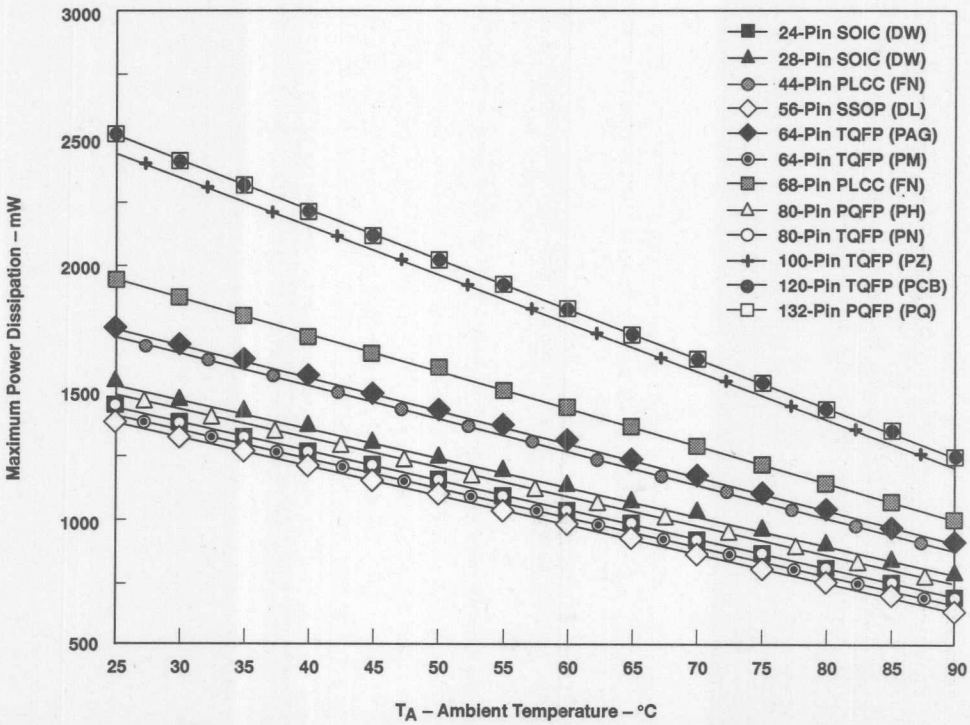


Figure 1. Comparison Summary of Advanced Packaging Derating Curves (in still air)

Figure 1. Comparison Summary of Advanced Packaging Derating Curves (in still air)

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FIFO Surface-Mount Package Information

First-In, First-Out Technology

Tom Jackson and Mary Helmick
Advanced System Logic – Semiconductor Group

TEXAS INSTRUMENTS

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Introduction

Texas Instruments provides seven types of plastic surface-mount packages for CMOS FIFO memory devices. These packages and the data bus width that each package can provide are listed in Table 1.

Table 1. Plastic Surface-Mount FIFO Packages

PACKAGE	NO. OF DATA BITS
44-pin PLCC	9
64-pin TQFP	9
56-pin SSOP	18
68-pin PLCC	18
80-pin TQFP	18
80-pin QFP	18
120-pin TQFP	32 or 36

SSOP = shrink small-outline package
PLCC = plastic leaded chip carrier
TQFP = thin quad flat package
QFP = quad flat package

This application report discusses several topics concerning the FIFO packages listed in Table 1:

- The thermal resistance, $R_{\Theta JA}$, and the chip junction temperature of the device
- The need for dry packing to maintain safe moisture levels inside the package
- The three methods used by Texas Instruments for shipping FIFOs to customers
- The package dimensions, including two-dimensional drawings that show areas, heights, and lead pitches
- The area comparison of surface-mount packages used for commercial FIFO memories
- The test sockets available for surface-mount FIFO packages

Thermal Resistance

Thermal resistance is defined as the ability of a package to dissipate heat generated by an electronic device and is characterized by $R_{\Theta JA}$. $R_{\Theta JA}$ is the thermal resistance from the integrated circuit chip junction to the free air (ambient). Units for this parameter are in degrees Celsius per watt. Table 2 lists $R_{\Theta JA}$ for SSOP, PLCC, TQFP, and QFP packages under five different air-flow environments: 0, 100, 200, 250, and 500 linear feet/minute. The chip junction temperature (T_J) can be determined using equation 1.

$$T_J = R_{\Theta JA} \times P_T + T_A \quad (1)$$

Where:

T_J = chip junction temperature (°C)
$R_{\Theta JA}$ = thermal resistance, junction to free-air (°C/watt)
P_T = total power dissipation of the device (watts)
T_A = free-air (ambient) temperature in the particular environment in which the device is operating (°C)

Table 2. Thermal Resistance, $R_{\Theta JA}$, for FIFO Packages

PACKAGE	LEAD FRAME	$R_{\Theta JA}$ (°C/W)				
		0 LFPM	100 LFPM	200 LFPM	250 LFPM	500 LFPM
56-pin SSOP	Copper	94.2	82.2	N/A	70	57.8
44-pin PLCC	Copper	65	N/A	N/A	N/A	N/A
68-pin PLCC	Copper	47.2	43.4	N/A	32.7	27.8
64-pin TQFP	Copper	92.5	87.8	N/A	72.9	57.8
80-pin TQFP	Copper	87.8	79.1	N/A	67.3	54.2
120-pin TQFP†	Copper	49.6	44.3	N/A	38.3	28.6
80-pin QFP	Alloy 42	80	67	61	N/A	N/A

† Heat slug molded inside the package
N/A = not available

The $R_{\Theta JA}$ generally increases with decreasing package size; however, this is not true with the 120-pin SQFP package. A heat slug molded inside the package absorbs a large amount of heat dissipated by the device. As a result, this package provides a relatively low $R_{\Theta JA}$.

Package Moisture Sensitivity

When a plastic surface-mount package is exposed to temperatures typical of furnace reflow, infrared (IR) soldering, or wave soldering (215°C or higher), the moisture absorbed by the package turns to steam and expands rapidly. The stress caused by this expanding moisture results in internal and external cracking of the package that leads to reliability failures. Possible damage includes the delamination of the plastic from the chip surface and lead frame, damaged bonds, cratering beneath the bonds, and external package cracks.

To prevent potential damage, packages that are susceptible to the effects of moisture expansion undergo a process called dry pack. This dry pack process helps to reduce moisture levels inside the package. The process consists of a 24-hour bake at 125°C followed by sealing of the packages in moisture-barrier bags with desiccant to prevent reabsorption of moisture during the shipping and storage processes. These moisture-barrier bags allow a shelf storage of 12 months from the date of seal. Once the moisture-barrier bag is opened, the devices in it must be handled by one of the following four methods, listed in order of preference:

- The devices may be mounted within 48 hours in an atmospheric environment of less than 60% relative humidity and less than 30°C.
- The devices may be stored outside the moisture-barrier bag in a dry-atmospheric environment of less than 20% relative humidity until future use.
- The devices may be resealed in the moisture-barrier bag adding new fresh desiccant to the bag. When the bag is opened again, the devices should be used within the 48-hour time limit or resealed again with fresh desiccant.
- The devices may be resealed in the moisture-barrier bag using the original desiccant. This method does not allow the floor life of the devices to be extended. The cumulative exposure time before reflow must not exceed a total of 48 hours.

All plastic surface-mount FIFO devices are tested for moisture sensitivity in accordance with Texas Instruments JESD A112 procedure.

Shipping Methods/Quantities/Dry Pack

Three methods are used by Texas Instruments for shipping FIFOs to customers. These methods are tubes, tape/reel, and trays. The quantities for each of the shipping methods are listed in Table 3. The shipping quantity is defined as the maximum number of packages that can be packed in a single shipping unit (e.g., the maximum number of 56-pin SSOP packages that can be packed in a tube is 20). Whether or not the packages require dry pack before shipping is noted in the dry-pack column.

Table 3. Shipping Methods and Quantities

PACKAGE	SHIPPING METHOD			DRY PACK
	TUBE†	TAPE/REEL†	TRAYS†	
56-pin SSOP	20	500	N/A	No
44-pin PLCC	27	500	N/A	No
68-pin PLCC	18/19‡	250	N/A	Yes
64-pin TQFP	N/A	N/A	160	Yes
80-pin TQFP	N/A	N/A	119	Yes
120-pin TQFP	N/A	N/A	90	Yes
80-pin TQFP	N/A	N/A	50	Yes

† Texas Instruments reserves the right to change any of the shipping quantities at any time without notice.

‡ Eighteen packages can be packed in a single tube when pin is used as a tap or nineteen packages can be packed in a tube when plug is used as a tap.

N/A = not applicable

Package Dimensions and Area Comparison

Figure 1 contains two-dimensional drawings of the seven available surface-mount FIFO packages. For detailed mechanical drawings of these packages, please refer to the mechanical drawing section of the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B.

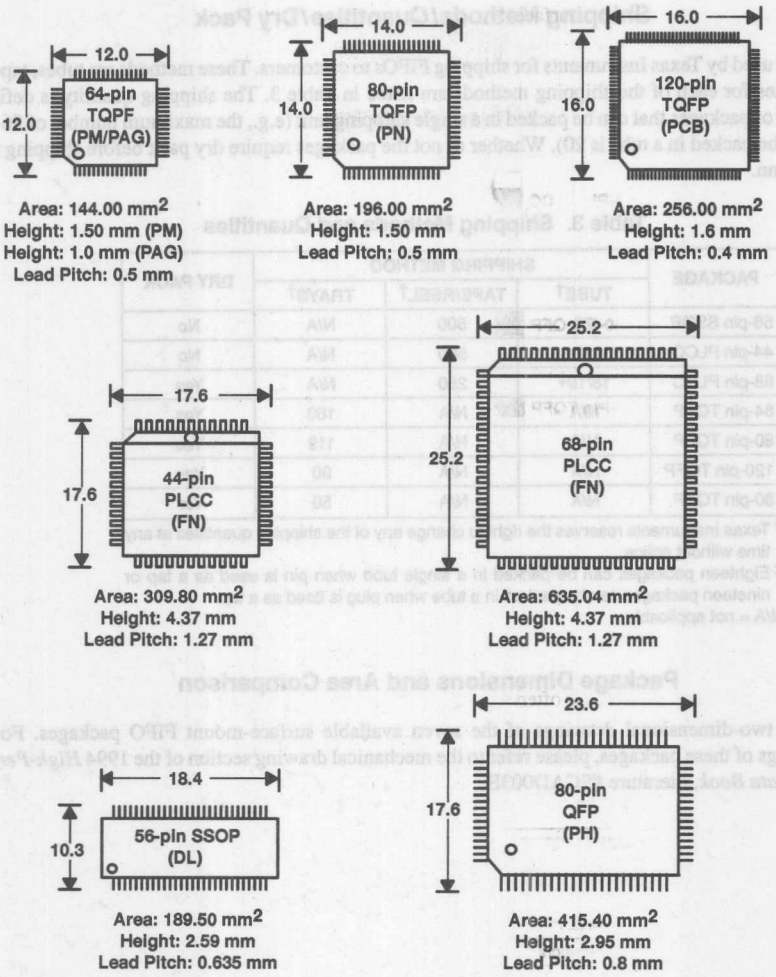


Figure 1. Package Dimensions

Figure 2 shows the area comparison of surface-mount packages for FIFOs from Texas Instruments and other FIFO vendors.

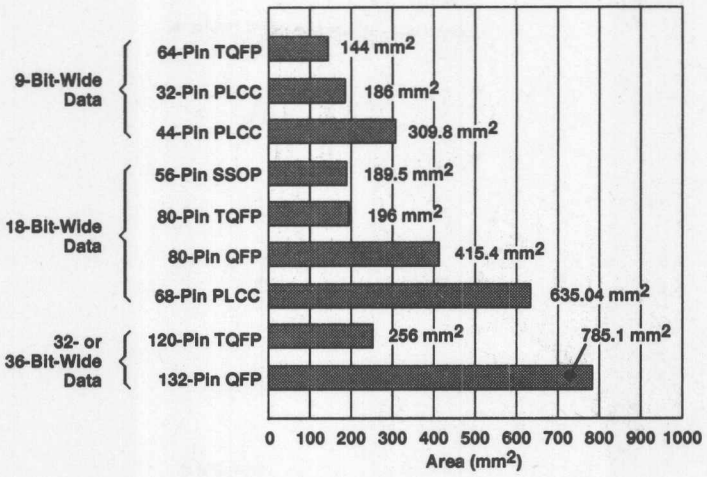


Figure 2. Surface-Mount Package Area Comparison

Test Sockets

For prototype development of a system, it is often an advantage to have sockets for surface-mount products. Test sockets available for use with Texas Instruments FIFO packages are listed in Table 4. Only one manufacturer is listed for each socket type, although other vendors may offer comparable sockets.

Table 4. Test Sockets for FIFO Packages

PACKAGE	MANUFACTURER	NUMBER	DESCRIPTION
56-pin SSOP	Yamaichi	IC51-0562-1387	Solder through hole
44-pin PLCC	NEY	6044	Solder through hole
68-pin PLCC	NEY	6068	Solder through hole
64-pin TQFP	Yamaichi	IC51-0644-807	Solder through hole
80-pin TQFP	Yamaichi	IC51-0804-808	Solder through hole
120-pin TQFP	Yamaichi	IC51–1204–1596	Solder through hole
80-pin QFP	Yamaichi	IC51-0804-394	Solder through hole

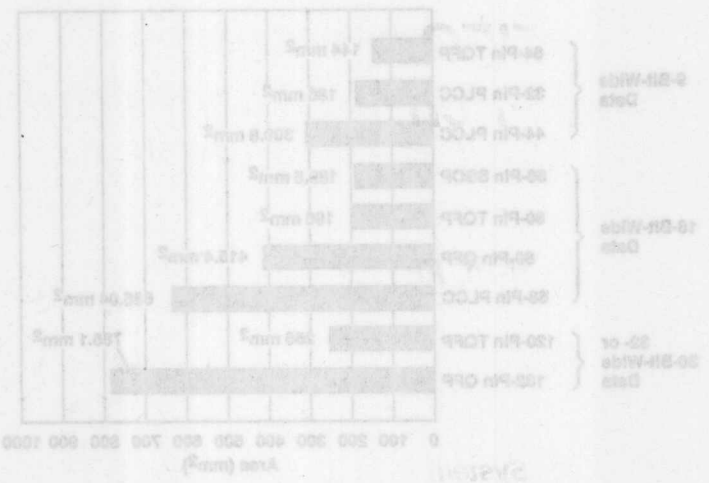


Figure 2. Surface-Mount Package Area Comparison

FIFO Memories: Fine-Pitch Surface-Mount Manufacturability

First-In, First-Out Technology

Tom Jackson
Advanced System Logic – Semiconductor Group



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Introduction

Recent advances in semiconductor processing and packaging have produced highly integrated, fine-pitch devices to satisfy the demand for smaller systems. With the trend towards higher chip complexity occupying less board space, device manufacturers must increase bit density while decreasing package size. To accommodate these requirements, manufacturers have two choices: increase bit density, keeping the number of pins constant while reducing pitch and area, or reduce the package lead pitch, keeping area constant while increasing pin count. Manufacturers of hand-held and laptop computers and data communications and telecommunications equipment require the use of fine-pitch packages to build and maintain a competitive advantage.

Improved Function Density

Texas Instruments (TI) provides five types of fine-pitch plastic surface-mount packages for its FIFO product line (see Table 1). Each of these surface-mount packages has lead-to-lead spacing less than or equal to 0.635 mm (0.025 in.). All of these packages offer designers critical board-space savings that is required for advanced systems. Compared to the commonly used 68-pin plastic leaded chip carrier (PLCC) for 18-bit FIFOs, TI's Widebus™ package, in either the 56-pin shrink small-outline package (SSOP) or the 80-pin thin quad flat package (TQFP), reduces board space by 70%. A 67% saving of board space is available with TI's 36-bit FIFO family in the 120-pin TQFP compared to the 132-pin plastic quad flat package (PQFP).

Table 1. Fine-Pitch Packages

	THIN QUAD FLAT PACKAGE (TQFP)				THIN SHRINK SMALL-OUTLINE PACKAGE (SSOP)
Pin count	64	80	120	132	56
Lead pitch (mm)	0.5	0.5	0.4	0.635	0.635
Footprint (mm)	12 × 12	14 × 14	16 × 16	28 × 28	10.35 × 18.42
Board area (mm^2)	144	196	256	784	190.6
Package suffix	PM	PN	PCB	PQ	DL

Manufacturing

Manufacturers are currently employing high-volume board-assembly techniques using standard lead pitches of 0.5 mm (20 mils) and greater. However, as lead pitch continues to decrease, questions must be asked of both the manufacturer and the supplier:

Are fine-pitch packaging capabilities available?

Does production equipment have sufficient accuracy to produce high-volume, high-quality parts?

Do the manufacturing personnel have experience in high-volume, high-quality production using fine-pitch packaging?

Have the testability issues of fine-pitch packaging been considered?

Standard processing techniques such as those used with surface-mount rigid-lead packages become difficult with fine-pitch packaging. Manufacturing issues may arise from compromises in screen-printing techniques, solder board/lead coplanarity, placement-accuracy requirements of components, and solder deposition methods (e.g., mass reflowing). All of these factors can result in shorts or opens due to poor placement, too much solder, or not enough solder. These issues influence the overall yield and reliability of the product.

Widebus is a trademark of Texas Instruments Incorporated.

Equipment for the placement of fine-pitch packaging must feature a highly accurate positioning system. Placement accuracy for fine-pitch packages must increase as lead pitch decreases. Misaligned packages and boards greatly reduce production yields as well as throughput. Systems that feature state-of-the-art machine vision, align and inspect leads, and calculate registration with an extremely high degree of accuracy and repeatability, ensure high production yields. There must also be careful control over the Z-axis pressure when placing these fine-pitch packages to protect the lead coplanarity. Currently, there are systems available with accurate placement as fine as 0.1-mm pitch.

One of the most critical issues facing the manufacturer is the reliability of the footprint design. Constraints include the length and width of the footprint and the amount of solder paste used to produce a good joint. If too much solder is used, the footprint can bridge, causing a short (see Table 2). The minute dimensions associated with fine-pitch packages require that the footprint be drawn to the highest level of accuracy in order to ensure consistent reliability. Board assemblers must be able to match the footprint with the same level of accuracy and repeatability.

Table 2. Defect Causes and Effects

DEFECT	CONTROL
Solder bridging	Control the solder-paste quantity
Open circuits	Control solder-paste thickness and maintain lead coplanarity
Shorts and opens	Control equipment accuracy in the placement of parts

As previously discussed, the key to ensuring high yield is an accurate footprint pattern. Many manufacturers request footprint patterns and dimensions to assist in their board assembly. There are several factors to consider when designing a footprint pattern to ensure reliability:

- Device design – JEDEC or EIAJ Standard
- PWB – foil thickness, number of layers, supplier's capabilities
- Solder paste – type, solder mesh
- Printer – manufacturer, standoff control, squeegee pressure
- Print mask – type (stencil/mesh), tension, bias
- Reflow process – preheat, temperature, dwell, etc.

The key dimensions for designing an accurate footprint layout is shown in Figure 1.

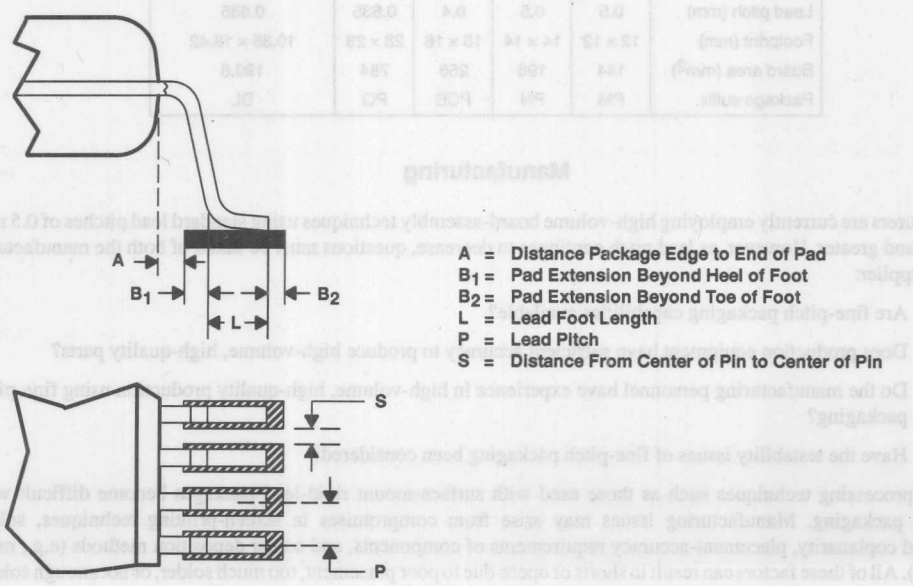


Figure 1. Footprint Diagram

Palladium-Plated Lead Frames

Another area for manufacturers to investigate is metallization, or bonding of the leads to the circuit board with solder. There are several widely used localized reflow techniques including hand soldering, hot bar, focused infrared (IR), and laser. With each technique, heat is applied to the leads until the solder melts. When the heat source is removed, the solder cools forming the joint. Each manufacturer must make the choice between precision point-to-point systems (one chip at a time) and the speed of gang bonding (multiple chip bonding). Another area of metallization to consider is preplating of the leads by the device manufacturer. TI has begun to implement palladium (Pd) lead plating on many fine-pitch packages. These efforts began with joint testing of palladium-plated leads with several large computer and telecom customers in 1987. Since then, TI has begun high-volume manufacturing with over five billion palladium-plated devices in the field.

Palladium preplating is essentially a nickel- (Ni) plated lead frame that has a minimum of 3 micro inches (0.076 micron) of Pd. The Pd finish protects the Ni from oxidation and eliminates the need for silver spotting. Silver (Ag) spots are used to attach the fine wires from the die to the lead frames. However, the silver can migrate over time to form extraneous electrical contacts that greatly impact reliability. Many problems associated with fine-pitch manufacturing can be eliminated with palladium preplating:

- Reduces excess solder
- Excellent Pd wetting characteristics
- Reduced handling
- Improved package integrity
- Reduced mechanical damage
- Tarnish resistant
- Compatible with existing assembly processes
- Excellent adhesion to mold compounds

Table 3 shows the results of a solder-joint strength test comparing Pd solder joints to traditional solder joints. The results demonstrate an equal performance between the two techniques. Palladium preplating also exhibits adhesion to most mold compounds, which reduces moisture ingress and plastic-to-lead-frame delimitation.

Table 3. Results of Soldered Joint Strength

SAMPLE	HOURS OF HEAT AGING			
	0 HR	8 HR	16 HR	24 HR
3 microinches Pd	5.17 lbf	5.95 lbf	5.85 lbf	4.71 lbf
Solder dip	5.07 lbf	4.51 lbf	5.55 lbf	5.50 lbf

In many cases, the cause for shorts and opens can be attributed to lead coplanarity, or the extent to which all leads lie in a single plane. This holds especially true for fine-pitch packaging due to the smaller geometries and delicate leads. Traditional solder-dipped leads tend to have more pin-to-pin alignment problems than the Pd-plated leads. The Pd-preplated leads have a more conformal and uniform coating than those that are solder dipped since the plating is performed prior to the packaging process (see Figure 4). An increase in coplanarity improves overall circuit reliability. The excellent wetting characteristics of Pd improve the wicking effects of solder and form a better solder joint/fillet. The thin Pd coating and minimal handling reduce the chance of coplanarity problems (i.e., shorts and opens) and also produce uniform solder joints with a minimum amount of solder. Table 4 lists TI's fine-pitch packages that implement Pd plating.

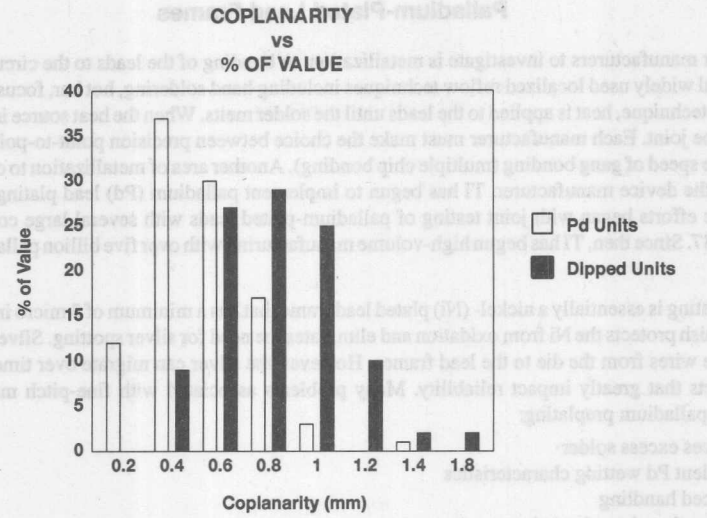


Figure 2. Coplanarity Results

Table 4. Lead-Frame Platings by Package Type

PACKAGE	SUFFIX	LEAD FRAME
132-pin PQFP	PQ	Palladium
120-pin TQFP	PCB	Palladium
80-pin TQFP	PN	Solder
64-pin TQFP	PM	Solder
56-pin SSOP	DL	Palladium

Testability

Another issue introduced by the onset of fine-pitch surface-mount packages involves testing circuit boards. With denser printed-circuit boards heavily populated with fine-pitch surface-mount packages, the issues involved with functional testing should be addressed. One of the most cost-effective solutions is the implementation of boundary-scan methodology defined by the joint test action group (JTAG) and adopted by the IEEE 1149.1 committee. JTAG devices incorporate on-chip test points called boundary-scan cells and utilize a serial-scan protocol through the device. Devices with JTAG can be designed into the datapath and provide the controllability and observability needed to troubleshoot manufacturing defects.

Design/Preproduction Considerations

For designers who wish to implement fine-pitch packaging, TI provides an easy alternative for the development of prototypes and breadboarding. TI has worked with several test-socket manufacturers who provide accurate and easy-to-use through-hole test sockets for all of their surface-mount packaging. In addition to test sockets, TI also offers mechanical packages. These are packages that include lead frames without the silicon and meet all mechanical specifications. Mechanical packages provide an inexpensive means for manufacturing capability studies, machine setup, personnel training, and process-development work (see Table 5).

Table 5. Available Fine-Pitch Test Sockets and Mechanical Packages

SOCKET TYPE	MANUFACTURER	PART NUMBER	DESCRIPTION
64-pin TQFP	Yamaichi	IC51-0644-807	Through hole
56-pin SSOP	Yamaichi	IC51-0562-1514	Through hole
80-pin TQFP	Yamaichi	IC51-0804-808	Through hole
120-pin TQFP	Yamaichi	IC51-1204-1596	Through hole
132-pin PQFP	Yamaichi	IC51-828-KS12338	Through hole

PACKAGE	TI PART NUMBER
64-pin TQFP	SN700870PM
56-pin SSOP	SN250011DLR
80-pin TQFP	SN700871PN
120-pin TQFP	SN700782PCB

Conclusion

Designs that incorporate fine-pitch packages have the advantage of critical board-space reduction. As designers continue to implement higher levels of integration, board space remains at a premium. With the implementation of concurrent engineering practices from design to test to manufacturing, many packaging difficulties can be overcome. Fine-pitch packaging is the designers' easiest option to reduce critical board space without the loss of higher chip integration.

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Package Thermal Considerations

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Abstract

To meet current and future system requirements of increasing speed and decreasing size, integrated circuit manufacturers are pushing the edge on existing packaging technology. A component's performance is determined by process technology and the thermal limitations of its package. As a leader in package technology, Texas Instruments (TI) has introduced a number of fine-pitch packages and is acutely aware of the thermal considerations that must be examined by systems designers. This paper is intended to create awareness and understanding of thermal issues and to explore factors that influence thermal performance.

Introduction

Thermal awareness became an industry concern when surface-mount (SMT) packages began replacing through-hole (DIP) packages in PCB designs. Circuits operating at the same power enclosed in a smaller package meant higher power. To add to the issue, systems required increased throughput, which resulted in higher frequencies, increasing the power density even further. Not only are these same concerns haunting designers today, they are progressively getting more severe.

Figure 1 shows part of the reason for increased attention to thermal issues. As a baseline for comparison, the 24-pin small-outline integrated circuit (SOIC) is shown along with several fine-pitch packages supplied by TI, including the 24-pin SSOP (shrink small outline), 48-pin SSOP, and the 100-pin TQFP (thin quad flat pack). The 24-pin SSOP (8, 9, and 10 bits) allows for the same circuit functionality of the 24-pin SOIC to be packaged in less than half the area, while the 48-pin SSOP (16, 18, and 20 bits) occupies just slightly more area but has twice the functionality of the 24-pin SOIC. This same phenomena is expanded even further with the 100-pin TQFP (32 and 36 bits), which is the functional equivalent of four 24-pin or two 48-pin devices, with additional board savings over that of the SSOP packages. As the trend in packaging technology continues toward smaller packages, attention must be focused on the thermal issues that are created.

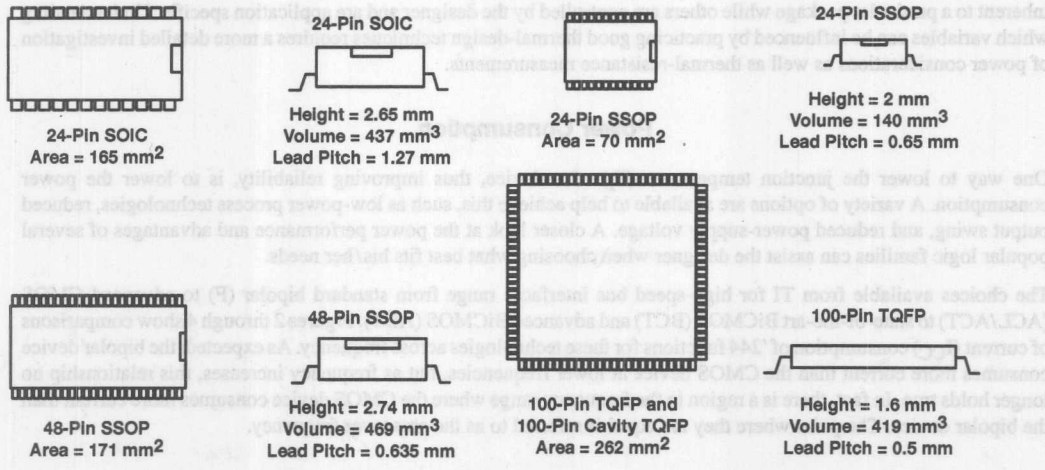


Figure 1. Advanced Packages

Reliability

The overriding effect of increased power densities in integrated circuits is a decrease in overall system reliability. A direct relationship exists between junction temperature and reliability.

Table 1 provides an example of a device with an initial junction temperature of 150°C and the calculated failure-rate decrease as the in-use junction temperature is lowered. The data in Table 1 indicates that lower junction temperature results in increased system reliability.

Table 1

TEMPERATURE °C	% FR†
150	96
140	80
130	46
120	11
110	1
100	0.02

† Failure rate at 100,000 hours

A better understanding of the factors that contribute to junction temperature (T_J) provides a system designer with more flexibility when attempting to solve thermal issues. Device junction temperature is determined by equation 1:

$$T_J = T_A + [\Theta_{JA} \times P_T] \quad (1)$$

Where:

T_J = junction (die) temperature (°C)
T_A = ambient temperature (°C)
Θ_{JA} = thermal resistance of the package from the junction to the ambient (°C/W)
P_T = total power of the device (W)

Junction temperature can be altered by lower chip power consumption, longer trace length, heat sinks, forced air flow, package mold compound, lead-frame size and material, surface area, and die size. Some of these are mechanically inherent to a particular package while others are controlled by the designer and are application specific. Understanding which variables can be influenced by practicing good thermal-design techniques requires a more detailed investigation of power considerations as well as thermal-resistance measurements.

Power Consumption

One way to lower the junction temperature (T_J) of a device, thus improving reliability, is to lower the power consumption. A variety of options are available to help achieve this, such as low-power process technologies, reduced output swing, and reduced power-supply voltage. A closer look at the power performance and advantages of several popular logic families can assist the designer when choosing what best fits his/her needs.

The choices available from TI for high-speed bus interfaces range from standard bipolar (F) to advanced CMOS (ACL/ACT) to state-of-the-art BiCMOS (BCT) and advanced BiCMOS (ABT). Figures 2 through 4 show comparisons of current (I_{CC}) consumption of '244 functions for these technologies across frequency. As expected, the bipolar device consumes more current than the CMOS device at lower frequencies, but as frequency increases, this relationship no longer holds true. In fact, there is a region in the frequency range where the CMOS device consumes more current than the bipolar device. The point where they are equal is referred to as the crossover frequency.

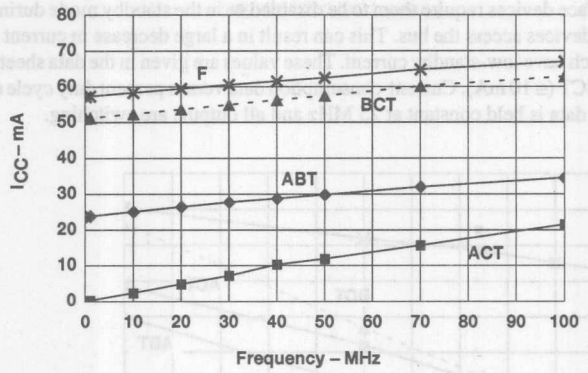


Figure 2. I_{CC} Versus Frequency (One Switching, Unused Outputs Low)

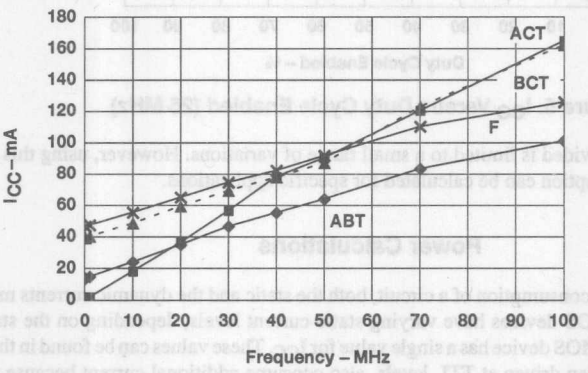


Figure 3. I_{CC} Versus Frequency (All Outputs Switching)

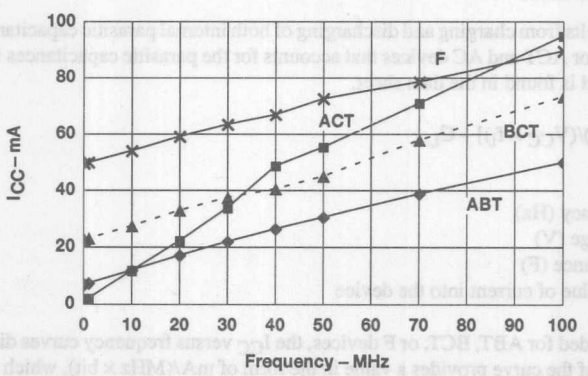


Figure 4. I_{CC} Versus Frequency (All Switching, 50% Duty Cycle Enabled)

Typical applications for bus-interface devices require them to be disabled or in the standby mode during certain periods of time, for instance, while other devices access the bus. This can result in a large decrease in current consumption for ABT, BCT, and ACT devices, which have low-standby current. These values are given in the data sheets as I_{CC} for ACT and I_{CCZ} for ABT (250 µA) and BCT (≅ 10 mA). Current-consumption data versus percent duty cycle enabled is shown in Figure 5. The frequency of the data is held constant at 25 MHz and all outputs are switching.

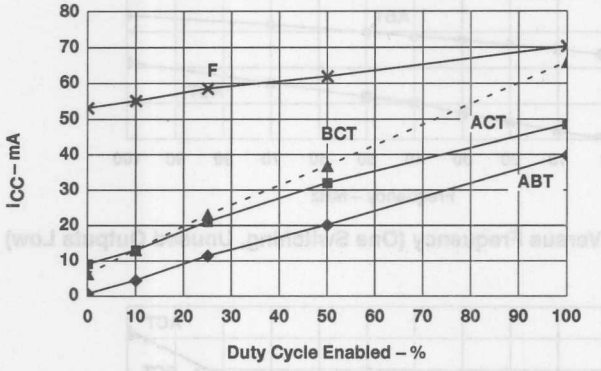


Figure 5. I_{CC} Versus Duty Cycle Enabled (25 MHz)

The power-consumption data provided is limited to a small range of variations. However, using this data, along with standard formulas, power consumption can be calculated for specific applications.

Power Calculations

When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account. Both bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output (I_{CCL}, I_{CCH}, or I_{CCZ}), while a CMOS device has a single value for I_{CC}. These values can be found in the individual data sheets. ACT and ABT inputs, when driven at TTL levels, also consume additional current because they may not be driven all the way to V_{CC} or GND; therefore, the input transistors are not completely turned off. This value is known as ΔI_{CC} and is provided in the data sheet.

Dynamic power consumption results from charging and discharging of both internal parasitic capacitances and external load capacitance. The parameter for ACT and AC devices that accounts for the parasitic capacitances is known as C_{pd}. It is obtained using equation 2 and is found in the data sheet.

$$C_{pd} = [I_{CC}\ (\text{dynamic})/(V_{CC} \times f_i)] - C_L \qquad (2)$$

Where:

f_i = input frequency (Hz)
V_{CC} = supply voltage (V)
C_L = load capacitance (F)
I_{CC} = measured value of current into the device

Although a C_{pd} value is not provided for ABT, BCT, or F devices, the I_{CC} versus frequency curves display essentially the same information. The slope of the curve provides a value in the form of mA/(MHz × bit), which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device without the load current.

Equations 3 through 7 can be used to calculate total power for CMOS, bipolar, and BiCMOS devices:

$$P_T = P_{S(\text{static})} + P_{D(\text{dynamic})} \qquad (3)$$

CMOS

AC (CMOS-level inputs)

$$P_S = V_{CC} \times I_{CC}$$
$$P_D = [(C_{pd} + C_L) \times V_{CC}^2 \times f_1] N_{sw} \quad (4)$$

ACT (TTL-level inputs)

$$P_S = V_{CC} [I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)]$$
$$P_D = [(C_{pd} + C_L) \times V_{CC}^2 \times f_1] N_{sw} \quad (5)$$

BiCMOS/Bipolar

$$P_S = V_{CC} [DC_{en}(N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T) + (1-DC_{en})Iccz] + (N_{TTL} \times \Delta I_{CC} \times DC_d) \quad (6)$$

Note: $\Delta I_{CC} = 0$ for bipolar devices

$$P_D = [DC_{en} \times N_{sw} \times V_{CC} \times f_1 \times (V_{OH} - V_{OL}) \times C_L] + [DC_{en} \times N_{sw} \times V_{CC}\, f_2 \times (mA/MHz \times bit)] \times 10^{-3} \quad (7)$$

Where:

V_{CC}	=	Supply voltage (V)
I_{CC}	=	Power-supply current (A) (from the data sheet)
I_{CCL}	=	Power-supply current (A) when outputs are in low state (from the data sheet)
I_{CCH}	=	Power-supply current (A) when outputs are in high state (from the data sheet)
I_{CCZ}	=	Power-supply current (A) when outputs are in high-impedance state (from the data sheet)
ΔI_{CC}	=	Power-supply current (A) when inputs are at a TTL level (from the data sheet)
DC_{en}	=	% duty cycle enabled (50% = 0.5)
DC_d	=	% duty cycle of the data (50% = 0.5)
N_H	=	Number of outputs in high state
N_L	=	Number of outputs in low state
N_{sw}	=	Total number of outputs switching
N_T	=	Total number of outputs
f_1	=	Operating frequency (Hz)
f_2	=	Operating frequency (MHz)
V_{OH}	=	Output voltage (V) in high state
V_{OL}	=	Output voltage (V) in low state
C_L	=	External load capacitance (F)
mA/(MHz × bit)	=	Slope of the I_{CC} versus frequency curve

Thermal-Resistance Values

Design trends requiring board size reduction have made way for circuit manufacturers to produce fine-pitch packages that appear to threaten the reliability of systems due to further thermal constraints. As a leader in packaging technology, TI has done considerable research into the validity of traditional thermal measurements and data provided by circuit manufacturers.

Unlike data-sheet parameters, where the industry has adopted a standard load for measurement (50 pf, 500 Ω), the measurement of Θ_{JA} has no standard to which all manufacturers comply. The problem facing the designer wishing to make comparisons of thermal data from several manufacturers is that this could be an apples-to-oranges type comparison. As a result, a software package has been developed at TI to allow designers to obtain thermal data based on their specific application.

The validity and usefulness of the traditional approach to presenting Θ_{JA} values became a pressing issue when TI and another manufacturer measured an identical package and obtained results that varied by 40%. Extensive research led

to the conclusion that the methodology used to measure Θ_{JA} did not cause the discrepancy but the physical aspects such as trace length, trace width, number of devices per board, and proximity of the other devices did.

To demonstrate the extreme impact of trace length alone, Figure 6 shows the Θ_{JA} values for TI's 48-pin SSOP at 0 LFMP and 250 LFMP with varying trace lengths. The 48-pin SSOP is shown in Figure 1 for a side-by-side comparison with the standard 24-pin SOIC, the 24-pin SSOP, and the 100-pin TQFP. The data in Figure 6 clearly shows the need for more complete thermal data, not simply a single data point.

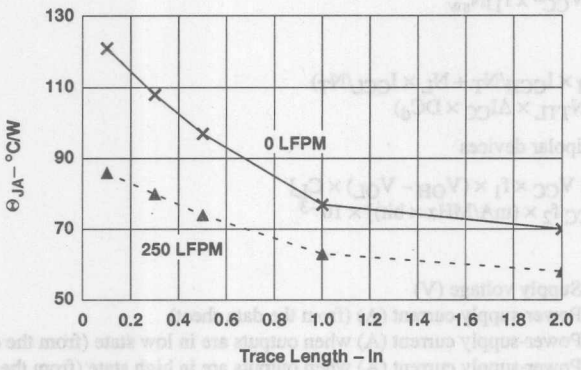


Figure 6. 48-Pin SSOP Θ_{JA} Versus Trace Length

There are other methods to lower the Θ_{JA} of a device. Using heat sinks or blowing air across a device certainly improves the ability to remove heat from its surface. Figure 7 provides Θ_{JA} data for the 48-pin SSOP with trace lengths of 200 mils and 1 inch while varying the amount of air flow. Although many applications tend to limit the amount of air flow, excellent benefits are possible with increased air flow.

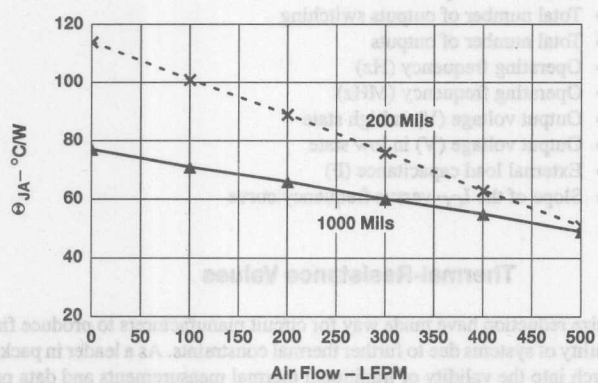
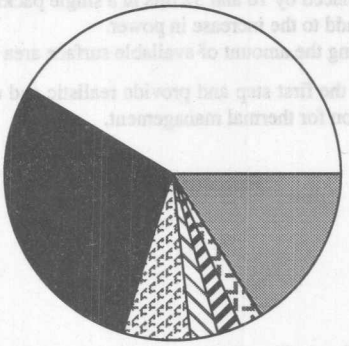


Figure 7. 48-Pin SSOP Θ_{JA} Versus Air Flow

Several variables that have a direct effect on Θ_{JA} values were compared and results are shown in Figure 8. Surprisingly, the major contributing factor is trace length, not air flow. Once again, this validates the need for improvement not necessarily in the test methodology used to calculate Θ_{JA} values, but certainly in the way those values are provided.



VARIABLE	RANGE	% CONTRIBUTION
Trace Length	75 mils – 2000 mils	41.4
Air Flow	0 LFM – 500 LFM	28.8
Board Extension After Trace	0 mils – 400 mils	6.5
Board Extension After Package End	0 mils – 755 mils	2.6
Trace Thickness	1 oz – 2 oz	2.2
Trace Width	3 mils – 15 mils	2.1
Power	0.5 W – 1.5 W	0.1
Total Interactions Between Factors		16.3

Figure 8. 48-/56-Pin SSOP K-Factor Board Modeling

TI provides Θ_{JA} values for a variety of packages (including the SOIC, SSOP, and QSOP) in a user-friendly software package. The program allows designers to specify their conditions, such as trace length, air flow, proximity of other devices, and trace width in order to obtain realistic thermal solutions.

Summary

How a system can avoid being a reliability nightmare in today's world where:

- Eight-bit devices are being replaced by 16 and 32 bits in a single package, increasing the power.
- Higher operating frequencies add to the increase in power.
- Fine-pitch packages are reducing the amount of available surface area to remove heat from a device.

Semiconductor manufacturers must take the first step and provide realistic and useful thermal information that will provide designers key variables to focus on for thermal management.

References

Thermal Software

Contact the factory at (903) 868-7682.

Power Dissipation

Advanced CMOS Logic Designer's Handbook, Texas Instruments Incorporated, 1988, literature number SCAA001B
SSOP Designer's Handbook, Texas Instruments Incorporated, 1991, literature number SCYA001

K-Factor Test-Board Design Impact on Thermal-Impedance Measurements

Larry W. Nye
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Abstract

The rapid advancement in semiconductor-device technology is placing unprecedented demands on device-packaging technology. In an effort to meet system requirements for increased speed in smaller footprints, integrated circuit manufacturers are pushing existing packaging technology to new limits. Product performance is a function of both device and packaging technologies. In many instances, the thermal limitations of the packaging system can severely restrict the performance of the device, thus limiting systems applications. System designers and integrated circuit manufacturers are becoming increasingly more concerned about accurate thermal characterization.

There are several indices typically reported to reflect the thermal performance of a package. Thermal impedances, Θ_{JA} (junction to ambient) and Θ_{JC} (junction to case) are the most frequently used throughout the industry. Although there are several specifications on the administration of these tests and measurements, there is no universally accepted industry-wide standard. This lack of standardization promotes an apples-to-oranges comparison of published data, as well as inaccurate estimation of application performance.

This paper focuses on the impact of the wind-tunnel k-factor test-board design parameters on reported Θ_{JA} results. By employing statistical experimental design techniques and finite element analysis (FEA), equations are derived that can be used to quickly normalize reported Θ_{JA} values under various test-board conditions. These mathematical equations are shown to correlate well with empirical wind-tunnel results. A computer program, THETACAL™, has been developed by Texas Instruments (TI) to assist system designers in understanding and comparing the thermal capabilities of packages sourced from various integrated-circuit manufacturers.

Introduction

The use of statistical design of experiment (DOE) techniques combined with FEA provides the engineering community with valuable tools for forecasting the behavior of a system or process. A natural marriage, the DOE and FEA combination allows the engineer to study a range of boundary conditions for numerous design factors and to analyze the impact and associated response for each factor and interaction within the system. With the use of orthogonal polynomial expansion techniques, experimental results can be effectively transformed into mathematical equations based on the strength of the various factors and associated interactions. These equations are useful for performing what-if analyses on a system or process.

The thermal impedance (k-factor) of a package is defined as the increase in junction temperature above the ambient due to the power dissipated by the device and is measured in degrees Celsius per watt. There are two indices commonly used to describe the thermal characteristics of an integrated-circuit package: Θ_{JA} and Θ_{JC}. Θ_{JC} is the thermal impedance from the integrated-circuit die junction to the package external case and is typically measured in a circulating bath of an inert liquid simulating an infinite heat sink. Θ_{JA} is the most widely used and least understood measurement utilized in package selection for application design criteria. There are actually two Θ_{JA} measurements commonly reported:

Socket mounted and measured in 1 cubic foot of still air

Board mounted and measured in a wind tunnel at various air flows

In case #1, the type of socket and socket manufacturer should be noted when comparing reported values, as they can significantly impact the reported Θ_{JA} values.

The focus of this report and the development of the THETACAL software tools are targeted to address the problems associated with board-mounted Θ_{JA} values reported under wind-tunnel conditions (case #2). As indicated earlier, there are several specifications on the administration of wind-tunnel tests and measurements, but there is no universally accepted standard. Wind-tunnel dimensions and k-factor board construction techniques vary widely from manufacturer to manufacturer and can dramatically impact the reported Θ_{JA} values. Figure 1 shows the differences noted on an identical package measured on two different integrated-circuit manufacturer's k-factor boards in the same wind tunnel.

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In Figure 1, there is roughly a 45°C/W difference (still air) between manufacturers induced by the k-factor board alone. Considering this fact, it is possible for a wide range of reported k-factor values to exist for any given package, depending on the test-board design employed by the manufacturer. Systems designers unaware of these differences can be artificially restricted in packaging selections based only on reported thermal-impedance values.

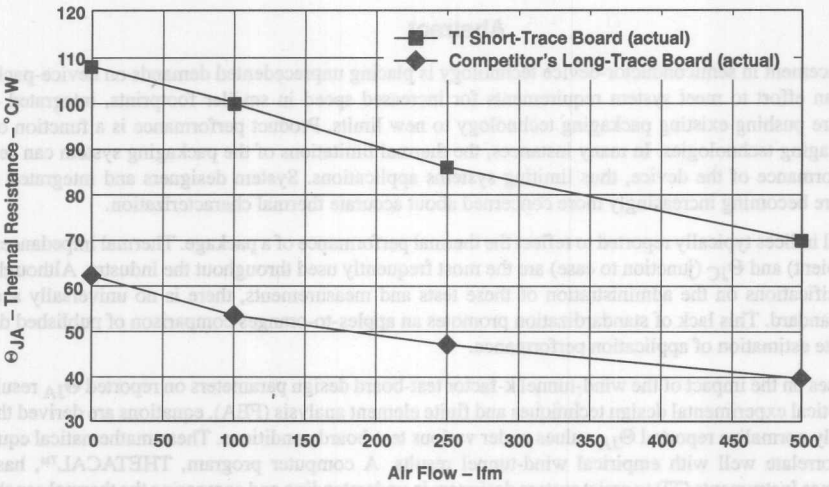


Figure 1. Competitor Versus TI K-Factor Board (52-pin MQFP)

In an effort to provide system designers with an accurate tool for estimating the impact of k-factor test-board designs on reported thermal impedance values (Θ_{JA}), TI has developed the THETACAL software package. By employing statistical experimental design techniques combined with finite element analysis tools, equations can be derived to perform *what-if* analyses varying single or multiple input parameters simultaneously to accurately estimate their impact on the desired response (Θ_{JA}). This tool allows designers to compare the thermal performance of a given package sourced from various manufacturers on an apples-to-apples basis. In addition, the software can be utilized to better understand the influence of the various board-related parameters and their impact on Θ_{JA}.

Modeling Approach

The following four-phase methodology was utilized to develop the THETACAL software package:

1. Design of the experiment using orthogonal arrays
2. Modeling the package using FEA (ABAQUS™) tools
3. Expansion of the matrix results into an orthogonal-polynomial equations
4. Mathematical simulation of the thermal response (Θ_{JA}) for performing what-if analyses

Once the orthogonal-polynomial equations are completed and verified, they are incorporated into the THETACAL software environment. Each package type and pin count are evaluated separately to ensure accuracy in the equations.

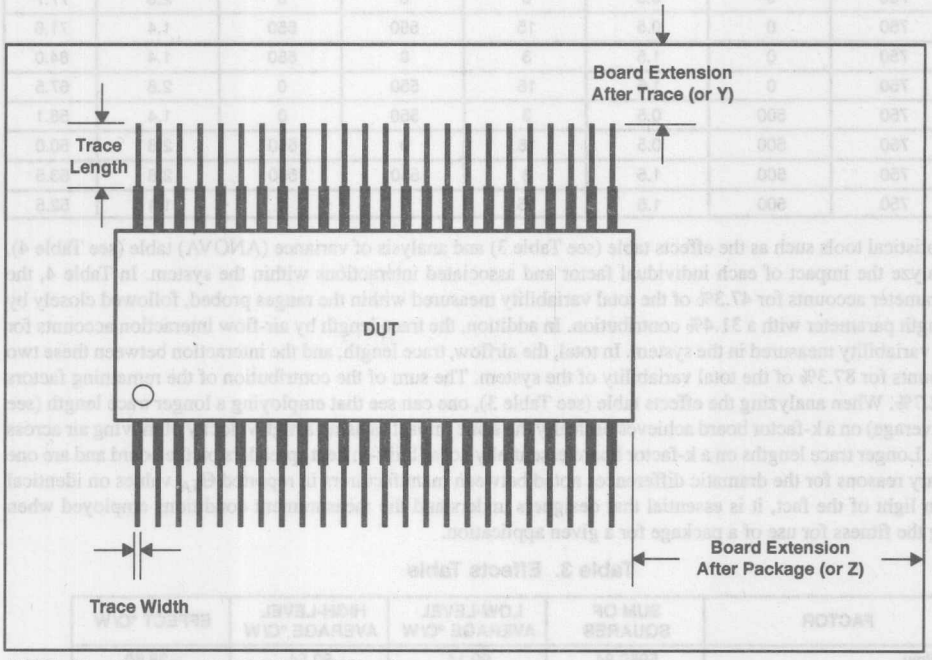
ABAQUS is a trademark of Texas Instruments Incorporated.

Design of the Experiment

Typical k-factor boards are constructed using an FR4 or polyimide-composite substrate. Copper traces of varying dimensions are fabricated upon this substrate for package mounting and to complete the electrical connections required for k-factor testing. The parameters in Table 1 are most typically varied in k-factor board construction (see Figure 2) and are the focus of this study and the THETACAL software development.

Table 1. Evaluation Parameters

	TRACE LENGTH (mils)	AIR FLOW (lfm)	POWER (watts)	TRACE WIDTH (mils)	BOARD Z EXTENSION (mils)	BOARD Y EXTENSION (mils)	TRACE THICKNESS (mils)
Low	50	0	0.5	3	0	0	1.4
High	750	500	1.5	15	550	550	2.8



NOTE: Y and Z are used for PLCC and QFP packages.

Figure 2. Test Board

An L_{16} orthogonal array[1] was selected as the design vehicle used to evaluate the impact of all identified main factors and their expected interactions within the k-factor test-board system. Since the focus of this study is to derive mathematical equations to be utilized for estimation purposes, it is extremely important to properly define the layout of the experiment to capture all sources of variability; i.e., the accuracy of the equation is best when the unresolved variability is minimized. Once the experiment has been properly defined, appropriate models are prepared per the matrix and processed through the finite element analysis thermal solver (ABAQUS). A typical data set, as returned by the FEA software, is shown in the far right column of Table 2. Statistical analysis is done and orthogonal-polynomial equations can be derived from the completed data set.

Table 2. Matrix Definition and Results

RUN	TRACE LENGTH (mils)	AIR FLOW (lfm)	POWER (watts)	TRACE WIDTH (mils)	BOARD Z EXTENSION (mils)	BOARD Y EXTENSION (mils)	TRACE THICKNESS (mils)	MODEL Θ_{JA} (°C/W)
1	50	0	0.5	3	0	0	1.4	151.3
2	50	0	0.5	15	550	550	2.8	100.6
3	50	0	1.5	3	0	550	2.8	119.2
4	50	0	1.5	15	550	0	1.4	121.2
5	50	500	0.5	3	550	0	2.8	66.5
6	50	500	0.5	15	0	550	1.4	68.6
7	50	500	1.5	3	550	550	1.4	61.6
8	50	500	1.5	15	0	0	2.8	75.5
9	750	0	0.5	3	0	0	2.8	77.7
10	750	0	0.5	15	550	550	1.4	71.6
11	750	0	1.5	3	0	550	1.4	84.0
12	750	0	1.5	15	550	0	2.8	67.5
13	750	500	0.5	3	550	0	1.4	56.1
14	750	500	0.5	15	0	550	2.8	50.0
15	750	500	1.5	3	550	550	2.8	53.5
16	750	500	1.5	15	0	0	1.4	52.5

By using statistical tools such as the effects table (see Table 3) and analysis of variance (ANOVA) table (see Table 4), one can analyze the impact of each individual factor and associated interactions within the system. In Table 4, the air-flow parameter accounts for 47.3% of the total variability measured within the ranges probed, followed closely by the trace length parameter with a 31.4% contribution. In addition, the trace length by air-flow interaction accounts for 8.6% of the variability measured in the system. In total, the airflow, trace length, and the interaction between these two factors accounts for 87.3% of the total variability of the system. The sum of the contribution of the remaining factors is a mere 12.7%. When analyzing the effects table (see Table 3), one can see that employing a longer trace length (see high-level average) on a k-factor board achieves basically the same impact as using a high velocity of moving air across the package. Longer trace lengths on a k-factor board essentially act as built-in heat spreaders on the board and are one of the primary reasons for the dramatic differences noted between manufacturers in reported Θ_{JA} values on identical packages. In light of the fact, it is essential that designers understand the measurement conditions employed when determining the fitness for use of a package for a given application.

Table 3. Effects Table

FACTOR	SUM OF SQUARES	LOW-LEVEL AVERAGE °C/W	HIGH-LEVEL AVERAGE °C/W	EFFECT °C/W
Air flow	5959.84	99.14	60.54	−38.60
Trace length	3956.41	95.56	64.11	−31.45
Trace length by air flow	1079.12	88.05	71.63	−16.42
Board Z ext.	402.00	84.85	74.83	−10.02
Trace length by board Y ext.	304.50	84.20	75.48	−8.72
Trace width	243.36	83.74	75.94	−7.80
Board Y ext.	219.04	83.54	76.14	−7.40
Trace thickness	198.81	83.36	76.31	−7.05
Trace length by board Z ext.	151.29	82.91	76.76	−6.15
Trace length by trace thickness	40.32	81.43	78.25	−3.18
Trace width by trace thickness	15.60	80.83	78.85	−1.98
Trace length by power	8.41	80.56	79.11	−1.45
Air flow by power	7.84	80.54	79.14	−1.40

Table 4. Analysis of Variance (ANOVA) (50-mil thru 750-mil trace lengths)

FACTOR	DOF	SUM OF SQUARES	MEAN SQUARES	F-TEST	% CONTRIBUTION	STATISTICAL SIGNIFICANCE
Air flow	1	5959.84	5959.84	2995	47.3	99%
Trace length	1	3956.41	3956.41	1988	31.4	99%
Trace length by airflow	1	1079.12	1079.12	542	8.6	99%
Board Z ext.	1	402.00	402.00	202	3.2	99%
Trace length by board Y ext.	1	304.50	304.50	153	2.4	99%
Trace width	1	243.36	243.36	122	1.9	99%
Board Y ext.	1	219.04	219.04	110	1.7	99%
Trace thickness	1	198.81	198.81	100	1.6	99%
Trace length by board Z ext.	1	151.29	151.29	76	1.2	95%
Trace length by trace thickness	1	40.32	40.32	20	0.3	95%
Trace width by trace thickness	1	15.60	15.60	8	0.1	
Trace length by power	1	8.41	8.41	4	0.1	
Air flow by power	1	7.84	7.84	4		
Error pool:						
Power	1	3.42				
Trace length by trace width	1	0.56				
Residual		0.005				
Total residual	2	3.98	1.99		0.2	
Total	15	12590.54			100	

Orthogonal-Polynomial Expansion

The results of an orthogonal array can be easily expanded into a powerful orthogonal-polynomial equation. Employing statistical principles, it is possible to construct an accurate mathematical model to quickly estimate the thermal response of a package by analyzing the impact of critical design parameters and key interactions. There has long been a need for an effective thermal calculator that can accurately and reliably estimate the thermal condition of a package under various design parameters, i.e., to analyze the impact of various material, dimensional, and air-flow conditions. Orthogonal-polynomial equations provide such a tool. Utilizing this approach, the solving power of the FEA software can be effectively transformed into a mathematical equation or a system of equations for the desired response for performing what-if analyses within the ranges probed. The general equation format for a two-level orthogonal array with interactions follows. Higher-order equations for nonlinear responses, not described in this work, can also be employed using this technique[2].

General Equation Format

$$\hat{\theta}_{JA} = \overline{\theta_{JA}}$$

$$+ b_{1(a)}(a - \bar{a}) \quad \text{[linear terms for factor a]}$$

$$+ b_{1(b)}(b - \bar{b}) \quad \text{[linear terms for factor b]}$$

$$+ b_{11(a-x-b)}(a - \bar{a})(b - \bar{b})\cdots \quad \text{[interaction terms for factor a – x –b]}$$

Where:

$\hat{\theta}_{JA}$ = Predicted matrix response

$\overline{\theta_{JA}}$ = Average matrix response

$b_{1(i)}$ = Coefficient of the linear response for i

$lvl_{(i)}$ = Number of factor levels at indicated setting for factor i

$h_{(i)}$ = Δ setting between factor levels

$b_{11(i)}$ = Coefficient of interaction response for i

a = Factor input variable for what-if analysis

$\overline{a}$ = Average of factor settings

Factor Coefficients

- **Linear coefficient:**

$$b_{1(a)} = \frac{-A_1 + A_2}{r * \lambda s_{(a)} h_{(a)}}$$

Where:

A_i = Sum of factor response at level indicated

r = Number of runs per factor level

λs = (1 for a 2-level factor) (2 for a 3-level factor)

$h_{(a)}$ = Factor Δ setting

- **Interaction coefficient:**

$$b_{11(A-x-B)} = \frac{[(A_1 + B_1) - (A_1 + B_2)] - [(A_2 + B_1) - (A_2 + B_2)]}{r * \lambda s_A h_A * \lambda s_B h_B}$$

Once the equation is derived, the initial test conditions can be plugged into the equation to check for accuracy against the original modeled parameters as shown in Table 5. If the experiment has been properly designed to capture all significant sources of variability, the equation results should closely match the modeled results. If the error term is minimal (see Table 4), as in this case, the equation matches the modeled results exactly. As the error increases, the accuracy of the equation decreases. At this point, the power of the FEA is transformed into a simple mathematical model for this response within the ranges probed for all parameters. It is now possible to vary individual or multiple input parameters (within the ranges studied) for performing what-if analyses. As with any simulation, equation results should be tested against empirical results to ensure proper accuracy. If the desired accuracy is not achieved, the input models should be reevaluated and adjusted as required.

Table 5. Equation Versus Model

RUN	TRACE LENGTH (mils)	AIR FLOW (lfm)	POWER (watts)	TRACE WIDTH (mils)	BOARD Z EXTENSION (mils)	BOARD Y EXTENSION (mils)	TRACE THICKNESS (mils)	MODEL Θ_{JA} (°C/W)	EQUATION Θ_{JA}(°C/W)
1	50	0	0.5	3	0	0	1.4	151.3	151.3
2	50	0	0.5	15	550	550	2.8	100.6	100.6
3	50	0	1.5	3	0	550	2.8	119.2	119.2
4	50	0	1.5	15	550	0	1.4	121.2	121.2
5	50	500	0.5	3	550	0	2.8	66.5	66.5
6	50	500	0.5	15	0	550	1.4	68.6	68.6
7	50	500	1.5	3	550	550	1.4	61.6	61.6
8	50	500	1.5	15	0	0	2.8	75.5	75.5
9	50	0	0.5	3	0	0	2.8	77.7	77.7
10	750	0	0.5	15	550	550	1.4	71.6	71.6
11	750	0	1.5	3	0	550	1.4	84.0	84.0
12	750	0	1.5	15	550	0	2.8	67.5	67.5
13	750	500	0.5	3	550	0	1.4	56.1	56.1
14	750	500	0.5	15	0	550	2.8	50.0	50.0
15	750	500	1.5	3	550	550	2.8	53.5	53.5
16	750	500	1.5	15	0	0	1.4	52.5	52.5

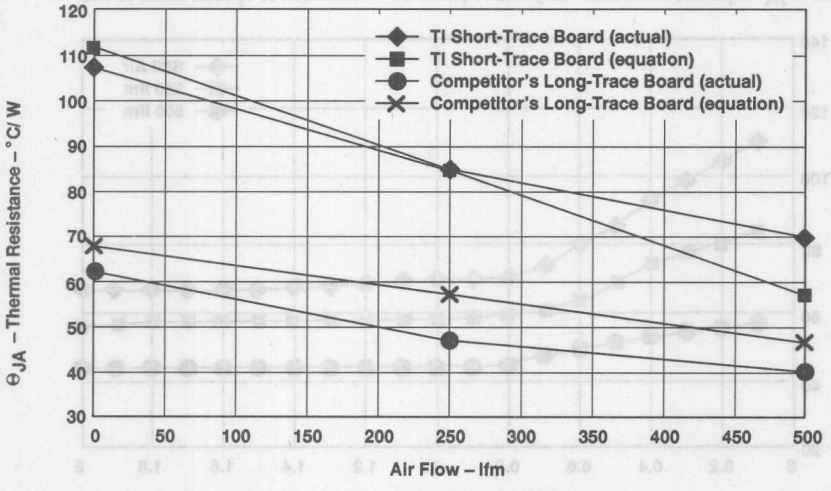


Figure 3. 52-Pin MQFP (actual versus equation)

Verification: Equation Versus Actual Measurements

The air-flow and trace-length parameters were the most dominant influences noted with respect to Θ_{JA}. Wind-tunnel measurements taken on k-factor boards with both short- and long-trace conditions were compared against the orthogonal-polynomial equation. Figure 3 shows that the equation accurately estimates the Θ_{JA} under radically different k-factor board conditions.

Individual FEA-model runs in the orthogonal array used to derive the equation can take several hours of computer processing time, depending on the type of workstation used. In an effort to minimize the modeling time required for each package, 2-level orthogonal arrays were used to minimize the number of runs required to approximate the system. Due to the extremely broad range of trace lengths that can be employed in k-factor test board design (50 mils to 2000 mils), and considering the dramatic influence of the trace-length parameter on Θ_{JA}, two separate matrices are evaluated for each package. The impact on the Θ_{JA} induced by the trace-length parameter is quite dramatic on most packages between 50 mils and 750 mils. From 750 mils to 2000 mils, the impact is less dramatic. In an effort to achieve acceptable equation resolution using linear approximations, two matrices were evaluated for each package. The first matrix focused on the shorter trace lengths and the second matrix focused on the longer traces. In the THETACAL software, this is transparent to the user upon input; however, minor discontinuities may be noted where the equations converge.

The equation(s) can now be utilized to perform what-if analyses on the various input parameters. Figure 4 indicates the impact that the trace length has on Θ_{JA} at various wind-speed conditions.

The knee of the curve at approximately 0.75 inches (750 mils) is the point where the equations from the two matrices converge. The THETACAL software can be used to evaluate any of the parameters considered in the study in a similar fashion. The equations used in the THETACAL software package provide the end users with the power of FEA capabilities (for the Θ_{JA} response) instantaneously and requires no workstation or special skills to use.

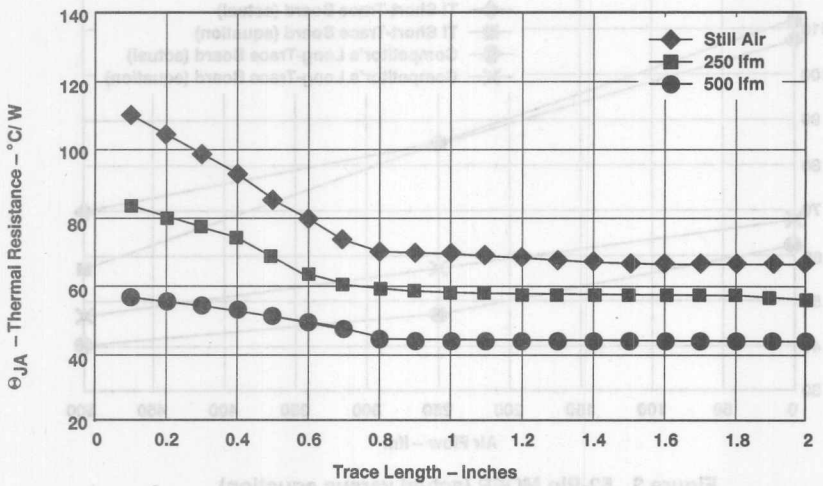


Figure 4. 52-Pin MQFP (trace length effect)

Conclusion

Thermal management of semiconductor packages is becoming increasingly more critical with the move to smaller package geometries and higher power requirements. In order to meet increasingly challenging design goals, systems designers and end users of integrated-circuit packages must be able to make informed decisions on the fitness for use of a package based on thermal considerations. K-factor test-board construction can dramatically impact reported Θ_{JA} results and promote restrictions in package selection and system-performance specifications. The THETACAL software package provides users with an effective tool to normalize reported Θ_{JA} values and assist in making informed decisions on package selection to reach design goals.

Acknowledgements

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More Power in Less Space: A Thermal Enhancement Solution for Thin Packages

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More Power in Less Space: A Thermal Enhancement Solution for Thin Packages

Abstract: Integrated circuit packaging technology can no longer be treated as a secondary consideration to circuit design. The packaging system is an integral part of the device function, composed of sophisticated materials and complex assembly processes that balances many diverse factors, dramatically impacting the device performance. Often, package design must now be done concurrent with circuit design, understanding the limitations of each on the other.

Recent advances in wafer fabrication technology have forced IC package designers to provide packaging solutions for higher power in smaller spaces. Traditionally, shrinking the size of plastic packages restricts the device performance due to thermal constraints.

Using the equivalent 8- and 16-bit functions as the board space benchmark, a package was needed to accommodate 32- and 36-bit logic devices. The resulting package size presented thermal management problems that had to be addressed with some revolutionary approaches. Additional design goals were the equivalent package reliability to existing packages and the ability to produce the package at an acceptable cost for the target market.

A cross-functional team was structured to include resources from package design, chip design, package assembly, reliability and device testing. Design for Manufacturability concepts were used to meet six sigma process capability on all aspects of the packaging system. The resulting design was a thermally enhanced thin quad flat package (TQFP TEP) that can dissipate 2.4 watts of power in a 256-mm^2 board area, assuming 25°C ambient temperature and 150°C maximum junction temperature.

TRENDS toward higher device functionality in smaller space have driven the development of space-efficient packages. Integrated circuit (IC) devices have evolved from low-pin-count, coarse-pitch, through-hole packages to high-pin count, fine-pitch, surface-mount packages. This evolution has placed new thermal management demands on IC packaging technology.

As plastic packages shrink in area and thickness, thermal impedances increase, limiting the power and frequency at which devices can operate. To take advantage of the increasing capability of IC devices, solutions must be found for smaller packages that can dissipate high power. A traditional option for thermal management is to add external heat sinks to conventional plastic packages, but emerging applications (e.g., laptop and notebook PCs) have placed additional clearance constraints, preventing this approach.

Customer requirements for this package design were: meet existing package reliability levels, 2.4 W power dissipation, footprint smaller than the equivalent function in multiple packages and manufacturable at acceptable cost. A design team was structured to include chip designers, assembly process engineers, package design engineers and key component suppliers to facilitate the development process.

Design Criteria

A new package was required for a family of 32- and 36-bit bus interface logic components. Several constraints were placed on the design of the package: the package must have 100- and 120-pin configurations; the board area must be no larger than that required for the equivalent function in 8- or 16-bit versions; the package must dissipate 2.4 watts without an external heat sink; and the manufacturing cost must be competitive in the marketplace.

Design Approach

Considering the design constraints, two form factors were analyzed; a dual in-line design and a quad design. Device architecture preferred the in-line design, but considering available die bonding and leadframe manufacturing capabilities, an in-line design that met the board space constraint would require a lead pitch of 0.3 mm. Research throughout the marketplace indicated that by 1993, 0.4-mm pitch

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was acceptable, but 0.3-mm pitch was not compatible with current board mount capabilities. The 0.4-mm outer lead pitch quad design was chosen.

Two approaches to thermal enhancement were considered (*Figure 1*) a cavity-type lidded plastic package and an exposed heat slug plastic package. Two heat slug options were evaluated; a heat slug attached to a conventional die pad and direct die attach to a heat slug. All designs were evaluated in chip-up and chip-down configurations.

Thermal models and analytical data showed that both design approaches can dissipate the required power. For each design, the chip-down configuration maximizes the heat transfer from the package, especially with forced convection. In this configuration, the customer has the option to use an external heat sink if the application demands (*Table I*).

The cavity design had addi-

Table I. Modeled Power Dissipation of Various Package Configurations.

Maximum Power Dissipation, Watts — assuming 25°C ambient & 150°C maximum junction temperature			
Package Configuration	**0 ft/min Airflow**	**250 ft/min Airflow**	**500 ft/min Airflow**
Cavity Style Chip Up	2.31	4.24	5.98
Chip Down	2.25	3.77	5.04
Heat Slug Style Chip Up	2.40	4.45	6.35
Chip Down	2.38	4.19	5.81

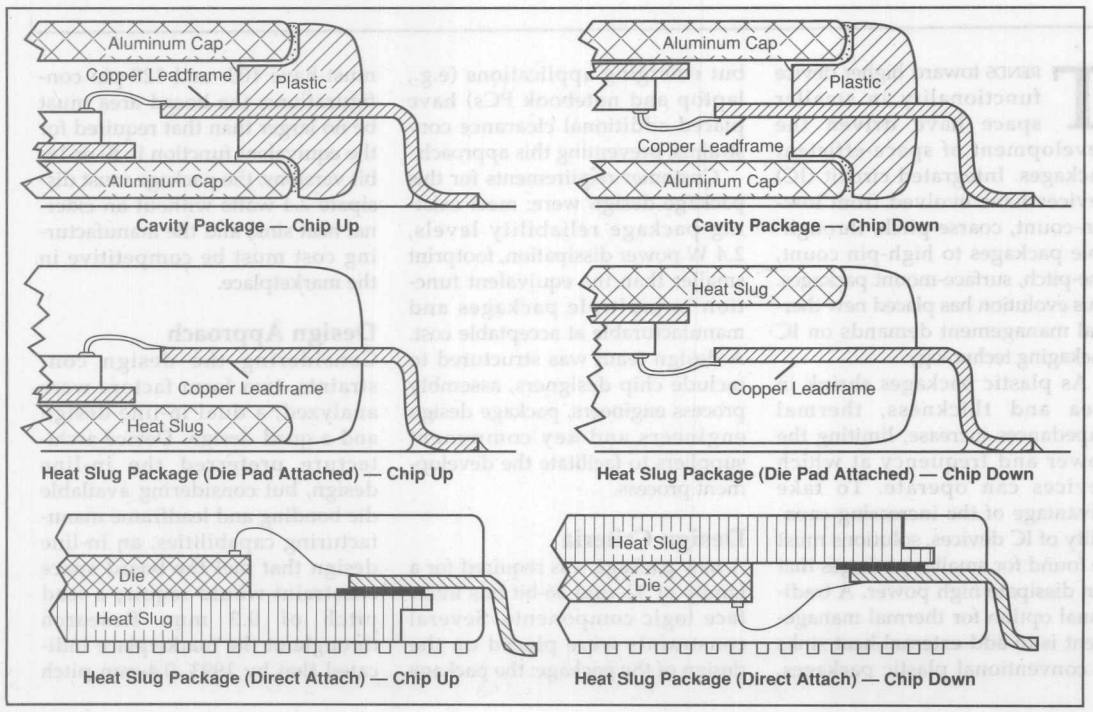


Figure 1. Package Configurations Considered.

tional process complexity and possible reliability problems due to moisture ingress, thermal mismatch and bond wire movement. The heat slug design used conventional processes and equipment. The heat slug design in the chip-down configuration was chosen based on its ability to meet the design criteria, compatibility with existing processes, potential for improved reliability performance and more cost-effective manufacturing flow. The package was designed to meet the emerging JEDEC standard for 1.4-mm thick thin quad flat packages (MO-136) (*Figure 2*).

Material Selection

Thermal constraints drove the use of a copper leadframe and a copper heat slug (*Figure 3*). Based on positive past results with fine-pitch packages, a palladium pre-plated leadframe was selected. The heat slug was directly attached to the leadframe due to the 1.4-mm thickness of the package. This design, as opposed to a slug attached to the die pad or a drop in heat spreader, gives a more direct heat path to the outside of the package and simplifies the assembly process. The heat slug is attached to the leadframe using a two-sided adhesive film. A polyimide film was chosen due to its stability at elevated processing temperatures and its low moisture absorption. The adhesive film also provides electrical isolation between the heat slug and the lead fingers.

The heat slug required a surface treatment to inhibit corrosion since it was exposed to air. A proprietary surface treatment was selected based on its superior adhesion performance with molding compounds. Shear tests were

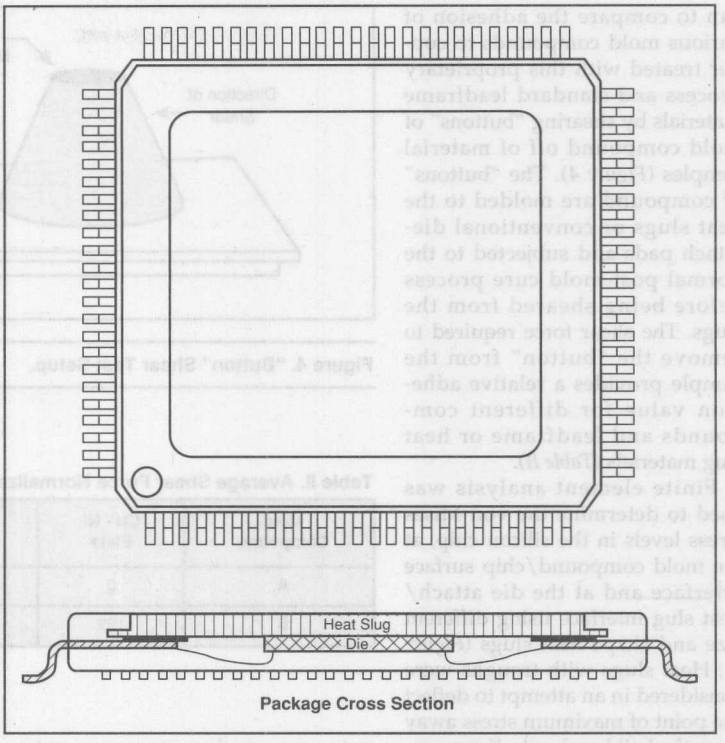


Figure 2. Package Outline Drawing — 100 TQFP TEP.

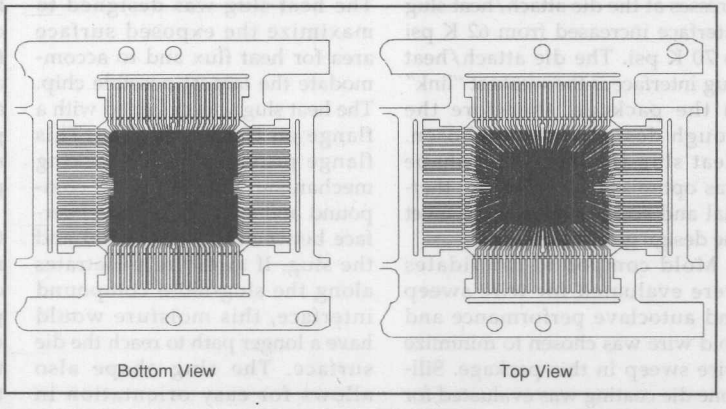


Figure 3. Leadframe with Attached Heat Slug.

run to compare the adhesion of various mold compounds to copper treated with this proprietary process and standard leadframe materials by shearing "buttons" of mold compound off of material samples (*Figure 4*). The "buttons" of compound are molded to the heat slugs or conventional die-attach pads and subjected to the normal post-mold cure process before being sheared from the slugs. The shear force required to remove the "button" from the sample provides a relative adhesion value for different compounds and leadframe or heat slug materials (*Table II*).

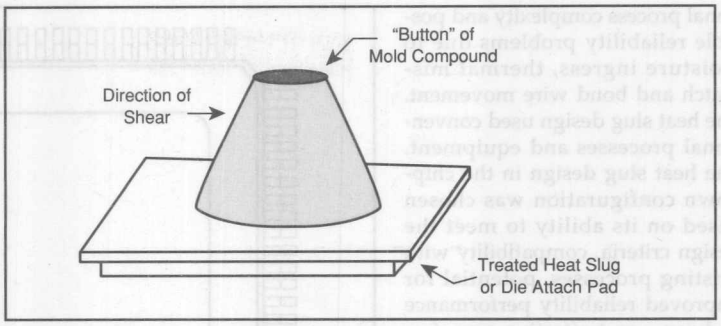


Figure 4. "Button" Shear Test Setup.

Table II. Average Shear Force Normalized for Button Area (psi).

Mold Compound	Cu - Ni Plate	Cu - Pd Plate	Cu - Proprietary Surface Finish
A	0	31	1017
B	182	130	1286

Finite element analysis was used to determine the von Mises stress levels in the silicon chip, at the mold compound/chip surface interface and at the die attach/heat slug interface using different size and shape heat slugs (*Figure 5*). Heat slugs with troughs were considered in an attempt to deflect the point of maximum stress away from the ball bond area. For example, in Cases 1 and 3 (Figure 5), while the stress at the ball bond was reduced from 7 K psi to 5.9 K psi with the addition of a trough, stresses at the die attach/heat slug interface increased from 62 K psi to 70 K psi. The die attach/heat slug interface is the weakest "link" in the package, therefore the trough design was not chosen. Heat slug thickness and shape was optimized by balancing thermal and stress responses to meet the design guidelines.

Mold compound candidates were evaluated for wire sweep and autoclave performance and gold wire was chosen to minimize wire sweep in this package. Silicone die coating was evaluated for enhanced die corrosion resistance, but test results showed that this extra processing step was not required to obtain the desired package reliability.

Design Features

The heat slug was designed to maximize the exposed surface area for heat flux and to accommodate the largest possible chip. The heat slug was designed with a flange on the top surface. This flange provides both a locking mechanism with the mold compound and a longer surface interface between the compound and the slug. If moisture penetrates along the slug-mold compound interface, this moisture would have a longer path to reach the die surface. The slug shape also allows for easy orientation in automated assembly processes (*Figure 6*).

The leadframe design employs a preplated palladium finish. The slug is attached to the leadframe using a two-sided adhesive film applied at high temperature. The film is cut in a "window-frame" configuration, providing support for all lead fingers. The package assembly operation starts with an assembled leadframe, which is processed using the same equipment and flows as conventional plastic packages.

The chip-down configuration of this package maximizes the thermal performance. The leadframe design allows the package to be processed conventionally (chip-up) through the molding operation (*Figure 7*). The package orientation is changed before lead form, but this change is transparent to the manufacturing process.

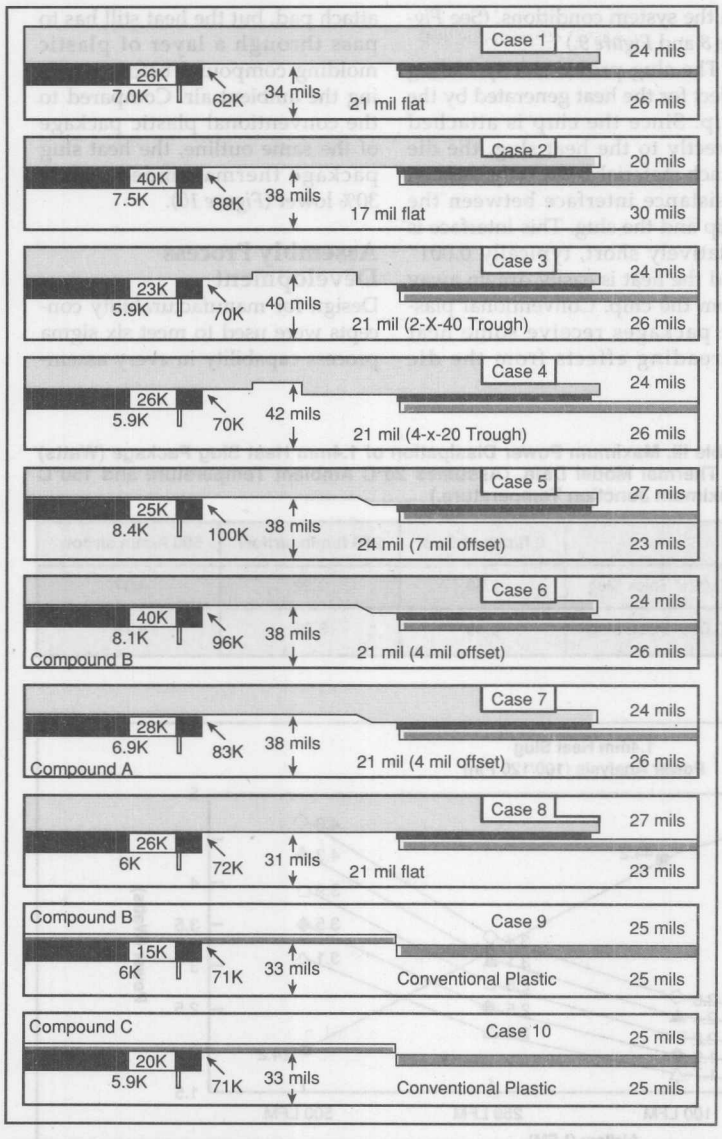


Figure 5. 100/120 Pin TQFP Heat Slug Stress Analysis Comparison of Critical Stress Sites Von Mises Stress (PSI).

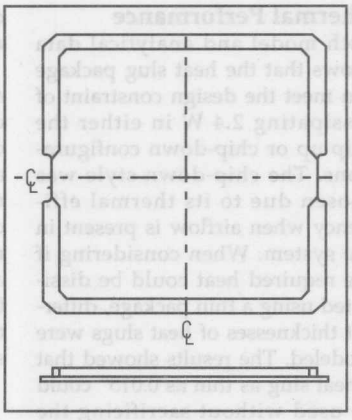


Figure 6. Heat Slug.

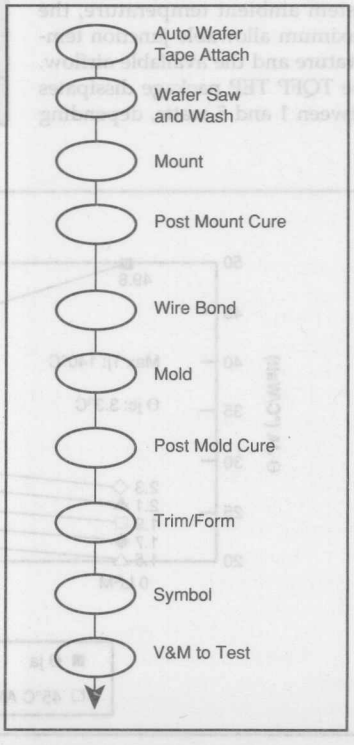


Figure 7. Assembly Process Flow.

Thermal Performance

Both model and analytical data shows that the heat slug package can meet the design constraint of dissipating 2.4 W in either the chip-up or chip-down configurations. The chip-down style was chosen due to its thermal efficiency when airflow is present in the system. When considering if the required heat could be dissipated using a thin package, different thicknesses of heat slugs were modeled. The results showed that a heat slug as thin as 0.015" could be used without sacrificing the desired performance (*Table III*).

Actual power dissipation of all packages is dependent on the thermal impedance of the package, the system ambient temperature, the maximum allowable junction temperature and the available airflow. The TQFP TEP package dissipates between 1 and 5 watts, depending on the system conditions. (See *Figure 8* and *Figure 9*.)

The slug provides a spreading effect for the heat generated by the chip. Since the chip is attached directly to the heat slug, the die attach material is the only thermal resistance interface between the chip and the slug. This interface is relatively short, typically 0.001" and the heat is easily drawn away from the chip. Conventional plastic packages receive some heat spreading effects from the die attach pad, but the heat still has to pass through a layer of plastic molding compound before reaching the ambient air. Compared to the conventional plastic package of the same outline, the heat slug package thermal impedance is 30% lower (*Figure 10*).

Assembly Process Development

Design for manufacturability concepts were used to meet six sigma process capability in every assem-

Table III. Maximum Power Dissipation of 1.4mm Heat Slug Package (Watts) — Thermal Model Data. (Assumes 25°C Ambient Temperature and 150°C Maximum Junction Temperature.)

	0 ft/min airflow	250 ft/min airflow	500 ft/min airflow
0.021" Thick Slug	2.56	3.32	4.37
0.015" Thick Slug	2.49	3.21	4.18

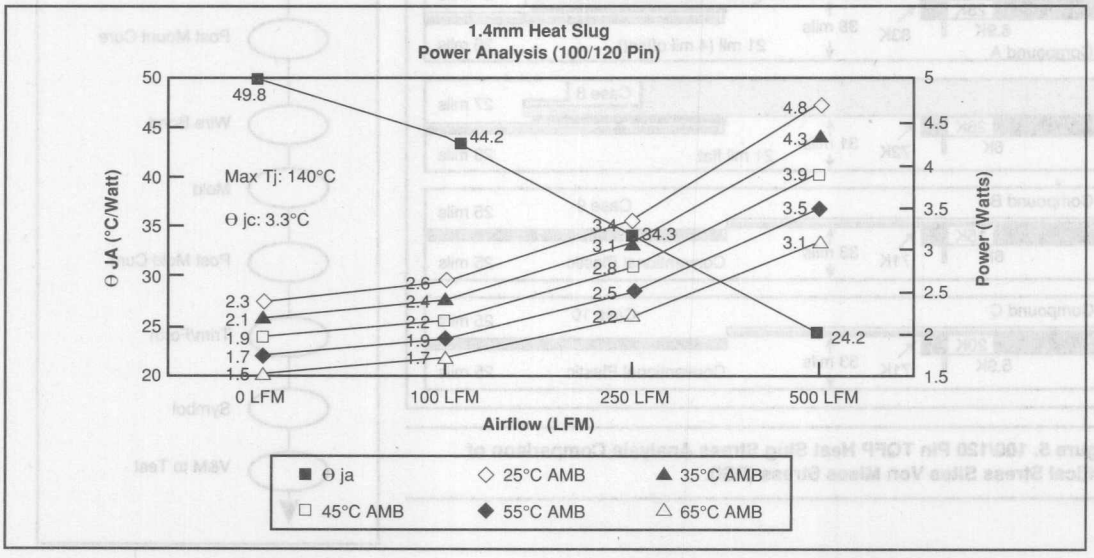


Figure 8. Power Dissipation at Scheduled Ambient Temperatures.

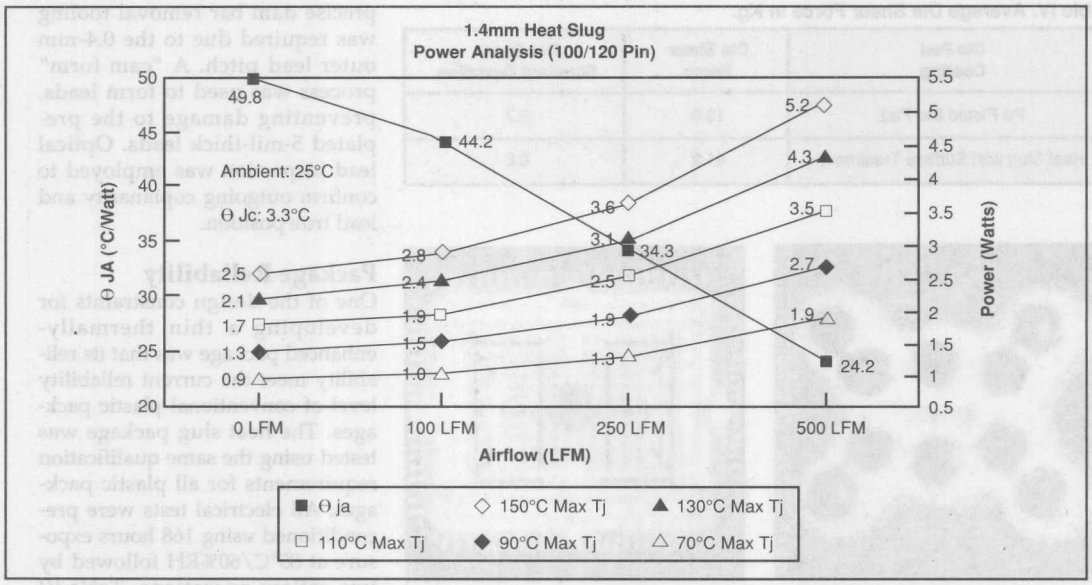


Figure 9. Power Dissipation at Selected Maximum Junction Temperatures.

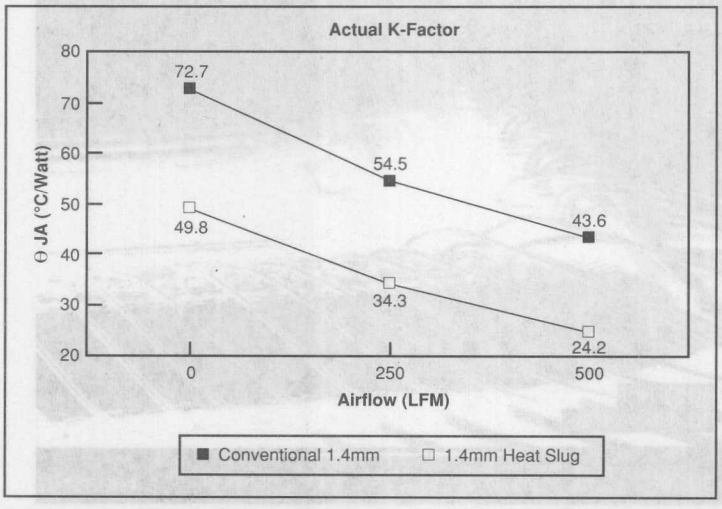


Figure 10. Thermal Impedance of Conventional vs. Heat Slug Packages.

bly process operation. Stress reduction and good thermal dissipation required a low stress die attach material with minimum voiding, thick bond line (>0.001″) and excellent adhesion characteristics. Several die attach materials, dispensing needles and parameters were evaluated to find the best combination. The evaluation efforts combined with the improved adhesion characteristics of the heat slug surface treatment yielded a substantial improvement in die shear strength compared with conventional Pd plated leadframes, as *Table IV* shows.

Optimum epoxy application parameters and customized dispenser needles designs allowed us to meet 100% epoxy coverage, less than 10% epoxy voiding and a minimum bond line thickness of 0.001″ (*Figure 11*).

Table IV. Average Die Shear Force in Kg.

Die Pad Coating	Die Shear Force	Die Shear Standard Deviation
Pd Plated Die Pad	13.0	2.7
Heat Slug with Surface Treatment	41.2	8.6

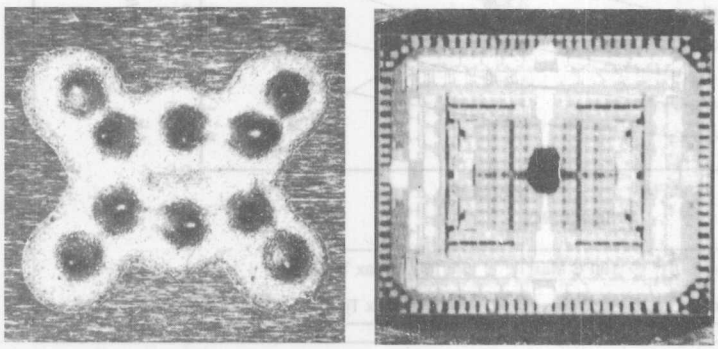


Figure 11. Epoxy Dispensing Pattern.

precise dam bar removal tooling was required due to the 0.4-mm outer lead pitch. A "cam form" process was used to form leads, preventing damage to the pre-plated 5-mil-thick leads. Optical lead inspection was employed to confirm outgoing coplanarity and lead true position.

Package Reliability

One of the design constraints for developing a thin thermally-enhanced package was that its reliability meet the current reliability level of conventional plastic packages. The heat slug package was tested using the same qualification requirements for all plastic packages. All electrical tests were preconditioned using 168 hours exposure at 85°C/60%RH followed by two reflow operations. *Table VI*

The heat slug leadframe subassembly required substantial wire bond process development. Heater block design was critical due to the presence of adhesive film in the bonding areas. The fine pitch leadframe fingers and the chip bonding pads required a new capillary design and utilization of advanced wire looping techniques (*Figure 12*).

Mold compounds were evaluated for wire sweep, voiding and moldability (*Table V*). The high-adhesion properties of the mold compound candidates required a unique mold die design, to assist in mold release. Both bond process and mold process optimization were used to minimize wire deflection during the encapsulation process (*Figure 13*).

Devices are symbolized using a proprietary laser process. Ultra

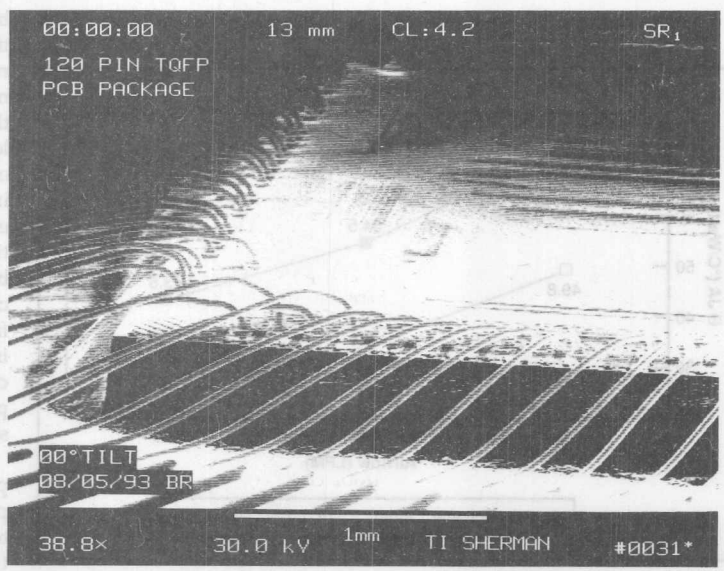


Figure 12. Wire Looping — 120 TQFP.

Table V. Mold Compound Evaluations — Wire Sweep. (*Wire Sweep % Deflection for Various Mold Compounds on 100 Pin TQFP Packages.)

Mold Compound	Compound A	Compound C	Compound D	Compound B	Compound B	Compound E	Compound F
Package Thickness (mm)	1.57	1.9	1.4	1.9	1.4	1.9	1.9
Average (%)	7.02	4.50	5.50	2.89	5.33	4.56	6.94
STD DEV (%)	1.86	1.81	1.37	1.16	1.01	1.07	1.19

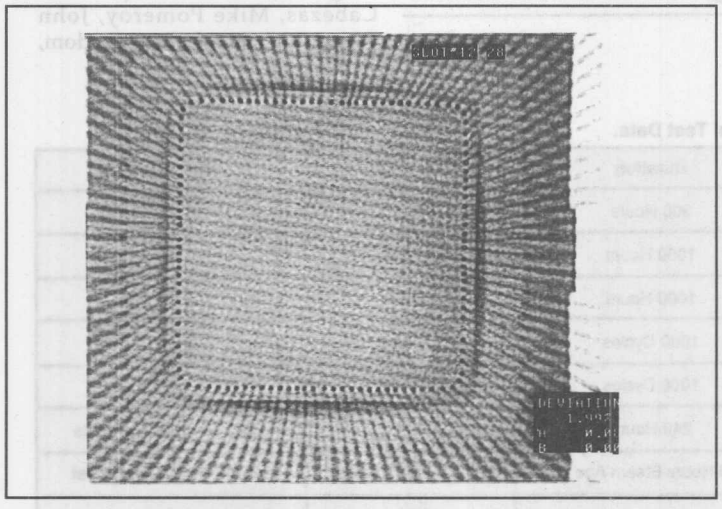


Figure 13. Molded Wires.

describes the results of this reliability qualification testing.

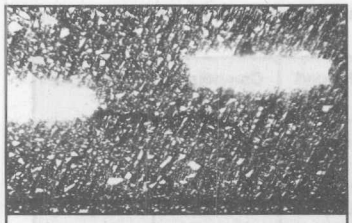
The moisture sensitivity tests were performed per the proposed IPC-SM-786A Level 1 and Level 2 conditions, 168 hours of 85 °C/85 %RH and 168 hours of 85 °C/60 %RH, respectively. The heat slug package passed both Level 1 and Level 2 moisture sensitivity tests, showing no degradation in delamination nor internal cracking after stressing. This is superior performance to a conventional plastic TQFP package. The photos in *Figure 14* show a typical crack in a TQFP package after Level 1 testing and the heat slug package after identical stress conditions (Figure 14).

Level 1 conditions equate to an unlimited exposure time at factory floor conditions of 30°C/ 60%RH and no special "dry" packaging. The Level 2 conditions equate to an exposure time of one year at 30°C/60%RH, providing the devices are protected during shipping and storage using a "dry" packaging scheme. This package provides an excellent opportunity to eliminate the need for desiccated packaging and special handling in a customer's factory.

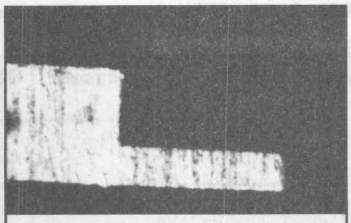
Conclusions

A thermally-enhanced plastic IC package has been developed by a cross-functional team from engineering and manufacturing to meet the constraints of space and power required by the customer. The package was developed with a primary goal of efficiency of manufacturing and compatibility with current plastic package assembly equipment and processes.

The TQFP TEP uses a leadframe subassembly, with a heat slug attached by two-sided adhesive film. This leadframe is processed through conventional assembly processes and equipment, with a change of orientation after the mold process. The proprietary surface treatment of the copper heat slug provides a tenfold improvement in mold compound adhesion and a threefold improvement in die attach adhesion compared to conventional leadframe surface finishes. The slug also provides stability to the thin package, preventing warpage. This package represents a substantial step forward in the quest for plastic IC



Typical Crack in TQFP Package Resulting from "Popcorn Effect"



TQFP TEP Package with No Cracks

Figure 14. Cross Sections of TQFP Packages After 168 Hours 85°C/85%RH.

packages that can meet the ever-increasing power and board space requirements of the electronics industry.

Acknowledgments

The authors would like to express their sincere appreciation to the following people, without whose contributions the development of this package would not have been possible: Bobby O'Donley, Mario Magaña, John Tellkamp, Pedro Cabezas, Mike Pomeroy, John Wiley, Rich Brook, Ray Purdom,

Table VI. 120 Pin TQFP TEP Environmental Test Data.

Test	Duration	Result	Comments
150°C HTRB	300 Hours	0/116	
85°C/85%RH THB	1000 Hours	0/116	
150°C Storage Life	1000 Hours	0/45	
–65°C/150°C Temperature Cycle	1000 Cycles	0/116	
–65°C/150°C Thermal Shock	1000 Cycles	0/116	
121°C/2 ATM Autoclave	240 Hours	0/76	Used Ceramic Substrate
Solderability	8 Hours Steam Age	0/22	Used Ceramic Plate Test
Lead Fatigue		0/22	
Lead Pull	To Destruction	0/22	
Lead Finish Adhesion		0/15	
Salt Atmosphere	24 Hours	0/22	
X-Ray	Top Only	0/5	
Physical Dimension		0/5	
Flammability	A	0/5	
	B	0/5	

	Condition	Electrical	Cracks
Moisture Sensitivity	168 Hours 85°C/85%RH	0/10	0/10
	168 Hours 85°C/60%RH	0/10	0/10

Terrill Sallee, Jim Fielding, Tomas Luna, Brenda Gogue, Steve Groothius, Dick Shaw, Jim Sisco, Jay Alexander, Archie Sutton, Herb Wyman and others who may have been omitted.



Edgar R. Zuniga

Edgar Zuniga has been involved with the development of new packages since 1989, first as part of the group that developed the 48- and 56-pin SSOP packages. For the last two years he has served as the team leader in the development of the 100- and 120-pin TQFP TEP packages. Before this, Edgar spent two years as engineering section head manager for the assembly operations in the Flexible Assembly Module in Sherman (FAM) and one year as assembly process engineer.

He joined TI in 1975 at the TI plant in El Salvador as a process engineer in the assembly operation. He transferred to Sherman in 1986.

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Larry Nye

Larry Nye is currently a member of the package development team within the Advanced System Logic Organization. Since 1983, Larry has been heavily involved in die attach and bonding process development activities including programs such as palladium bonding process development, copper wire bonding, low temperature bonding, hermetic chip, bonds over active circuits (BOAC), rapid cure process (RCP), and others.

Besides his development responsibilities, Larry serves as the ASL representative on the Worldwide Mount Commodity Team, the Worldwide Gold Wire Commodity Team and the Worldwide Bond Process Standardization Team. Additional responsibilities include thermal and stress modeling activities along with material characterization and qualification. He joined TI in 1983.

Larry has presented papers twice at the international electronic packaging conference on thermal analysis of semiconductor packages. He has written other papers on palladium bonding and thermal modeling of semiconductor packages. In addition, Larry has served as a co-author on papers dealing with thermal modeling, experimental design, semiconductor package design, and bonds over active circuits (BOAC). He currently has two patents pending in the U.S. patent office.



Mary Helmick

Mary Helmick is part of the package development group for the Advanced System Logic Department in Sherman. Mary joined TI in 1990 as part of the 48- and 56-pin SSOP package development team in the ASL Test/Finish area (formerly FAM). Since 1991 she has been part of ASL packaging engineering, working on the 100/120 pin Heat Slug Package Development Team.

She received her bachelor of science in mechanical engineering from Purdue University in 1986 and her master's degree in computer integrated design and manufacturing from George Washington University in 1989. ❑

FIFO Surface-Mount Packages for PCMCIA Applications

Tom Jackson
Advanced System Logic – Semiconductor Group

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Introduction

As today's applications become more complex and integrated, there is a continuing need to reduce board space without sacrificing functionality. This need has never been greater than for Personal Computer Memory Card International Association (PCMCIA) cards. The appeal for PC card adapters in large area network (LAN) is due to the small form factor and performance. PCMCIA card designers face the challenge of reducing current half-size boards (typically 4.5 in × 8 in) such as those used in present desktop systems, to the size of a credit card.

With the emergence of notebook computers, personal data assistants (PDAs), and wireless communications, designers are turning to PCMCIA cards to meet the growing demand for more flexibility. This trend has driven the chip-set manufacturers to reduce the number of add-on features normally designed into desktop computers to fit the board confines of portable systems. PCMCIA cards provide an alternative: standard add-on features in a miniature-portable format. Until the introduction and standardization of PCMCIA cards, portable systems were left virtually unconnected to other systems and peripherals. Many of the PCMCIA designs provide the needed interconnectedness between systems by performing input/output (I/O) data functions. Typical I/O adapters found today are EtherNet, faxes, SCSI, and modems, to name a few.

As bus widths and data speeds increase, so does the chance of data bottlenecks and latency. Specialty memories such as FIFOs are required for either rate matching or clock partitioning from data buses and processors. Until now, many designers either had to compromise performance or increase device count due to the lack of PCMCIA-compliant FIFO packaging. Texas Instruments (TI) has met the challenge of reduced board area and increased integration with their advanced FIFO memories. TI offers 9-, 18-, and 36-bit high-performance FIFO memories in the PCMCIA-compatible thin quad flat package (TQFP).

PCMCIA

PCMCIA was founded in 1989 to define and set PC-card standards. In today's market, there are three widely accepted standards: Type I, ratified in June 1990; Type II, ratified in September 1991; and Type III, which is pending. PCMCIA cards all share a common length and width, differing only in their height (see Figure 1).

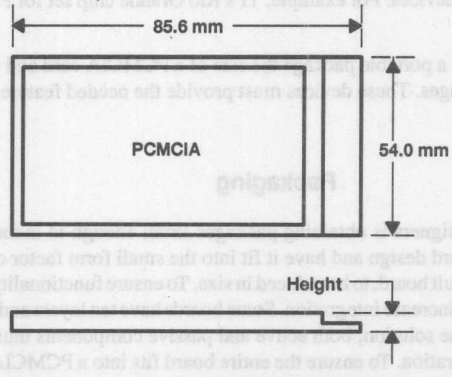
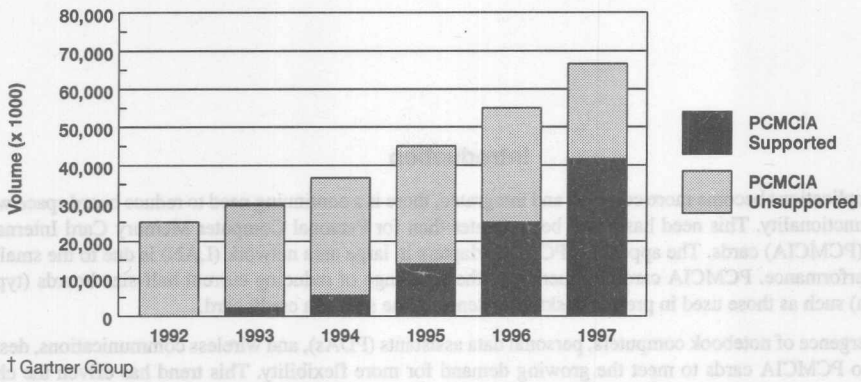


Figure 1. PCMCIA Card Dimensions

Due to the increased popularity of PCs (i.e., laptops, notebooks, and PDAs), a demand for the same functionality as found in larger PC counterparts has arisen. To keep pace with the growing market demand, portable-computer manufacturers have begun to support PCMCIA card ports on nearly all new designs (see Figure 2).



† Gartner Group

Figure 2. Portable Computers Supporting PCMCIA Cards†

In the past, PCMCIA cards were seen as a way to easily upgrade system memory without adding storage overhead to the already compact chip sets. Today, PCs are replacing hardwired-desktop networked systems as the main computing unit. The need to provide for system interconnection and data communications has targeted new PCMCIA designs for LAN, fax, and modem-adapter cards. These applications typically are found in Type II PCMCIA cards. Other designs such as subminiature disk drives and wireless radio frequency communication adapters typically found in Type III PCMCIA cards (see Table 1).

Table 1. PCMCIA Card Applications

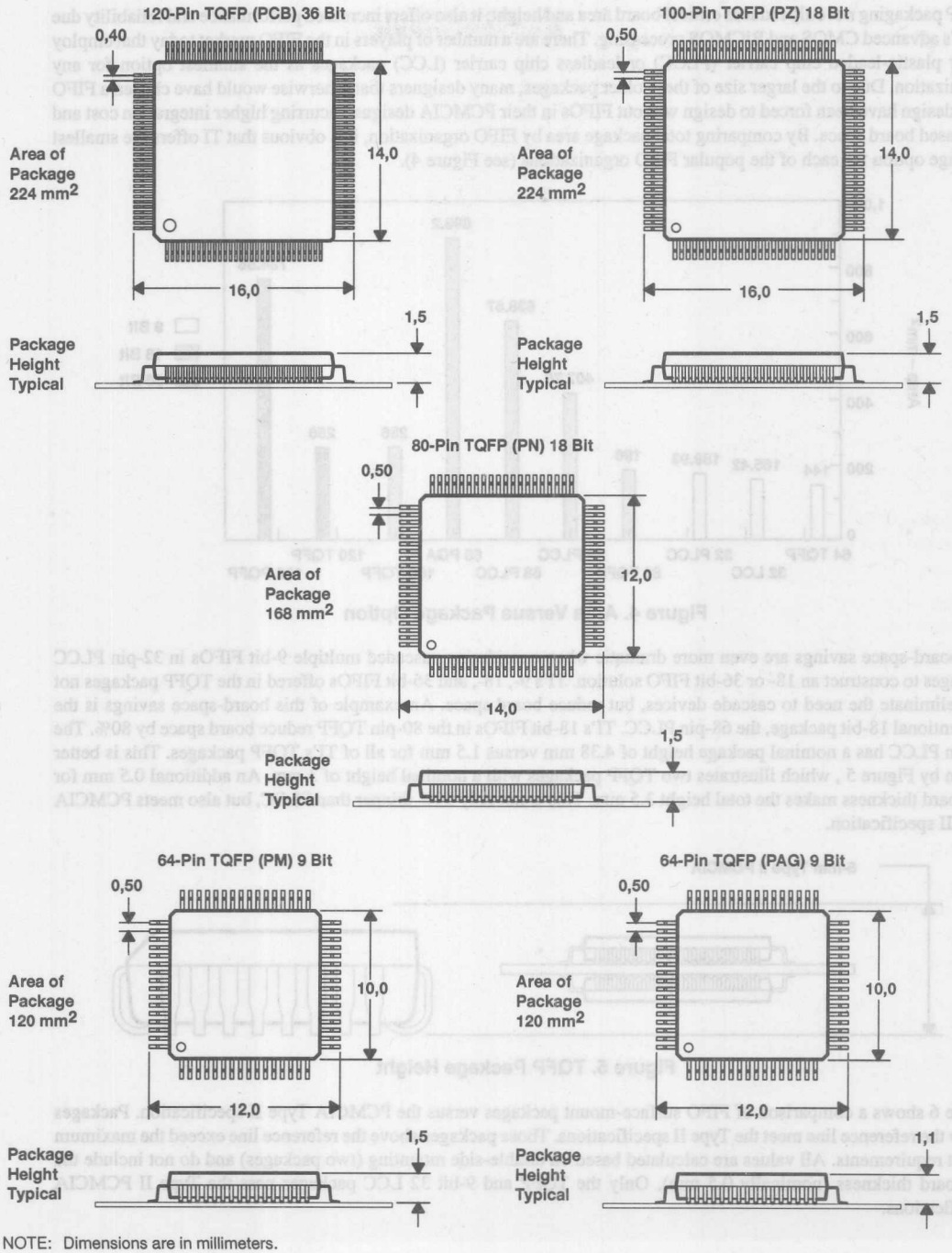
TYPE	HEIGHT	APPLICATION
I PC	3.3 mm	Memory devices: Flash, DRAM, OTP, and high-speed add-ons
II PC	5 mm	I/O devices: Fax, modems, and LAN adapters
III PC	10.5 mm	Wireless devices: RF-communications devices and submini disk drives

Type I cards are focused mainly for plug-in memory. Type II and Type III cards are gaining ground in many new applications. Type II cards are used mainly for I/O applications such as those listed in Table 1. The growing acceptance of PCMCIA cards for I/O interface has caused manufacturers of DSPs, CODECs, bus-interface devices, and ASICs to begin producing PCMCIA-compliant devices. For example, TI's Rio Grande chip set for PCI features ports to support two PCMCIA cards.

There is a demand for these features in a portable package the size of a PCMCIA card and an even greater demand for devices in PCMCIA-compatible packages. These devices must provide the needed features, consume less power, and require less critical board space.

Packaging

The primary obstacle facing many designers is obtaining packages small enough to incorporate into their PCMCIA designs. To shrink a current adapter-card design and have it fit into the small form factor of a PCMCIA card requires all components, not just the printed circuit board, to be reduced in size. To ensure functionality is not lost, many designers implement multilayered boards to help increase integration. Some boards have ten layers and measure only 0.03 in thick. Multilayered boards are only part of the solution; both active and passive components must be dual-side mounted for maximum chip count and overall integration. To ensure the entire board fits into a PCMCIA form requires specialized packaging from the device manufacturers. Since FIFOs play a key role in the functionality of many of these designs, TI has utilized board-space-saving TQFP packaging across 9-, 18-, and 36-bit FIFO product lines (see Figure 3).



NOTE: Dimensions are in millimeters.

Figure 3. FIFO Package Dimensions

TQFP packaging not only reduces critical board area and height; it also offers increased performance and reliability due to TI's advanced CMOS and BiCMOS processing. There are a number of players in the FIFO market today that employ either plastic-leaded chip carrier (PLCC) or leadless chip carrier (LCC) packages as the smallest option for any organization. Due to the larger size of these older packages, many designers that otherwise would have chosen a FIFO for a design have been forced to design without FIFOs in their PCMCIA designs, incurring higher integration cost and increased board space. By comparing total package area by FIFO organization, it is obvious that TI offers the smallest package option for each of the popular FIFO organizations (see Figure 4).

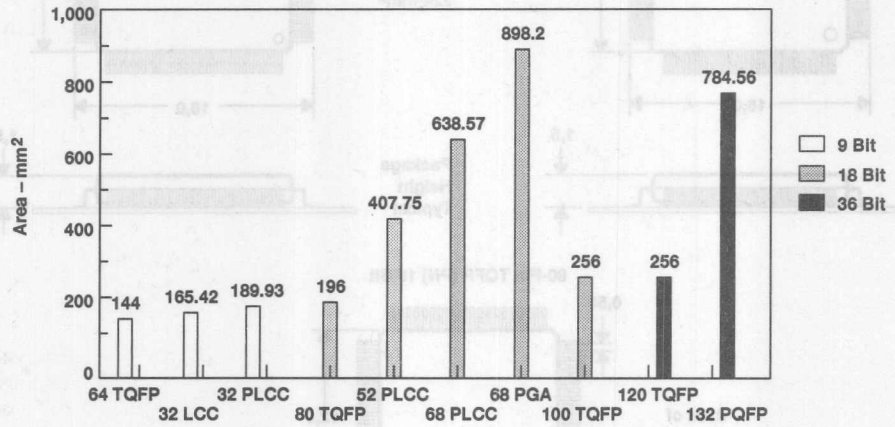


Figure 4. Area Versus Package Option

The board-space savings are even more dramatic when considering cascaded multiple 9-bit FIFOs in 32-pin PLCC packages to construct an 18- or 36-bit FIFO solution. TI's 9-, 18-, and 36-bit FIFOs offered in the TQFP packages not only eliminate the need to cascade devices, but reduce board space. An example of this board-space savings is the conventional 18-bit package, the 68-pin PLCC. TI's 18-bit FIFOs in the 80-pin TQFP reduce board space by 80%. The 68-pin PLCC has a nominal package height of 4.38 mm versus 1.5 mm for all of TI's TQFP packages. This is better shown by Figure 5 , which illustrates two TQFP packages with a nominal height of 3 mm. An additional 0.5 mm for PC board thickness makes the total height 3.5 mm. This is not only 20% thinner than PLCC, but also meets PCMCIA Type II specification.

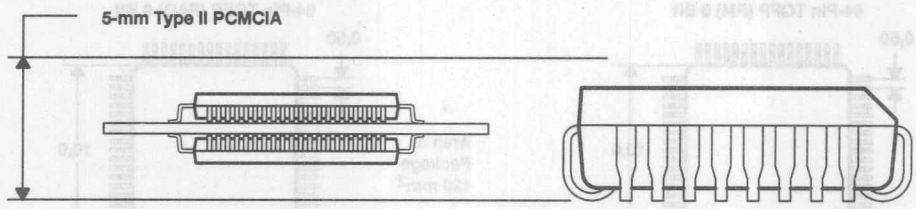


Figure 5. TQFP Package Height

Figure 6 shows a comparison of FIFO surface-mount packages versus the PCMCIA Type II specification. Packages below the reference line meet the Type II specifications. Those packages above the reference line exceed the maximum height requirements. All values are calculated based on double-side mounting (two packages) and do not include the PC board thickness (nominally 0.5 mm). Only the TQFP and 9-bit 32 LCC packages pass the Type II PCMCIA specifications.

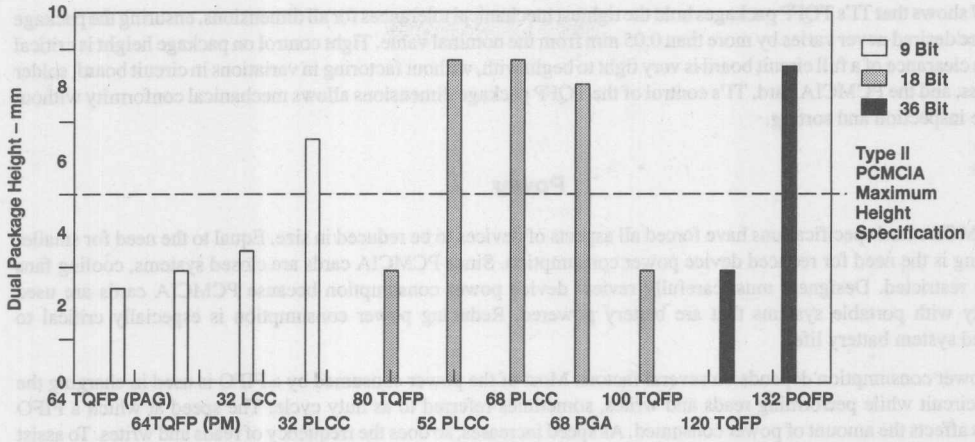


Figure 6. Type II PCMCIA Package Height Versus Dual Package Solutions†

† Board thickness is not included.

Although the LCC package may physically fit the requirements for PCMCIA cards, it does not permit optimum system design, since so much of the board area is occupied by one device. TI FIFOs available in TQFP packages allow a designer to choose the architecture and features that best meet the design criteria and dramatically reduce critical board space.

Another critical point to consider in PCMCIA design is package dimensioning and tolerances. As previously stated, the nominal values specified for a package may appear to meet PCMCIA card specification. However, due to different techniques involved in the mold processes of different packages, designers must carefully review all specifications given in the mechanical drawings for each package. In the case of the 32-pin LCC, the height tolerance varies greatly from a minimum of 1.27 mm to a maximum of 2.2 mm, a variance of 57% (see Figure 7).

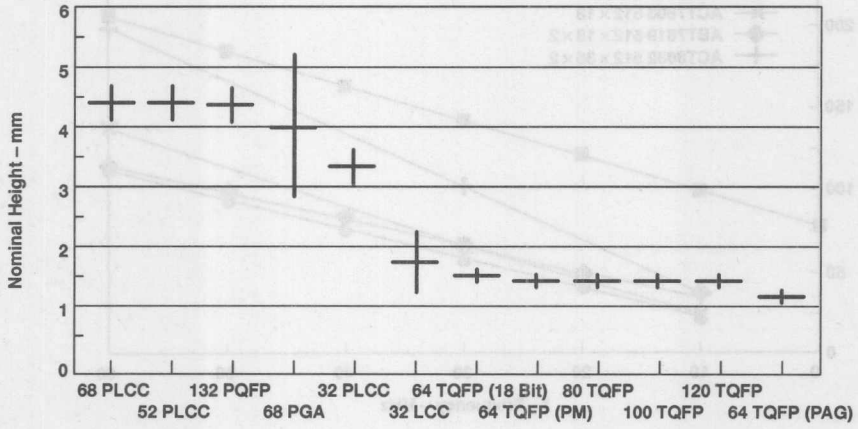


Figure 7. Typical Package Height Versus Height Variance

Figure 7 shows that TI's TQFP packages hold the tightest mechanical tolerances for all dimensions, ensuring the package clearance desired never varies by more than 0.05 mm from the nominal value. Tight control on package height is critical because clearance of a full circuit board is very tight to begin with, without factoring in variations in circuit board, solder thickness, and the PCMCIA card. TI's control of the TQFP package dimensions allows mechanical conformity without package inspection and sorting.

Power

The PCMCIA card specifications have forced all aspects of devices to be reduced in size. Equal to the need for smaller packaging is the need for reduced device power consumption. Since PCMCIA cards are closed systems, cooling fans are size restricted. Designers must carefully review device power consumption because PCMCIA cards are used primarily with portable systems that are battery powered. Reducing power consumption is especially critical to increased system battery life.

FIFO power consumption depends on several factors. Most of the power consumed by a FIFO is used in charging the CMOS circuit while performing reads and writes, sometimes referred to as duty cycle. The speed at which a FIFO operates affects the amount of power consumed. As speed increases, so does the frequency of reads and writes. To assist designers in calculating power, TI provides an I_{CC} versus frequency plot for each FIFO in the Sept. 1994 High-Performance FIFO Memories data book (literature number SCAD003B). Because the duty cycle and clock frequency at which a FIFO is operated depend on the design, TI has implemented a unique circuit feature on its advanced FIFOs, i.e., dynamic-sense amplifiers. Dynamic-sense amplifiers draw power only during a read or write operation; otherwise, they are idle, drawing less than 400 µA. Conventional FIFOs implement static-sense amplifiers that draw power even when the device is idle (approximately 50 mA). TI's dynamic-sense amplifiers are designed to optimize maximum performance without any degradation of propagation delay times. Figure 8 is a comparison of TI's 9-, 18-, and 36-bit clocked FIFOs with several conventional synchronous 9-bit FIFOs. The synchronous 9-bit FIFOs all draw more than 50 µA when idle. As system speed increases, so does the amount of power consumed. As speeds approach 60 MHz, the 9-bit synchronous FIFO draws more power than TI's clocked 36-bit FIFOs.

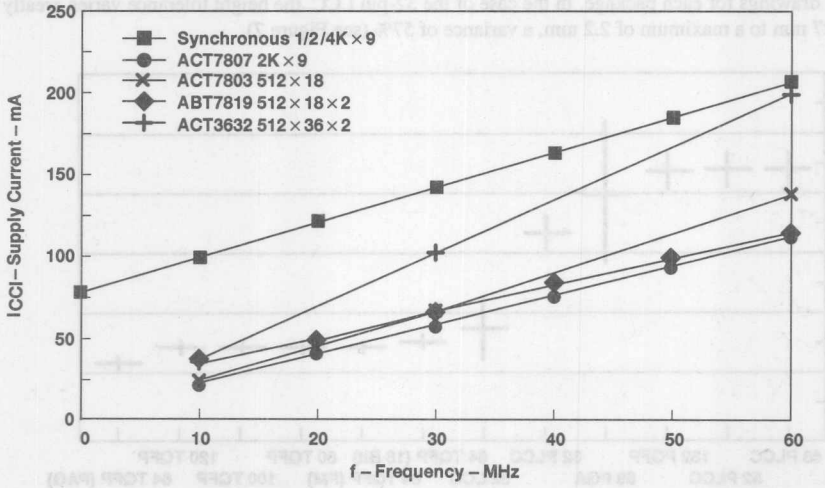


Figure 8. Active I_{CC} Versus Frequency

Using the following equation, an accurate power calculation can be made for any FIFO device.

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

Where:

I_{CC} = power-down supply current maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitance load
f_i = data input frequency
f_o = data output frequency

The power consumption of a single 9-bit device is an important consideration, since many designs require 18- or 36-bit FIFO solutions. Since power consumption is primarily a factor of the number of outputs switching, reducing power consumption with wider-word-width FIFOs is critical [for example, the total power consumption of a 1K × 36 FIFO when constructed by cascading four 1K × 9 FIFOs (see Figure 9)]. TI's single-chip solution, the SN74ACT3641, not only saves 65% board space, but reduces power consumption by 78% when operating at 60 MHz.

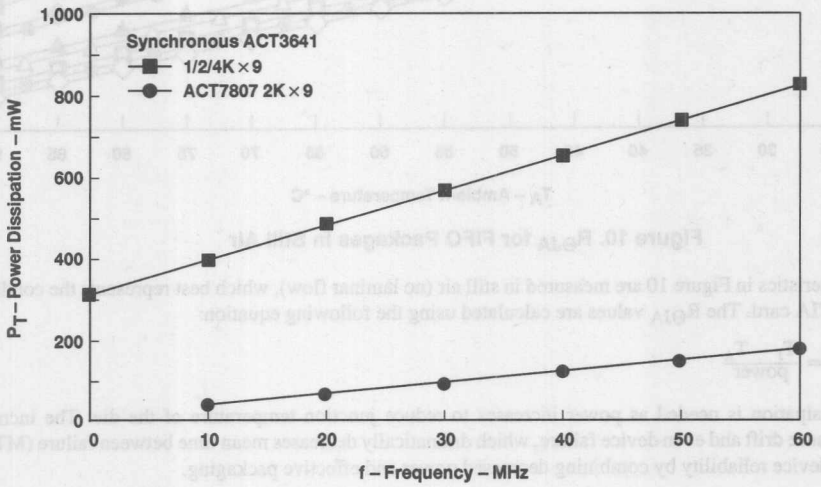


Figure 9. Multiple 9-Bit Solution Versus Single 36-Bit FIFO

Thermal Resistance

As with any small package, thermal considerations must be taken into account. Any heat generated by a device must be dissipated to ensure proper operation. The heat dissipation of a package is measured in terms of thermal resistance (R_Θ). $R_{\Theta JA}$ is defined as the thermal resistance from the die junction to ambient air. Figure 10 shows a listing of all TI's surface-mount packages and their associated $R_{\Theta JA}$ values. The listed values are measured in still air, which is a better representation of the true operating conditions of a FIFO in a PCMCIA card. The 120-pin TQFP is an example of TI's new thermally enhanced packaging (TEP) technology. The 120-pin TQFP has a heat spreader mounted to the top of the package and the die is mounted underneath in a dead-bug fashion. The 120-pin TQFP has the same $R_{\Theta JA}$ characteristics as the larger 132-pin PQFP and is 67% smaller. The heat dissipation similarities between the two packages are due to the addition of a heat spreader built into the 120-pin TQFP.

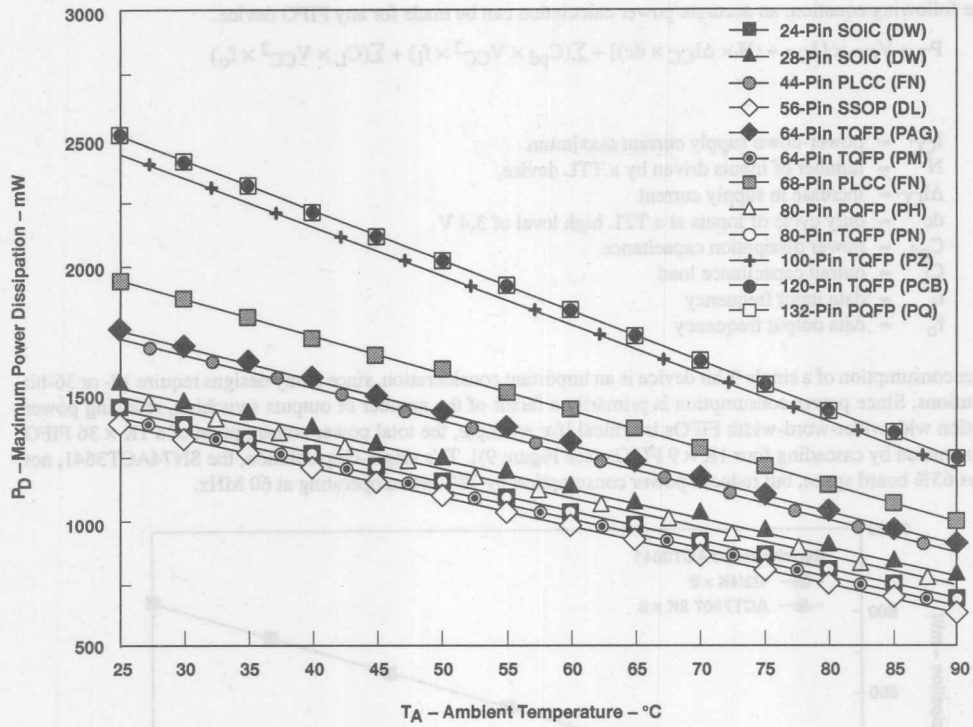


Figure 10. $R_{\Theta JA}$ for FIFO Packages in Still Air

The $R_{\Theta JA}$ characteristics in Figure 10 are measured in still air (no laminar flow), which best represents the conditions of a closed PCMCIA card. The $R_{\Theta JA}$ values are calculated using the following equation:

$$R_{\Theta JA} = \frac{T_J - T_A}{\text{power}}$$

Effective heat dissipation is needed as power increases to reduce junction temperature of the die. The increased temperature can cause drift and even device failure, which dramatically decreases mean time between failure (MTBF). TI has improved device reliability by combining decreased power and effective packaging.

Conclusion

As the demand for PCMCIA card continues, so does the demand for lower power and more space-saving packages. TI has met both demands with TQFP packages for their advanced CMOS and BiCMOS FIFOs. The TQFP package dramatically reduces board space over conventional packaging and eliminates the need to cascade multiple FIFOs to create 18- and 36-bit FIFO solutions. The implementation of dynamic-sense amplifiers on all advanced FIFOs reduces power consumption and; therefore, improves system reliability and provides longer battery life for portable systems.

Package Outlines and Thermal Data

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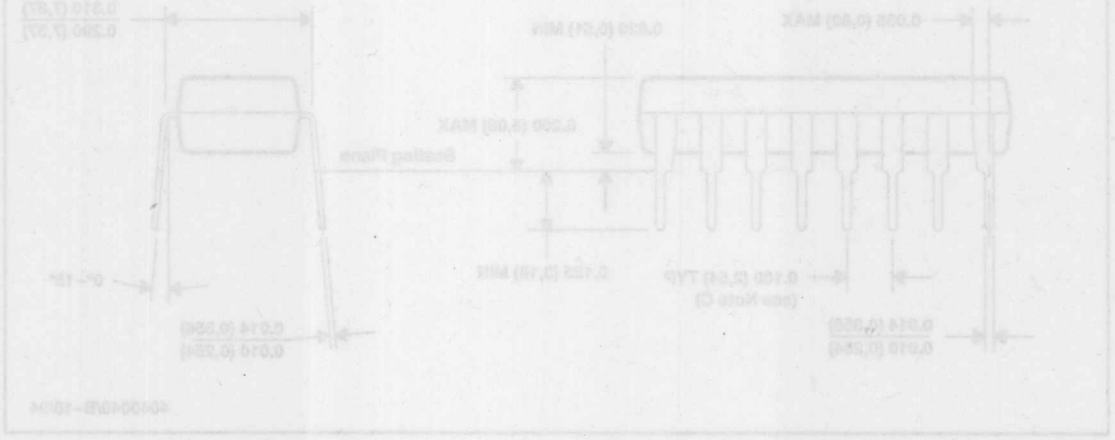
Package Outlines and Thermal Data

Introduction

The remainder of this section contains mechanical and thermal data for each package offered for TI's FIFOs.

The mechanical data consists of drawings of each package annotated with critical dimensions. These drawings typically include the following dimensions: lead pitch (tip to tip); body width and length; shoulder-to-shoulder insertion width; lead width, thickness, and angles; and package maximum height and stand-off clearances from seating plane to bottom of the package. For packages designed in English units, inch dimensions are shown first followed by millimeter dimensions in parentheses. A period is used as the English units decimal point and a comma as the metric units decimal point. The official JEDEC descriptor is used to identify each package type.

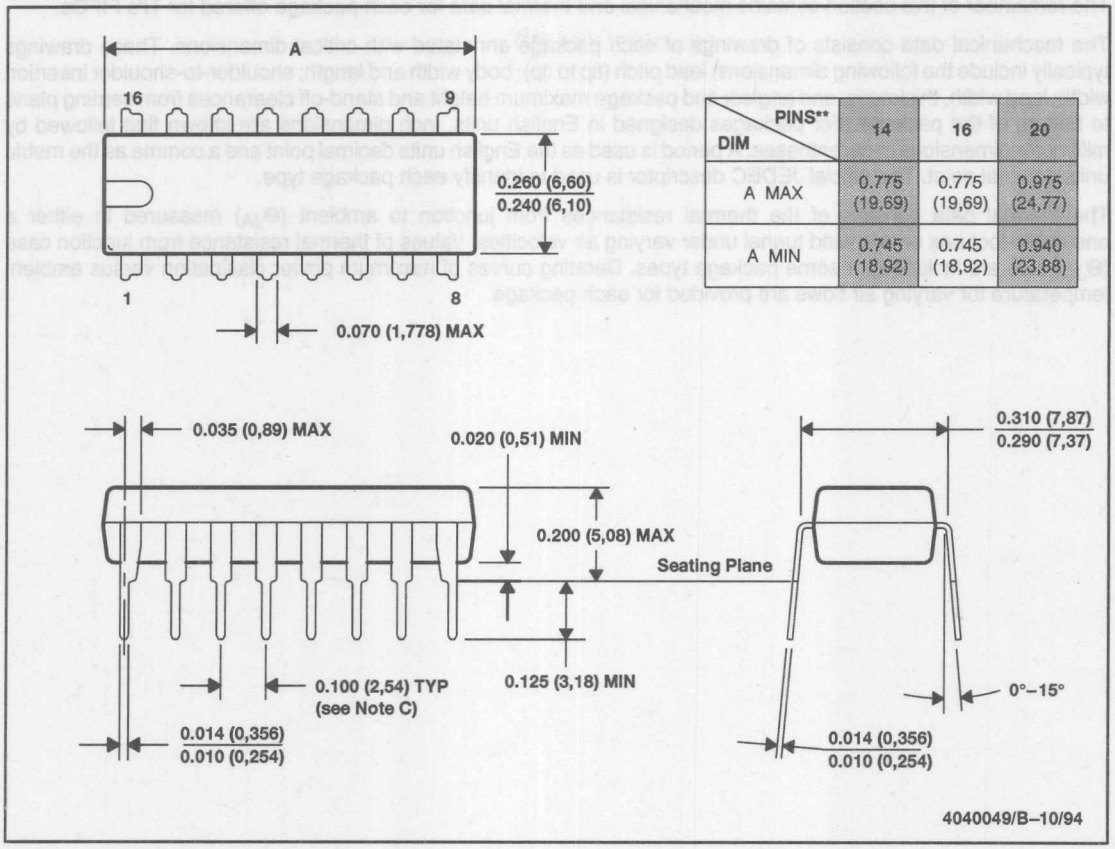
The thermal data consists of the thermal resistances from junction to ambient (Θ_{JA}) measured in either a one-cubic-foot box or in a wind tunnel under varying air velocities. Values of thermal resistance from junction case (Θ_{JC}) also are included for some package types. Derating curves of maximum power dissipation versus ambient temperature for varying air flows are provided for each package.



N/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

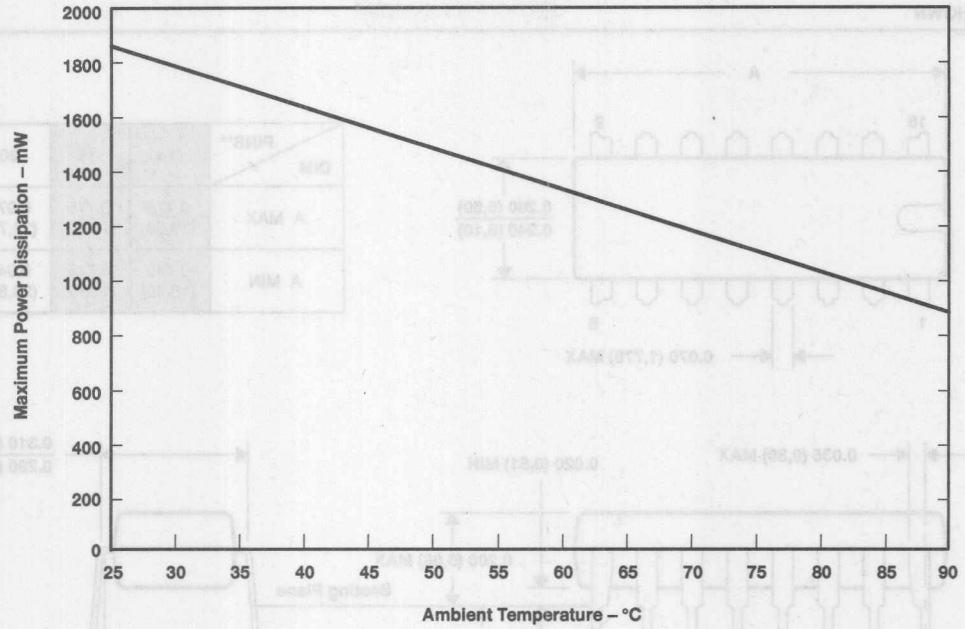
16 PIN SHOWN



DIM \ PINS**	14	16	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.940 (23,88)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.

16-Pin DIP (N) Package Power Dissipation Derating in Still Air



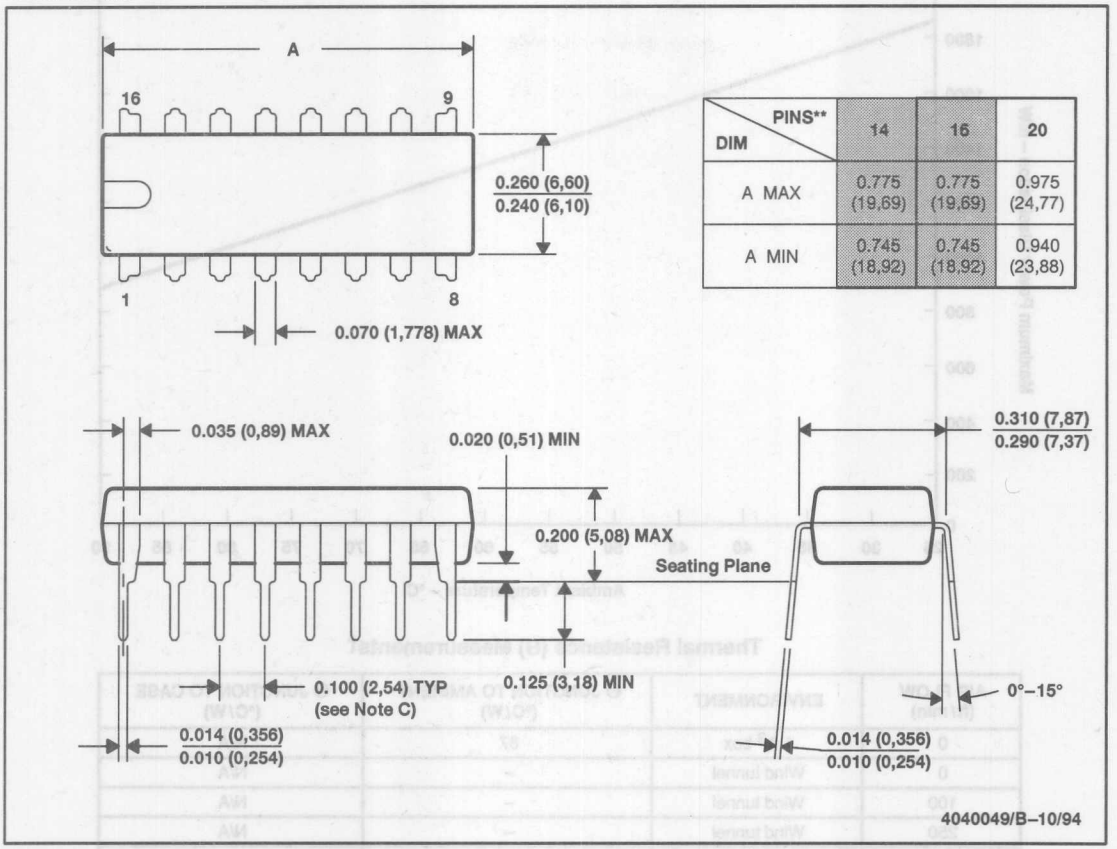
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	67	N/A
0	Wind tunnel	–	N/A
100	Wind tunnel	–	N/A
250	Wind tunnel	–	N/A
500	Wind tunnel	–	N/A
N/A	N/A	N/A	26

† Mounted on printed-circuit board

N/R-PDIP-T** **PLASTIC DUAL-IN-LINE PACKAGE**

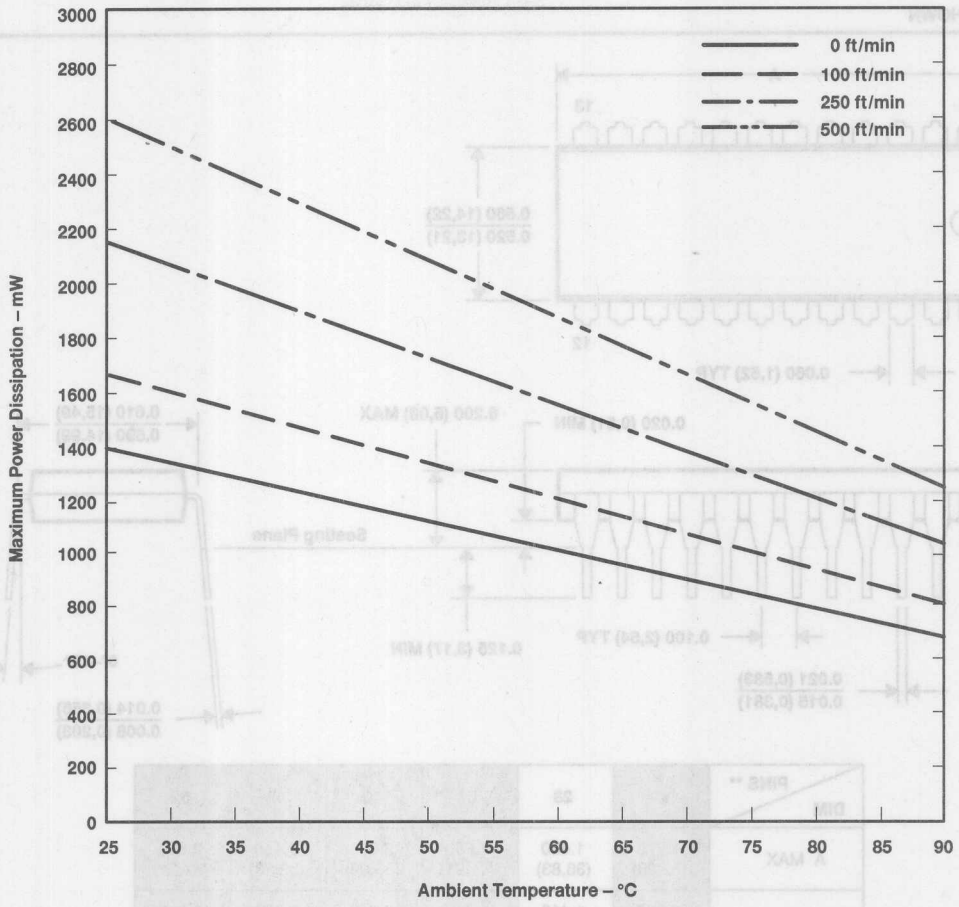
16 PIN SHOWN



DIM \ PINS**	14	16	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.940 (23,88)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.

20-Pin DIP (N) Package Power Dissipation Derating at Varying Air Flows



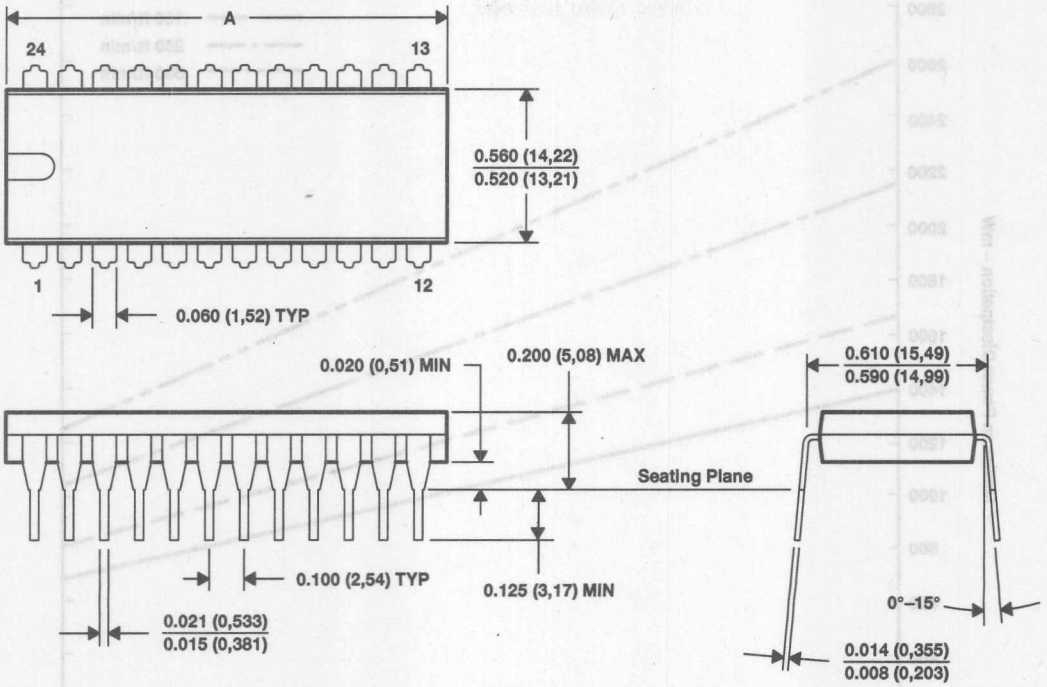
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	67	N/A
0	Wind tunnel	90	N/A
100	Wind tunnel	75	N/A
250	Wind tunnel	58	N/A
500	Wind tunnel	48	N/A
N/A	N/A	N/A	33

† Mounted on printed-circuit board

N/R-PDIP-T** PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN

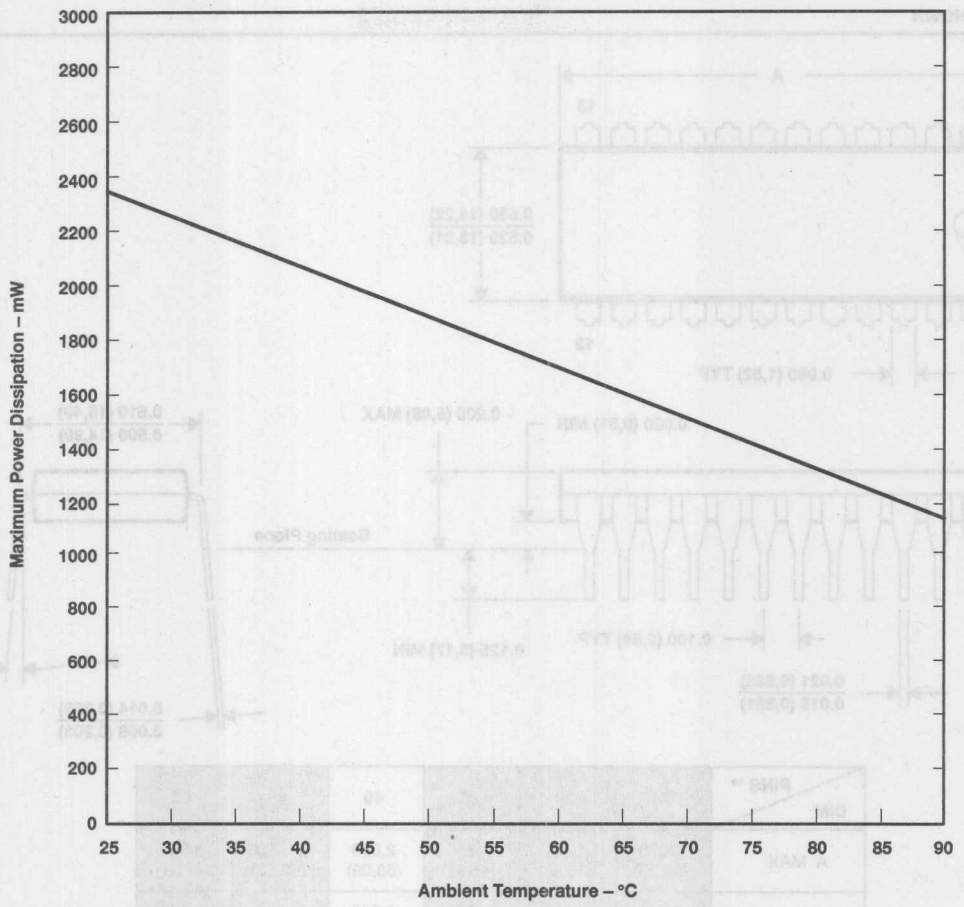


DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/B–10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

28-Pin DIP (N) Package Power Dissipation Derating in Still Air



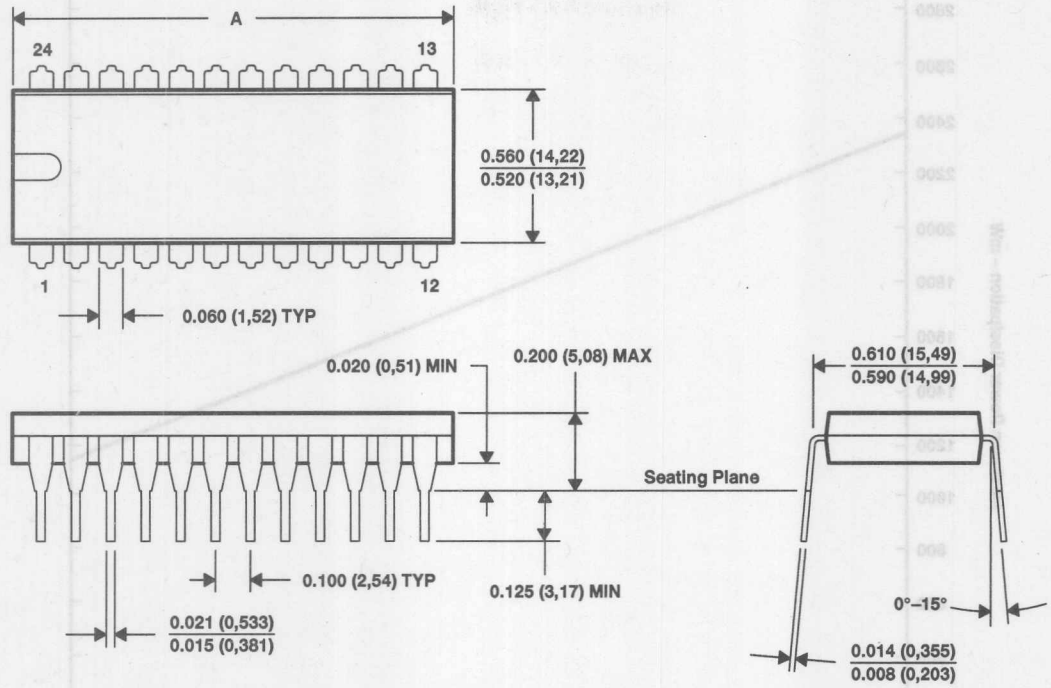
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	53	N/A
0	Wind tunnel	–	N/A
100	Wind tunnel	–	N/A
250	Wind tunnel	–	N/A
500	Wind tunnel	–	N/A
N/A	N/A	N/A	20

† Mounted on printed-circuit board

N/R-PDIP-T** **PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN

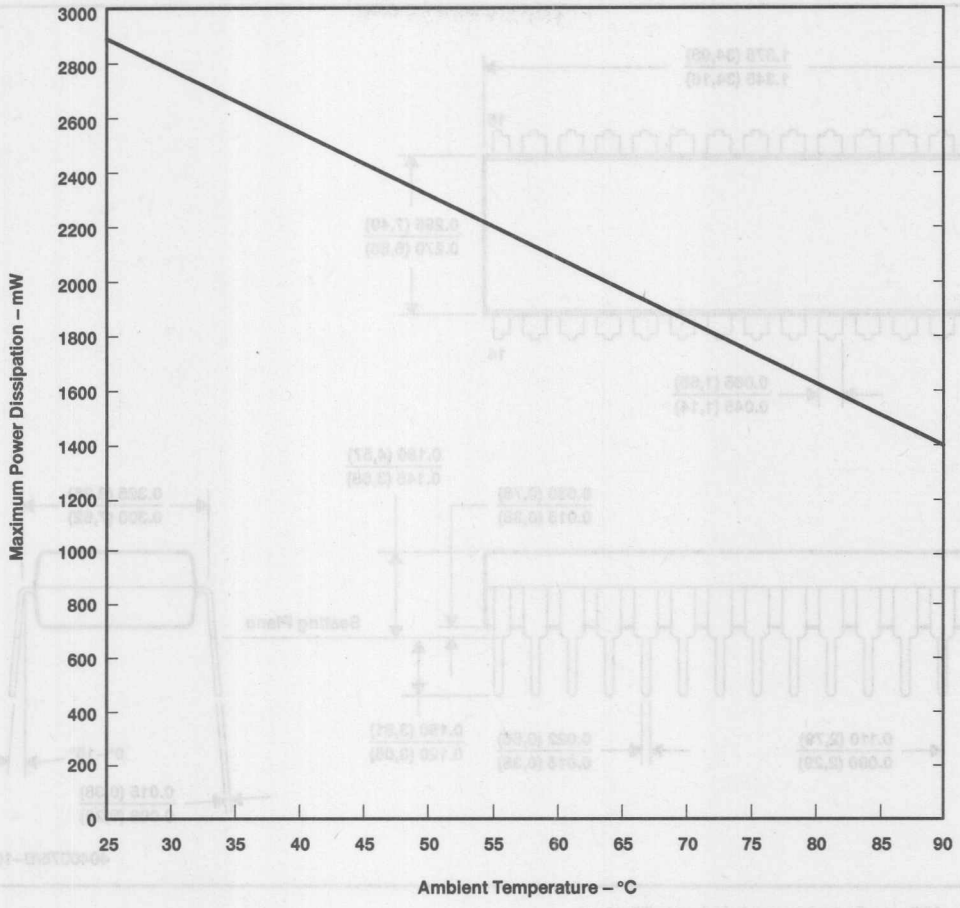


DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/B–10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

40-Pin DIP (N) Package Power Dissipation Derating in Still Air

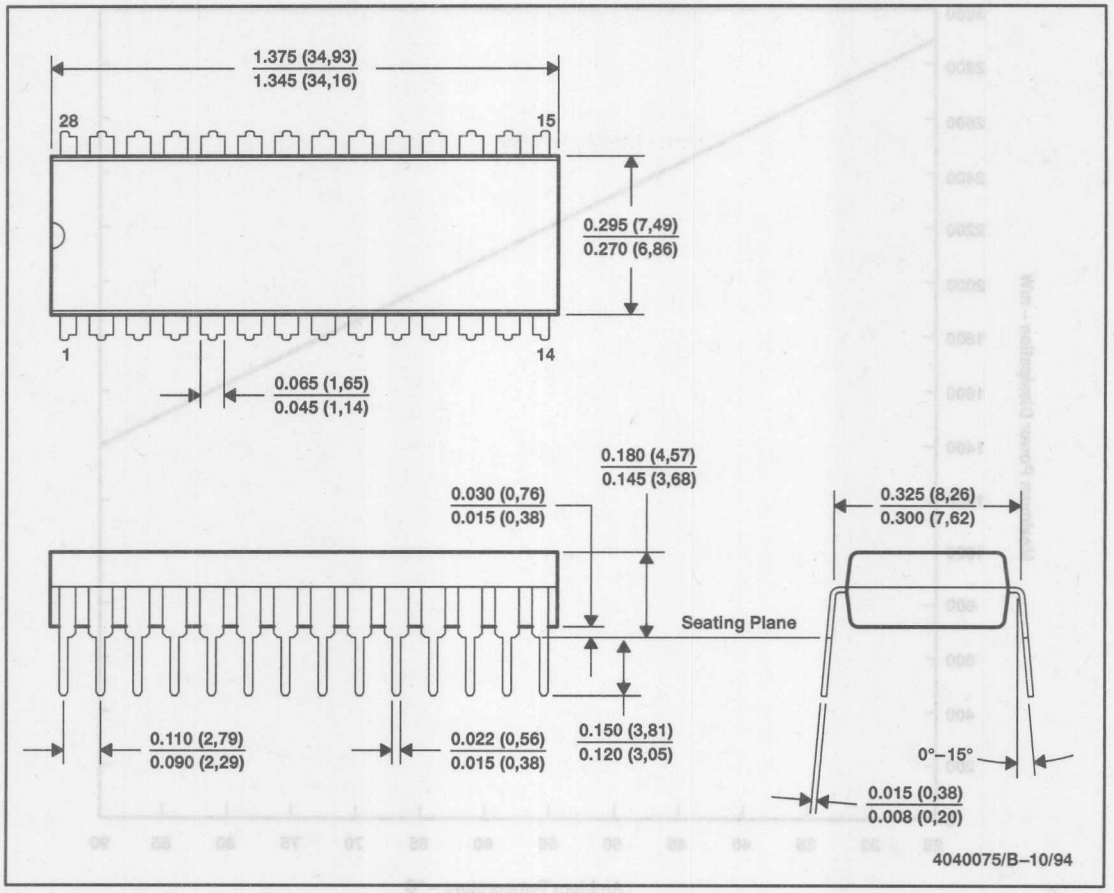


Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	43	N/A
0	Wind tunnel	–	N/A
100	Wind tunnel	–	N/A
250	Wind tunnel	–	N/A
500	Wind tunnel	–	N/A
N/A	N/A	N/A	12.5

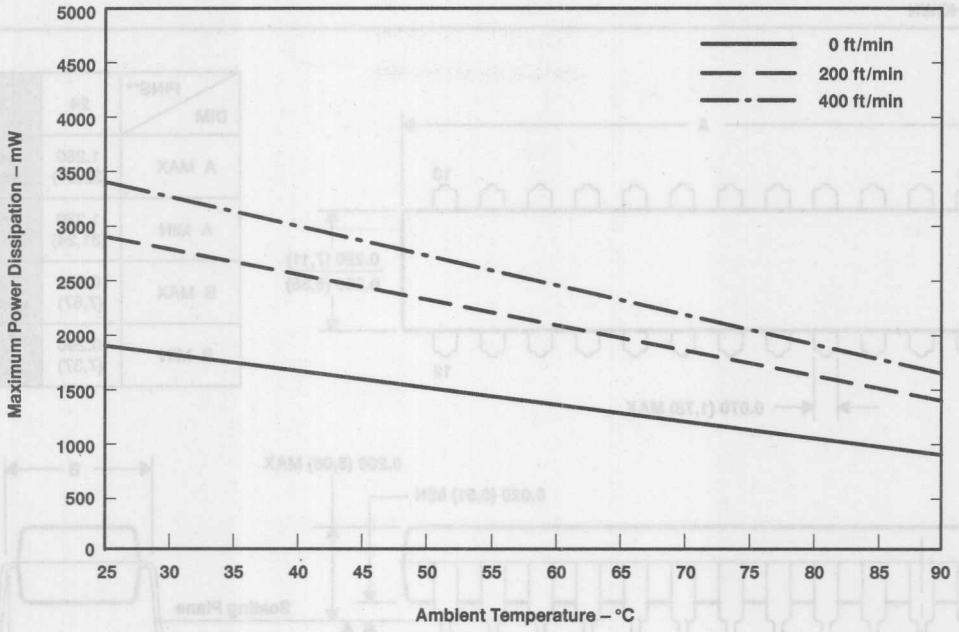
† Mounted on printed-circuit board

NP/R-PDIP-T28 **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimemsions do not include mold flash or protrusion.

28-Pin DIP (NP) Package Power Dissipation Derating at Varying Air Flows



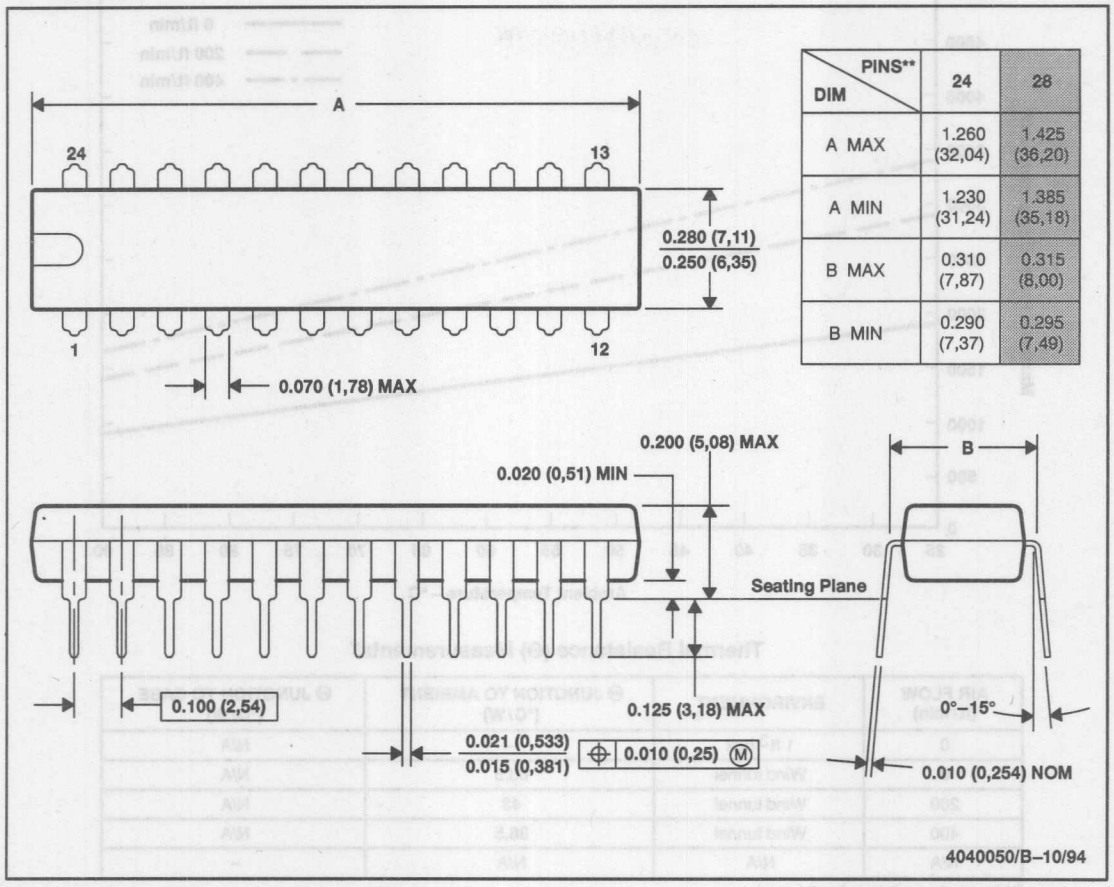
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	–	N/A
0	Wind tunnel	63.5	N/A
200	Wind tunnel	43	N/A
400	Wind tunnel	36.5	N/A
N/A	N/A	N/A	–

† Mounted on printed-circuit board

NT/R-PDIP-T** **PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN

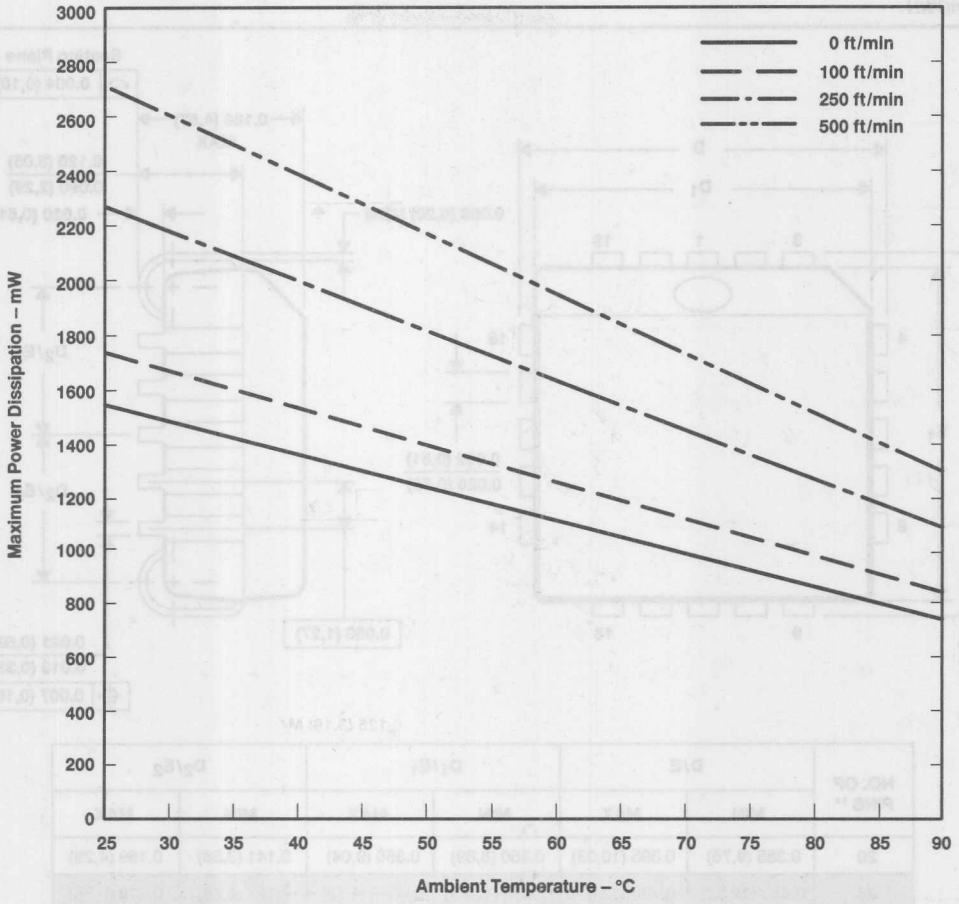


DIM \ PINS**	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

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28-Pin DIP (NT) Package Power Dissipation Derating at Varying Air Flows



Thermal Resistance (Θ) Measurements†

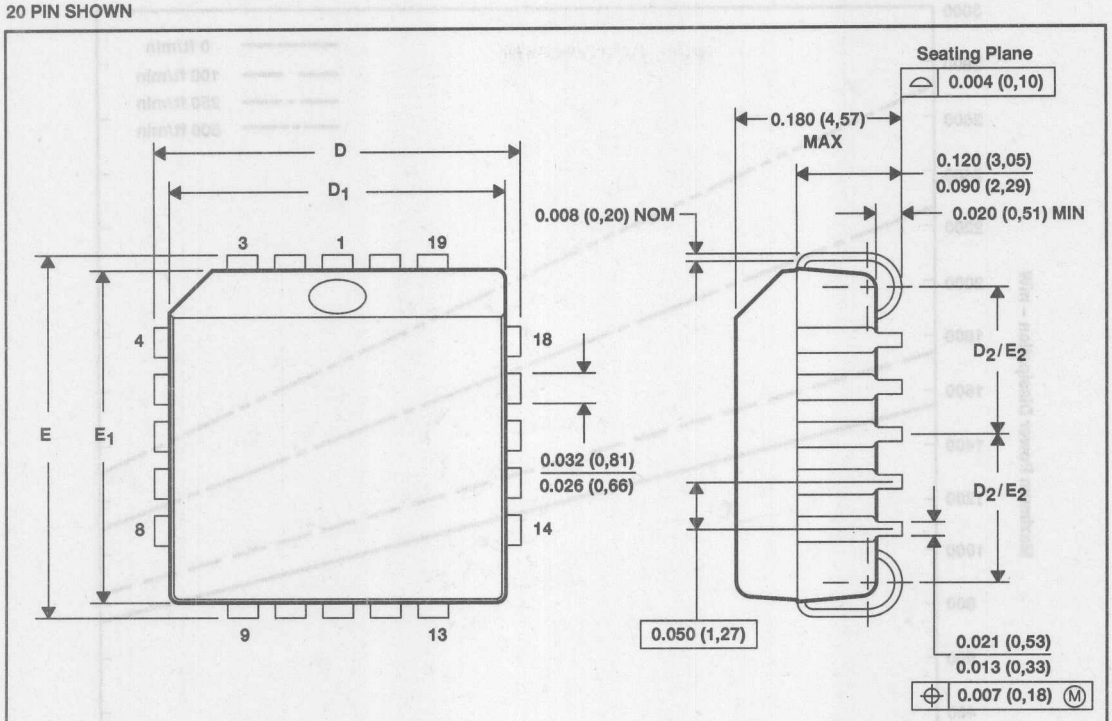
AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	67	N/A
0	Wind tunnel	81	N/A
100	Wind tunnel	72	N/A
250	Wind tunnel	55	N/A
500	Wind tunnel	46	N/A
N/A	N/A	N/A	25

† Mounted on printed-circuit board

FN/S-PQCC-J**

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN

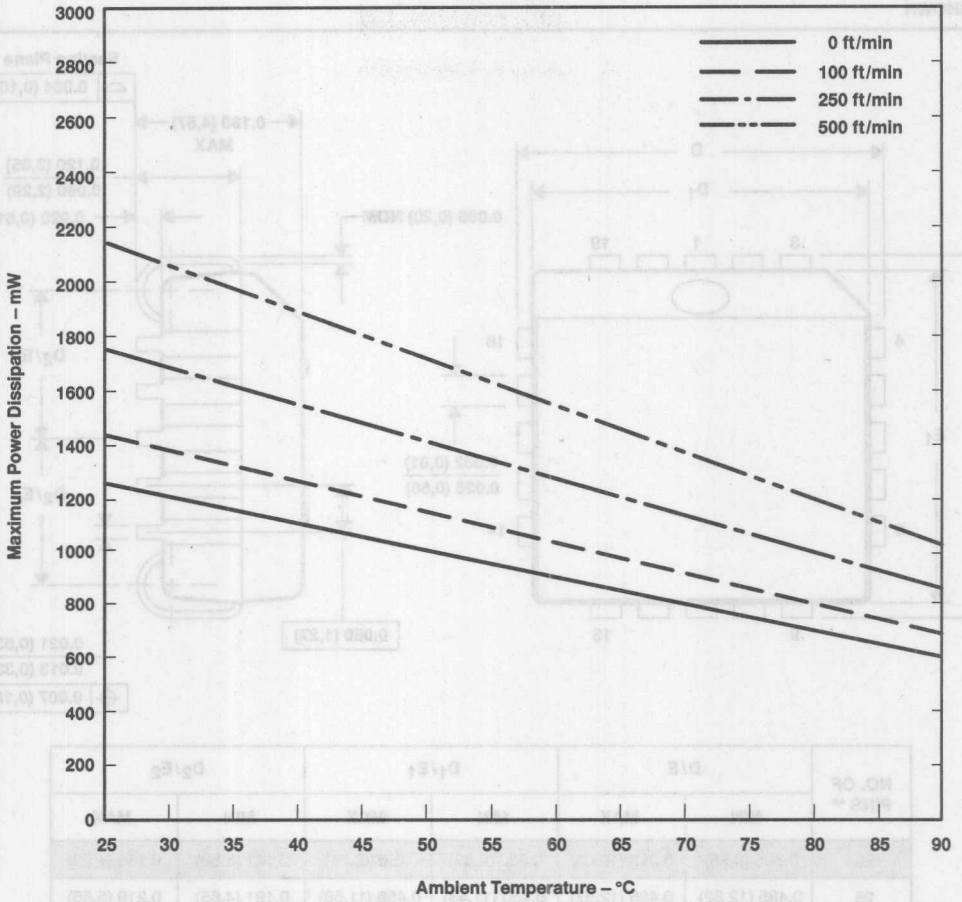


NO. OF PINS **	D/E		D_1/E_1		D_2/E_2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.956 (24,28)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B–10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

20-Pin PLCC (FN) Package Power Dissipation Derating at Varying Air Flows



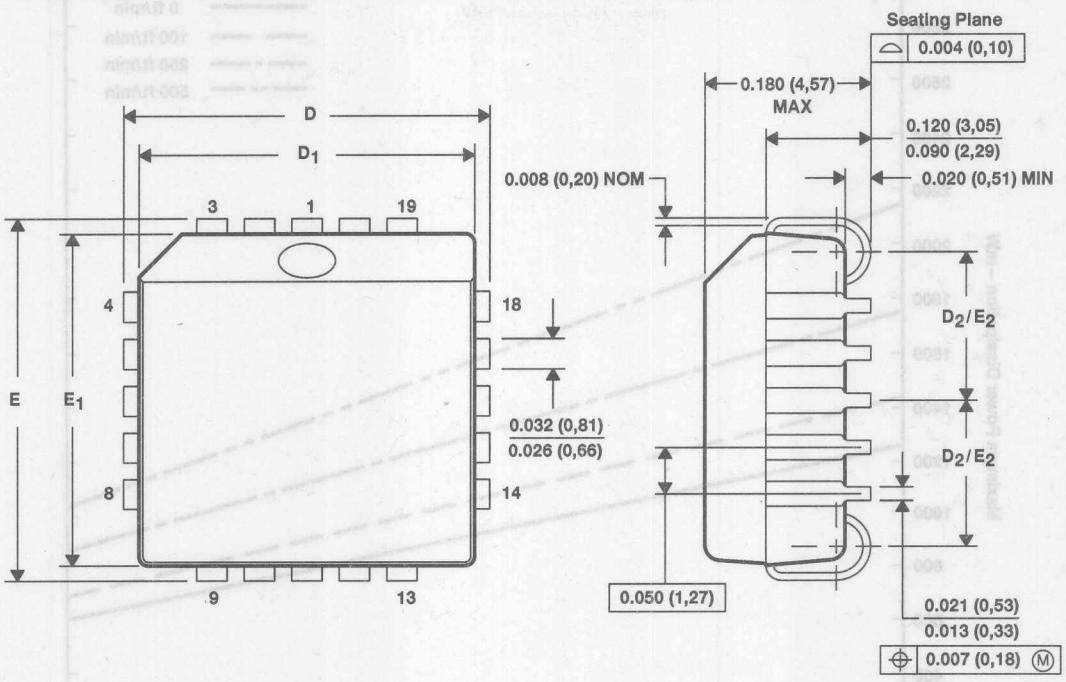
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	99	N/A
0	Wind tunnel	98.6	N/A
100	Wind tunnel	86.1	N/A
250	Wind tunnel	70.7	N/A
500	Wind tunnel	58.1	N/A
N/A	N/A	N/A	23

† Mounted on printed-circuit board

FN/S-PQCC-J** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN

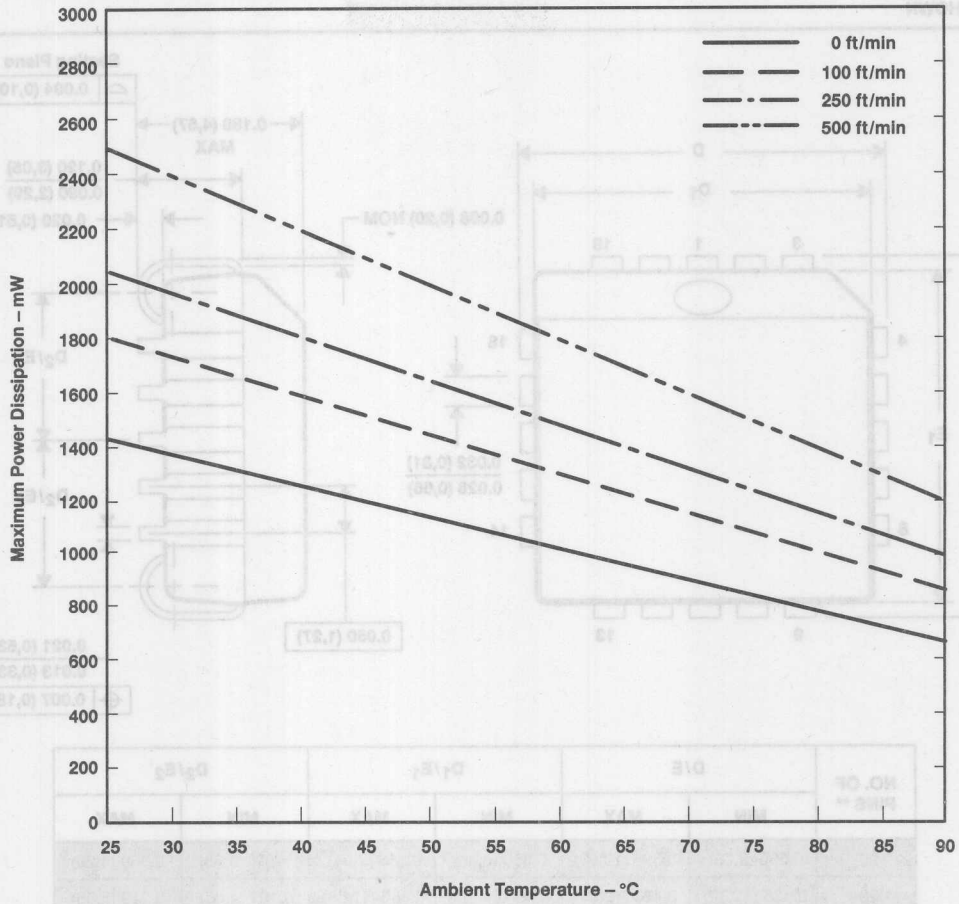


NO. OF PINS **	D/E		D_1/E_1		D_2/E_2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.956 (24,28)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B–10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

28-Pin PLCC (FN) Package Power Dissipation Derating at Varying Air Flows



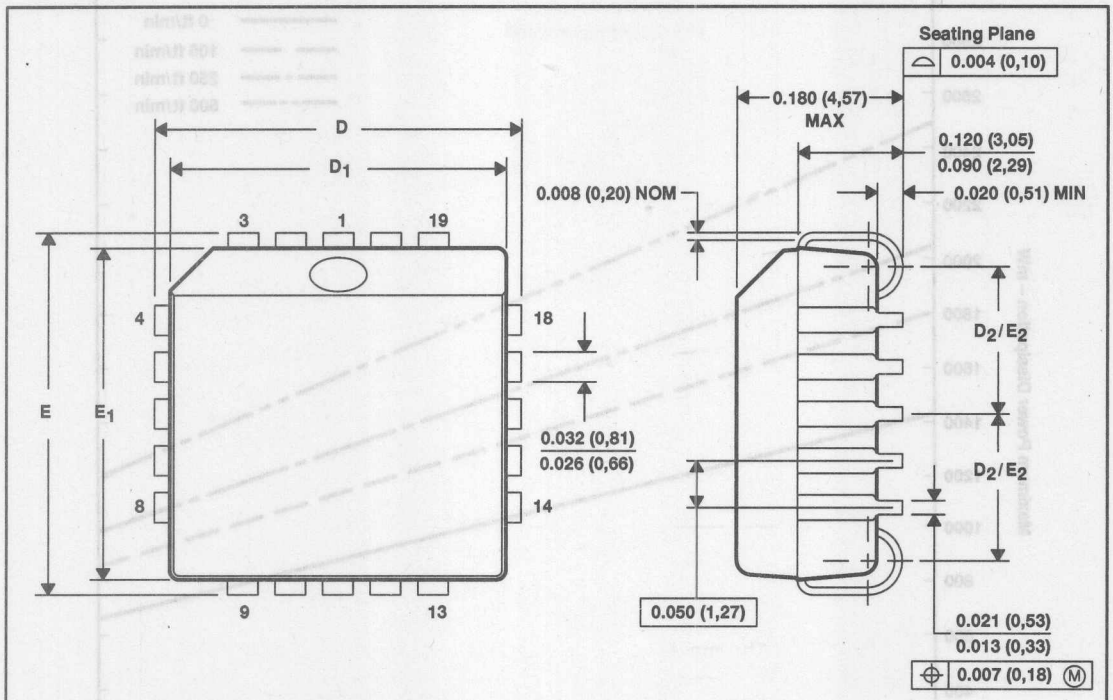
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	95.1	N/A
0	Wind tunnel	87.7	N/A
100	Wind tunnel	69.6	N/A
250	Wind tunnel	61	N/A
500	Wind tunnel	50	N/A
N/A	N/A	N/A	26.7

† Mounted on printed-circuit board

FN/S-PQCC-J** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN

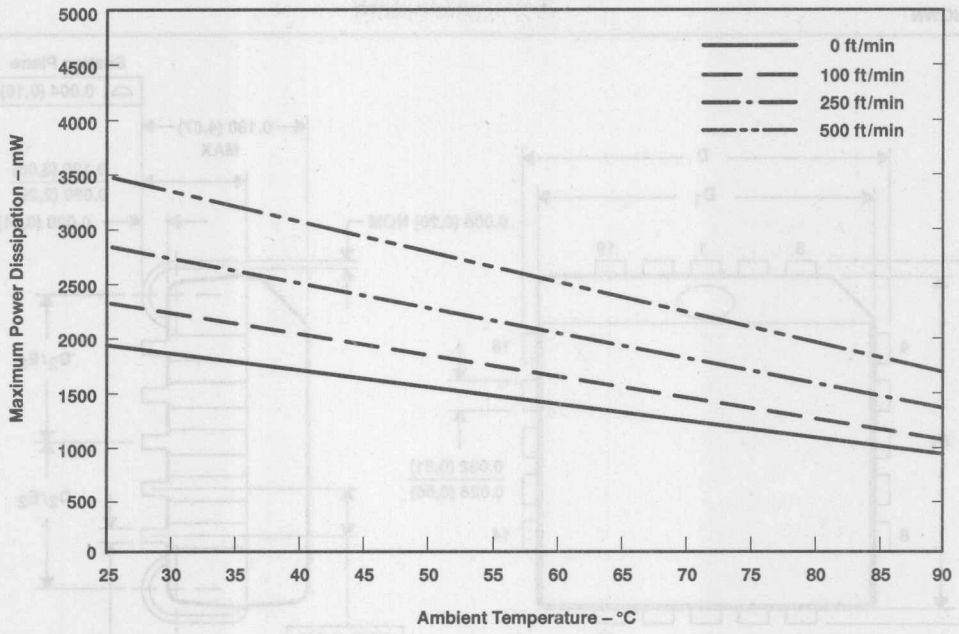


NO. OF PINS **	D/E		D_1/E_1		D_2/E_2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.956 (24,28)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B–10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

44-Pin PLCC (FN) Package Power Dissipation Derating at Varying Air Flows



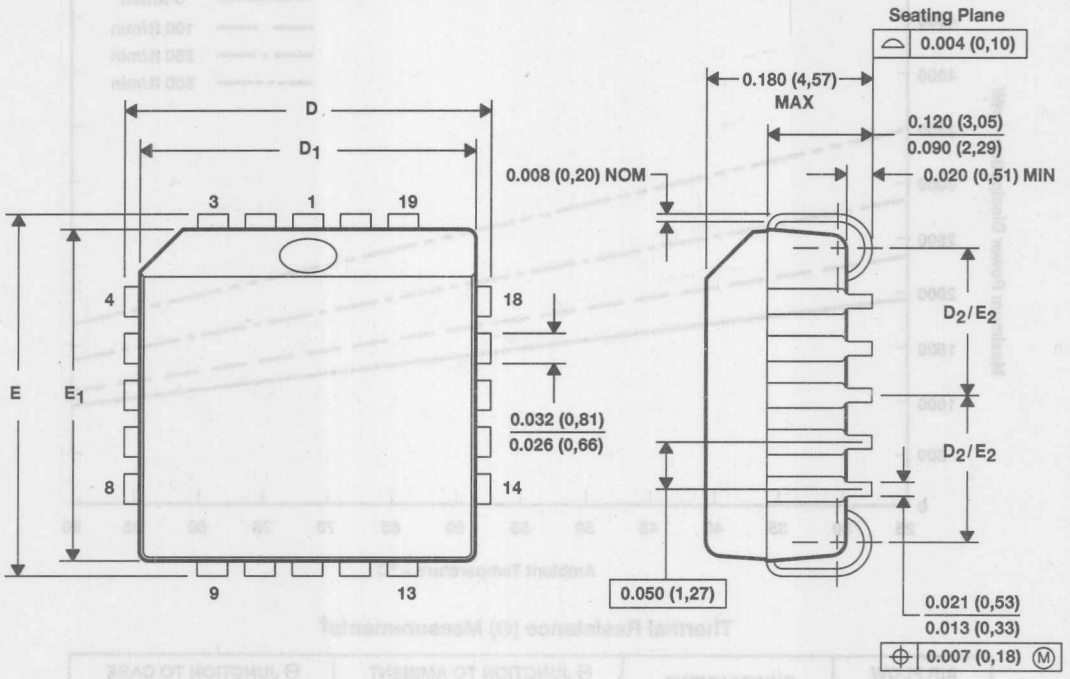
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	68.1	N/A
0	Wind tunnel	64.3	N/A
100	Wind tunnel	54.9	N/A
250	Wind tunnel	44.2	N/A
500	Wind tunnel	35.8	N/A
N/A	N/A	N/A	22

† Mounted on printed-circuit board

FN/S-PQCC-J** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN

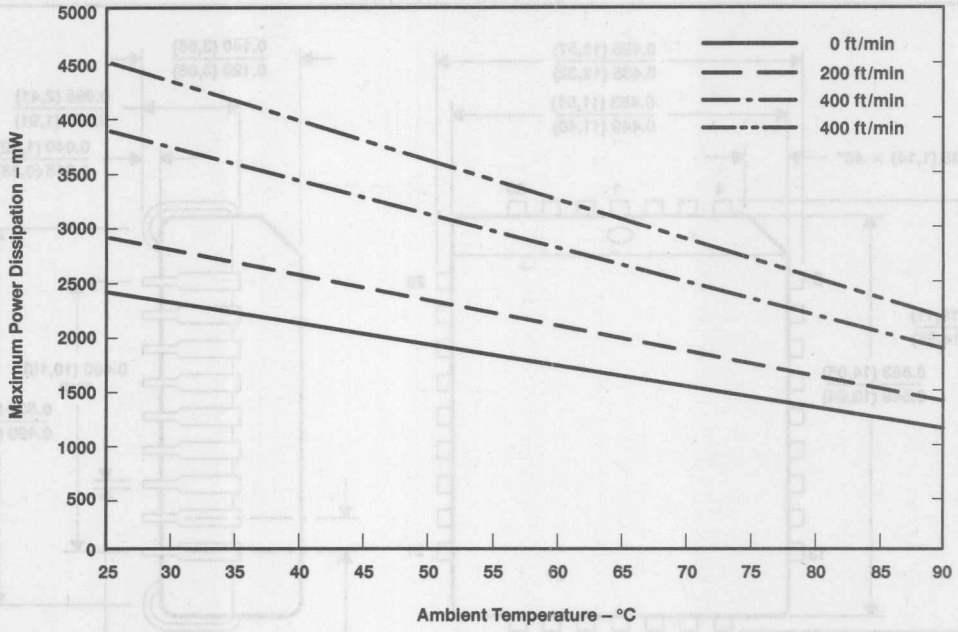


NO. OF PINS **	D/E		D_1/E_1		D_2/E_2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.956 (24,28)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B–10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

68-Pin PLCC (FN) Package Power Dissipation Derating at Varying Air Flows

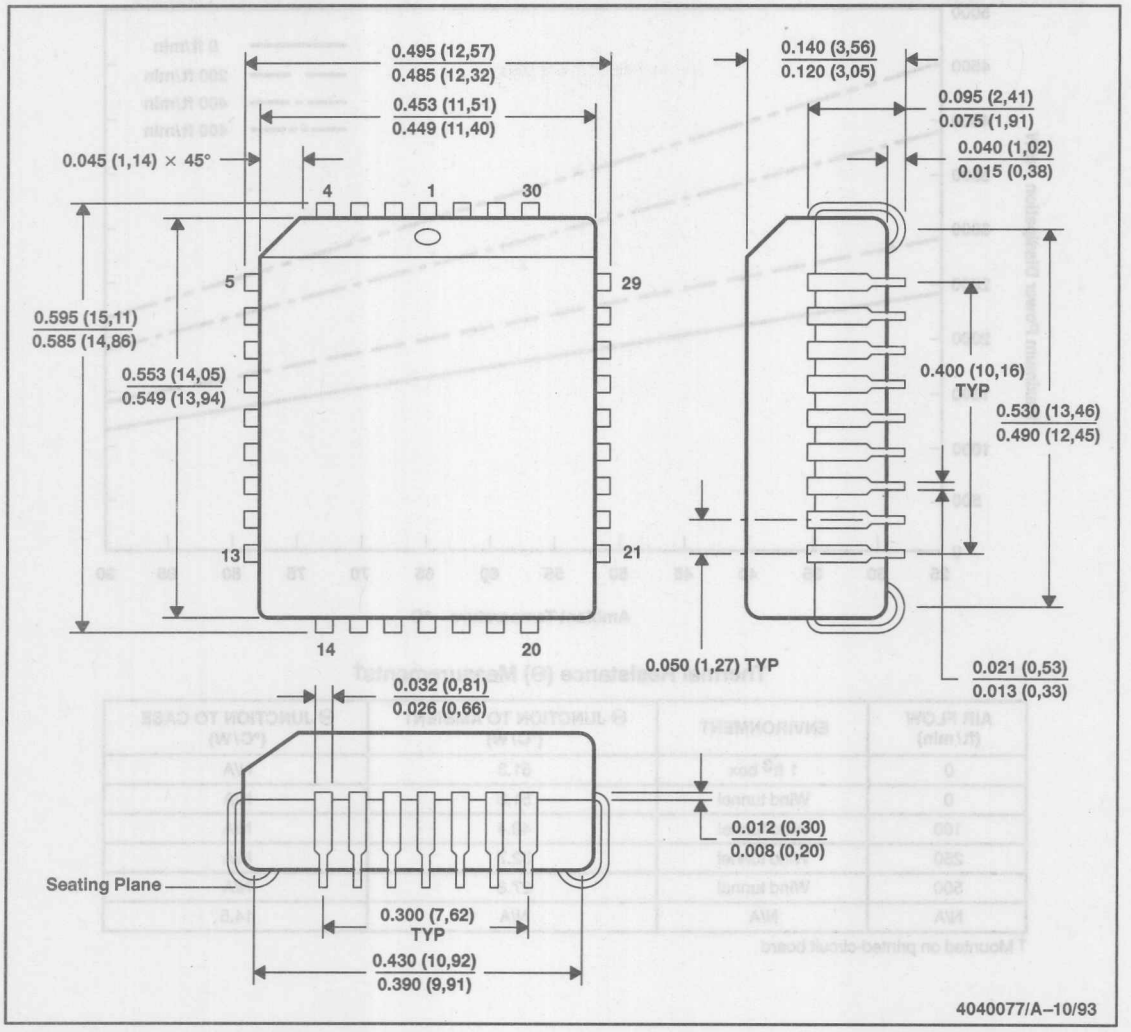


Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	51.3	N/A
0	Wind tunnel	51.3	N/A
100	Wind tunnel	43.4	N/A
250	Wind tunnel	32.7	N/A
500	Wind tunnel	27.8	N/A
N/A	N/A	N/A	14.5

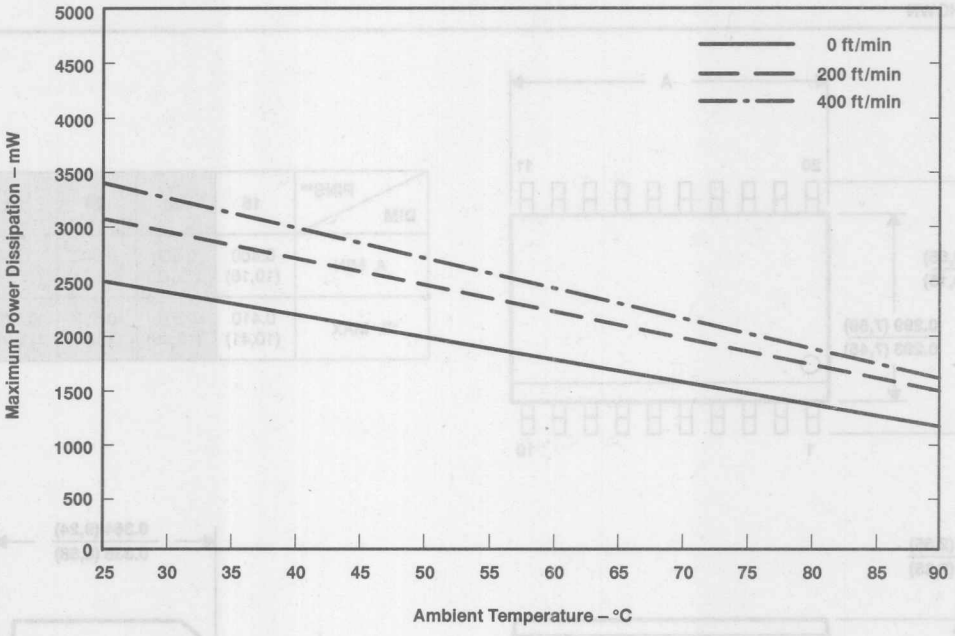
† Mounted on printed-circuit board

RJ/R-PQCC-J32 PLASTIC J-LEADED CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Formed leads shall be planar with respect to one another within 0.004 (0,10) at the seating plane.

32-Pin PQCC (RJ) Package Power Dissipation Derating at Varying Air Flows



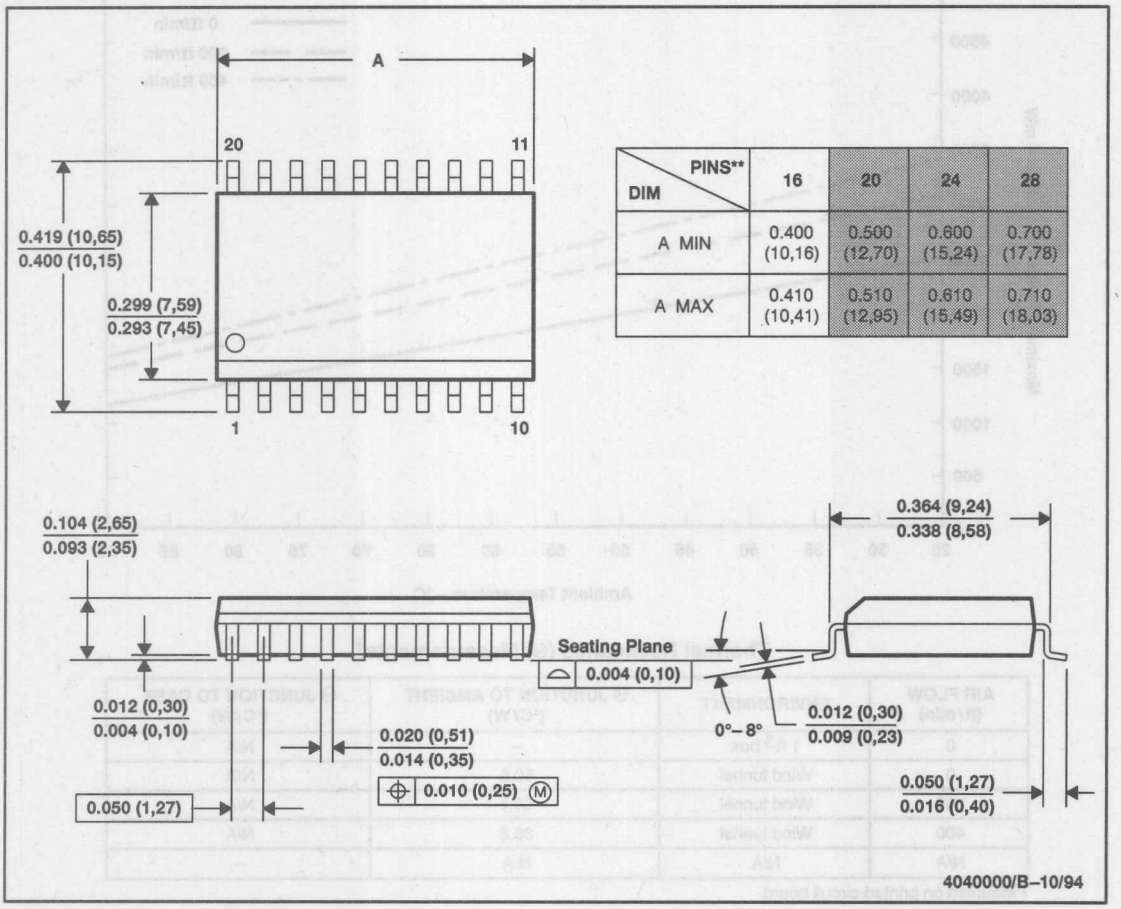
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	–	N/A
0	Wind tunnel	50.5	N/A
200	Wind tunnel	40.7	N/A
400	Wind tunnel	36.8	N/A
N/A	N/A	N/A	–

† Mounted on printed-circuit board

DW/R-PDSO-G** **PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE**

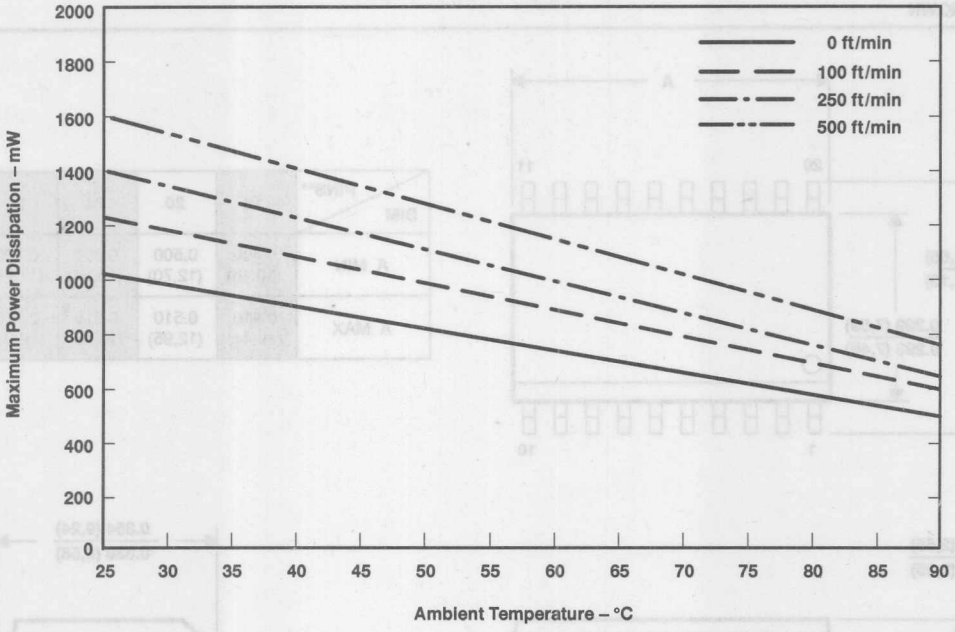
20 PIN SHOWN



DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

16-Pin SOIC (DW) Package Power Dissipation Derating at Varying Air Flows



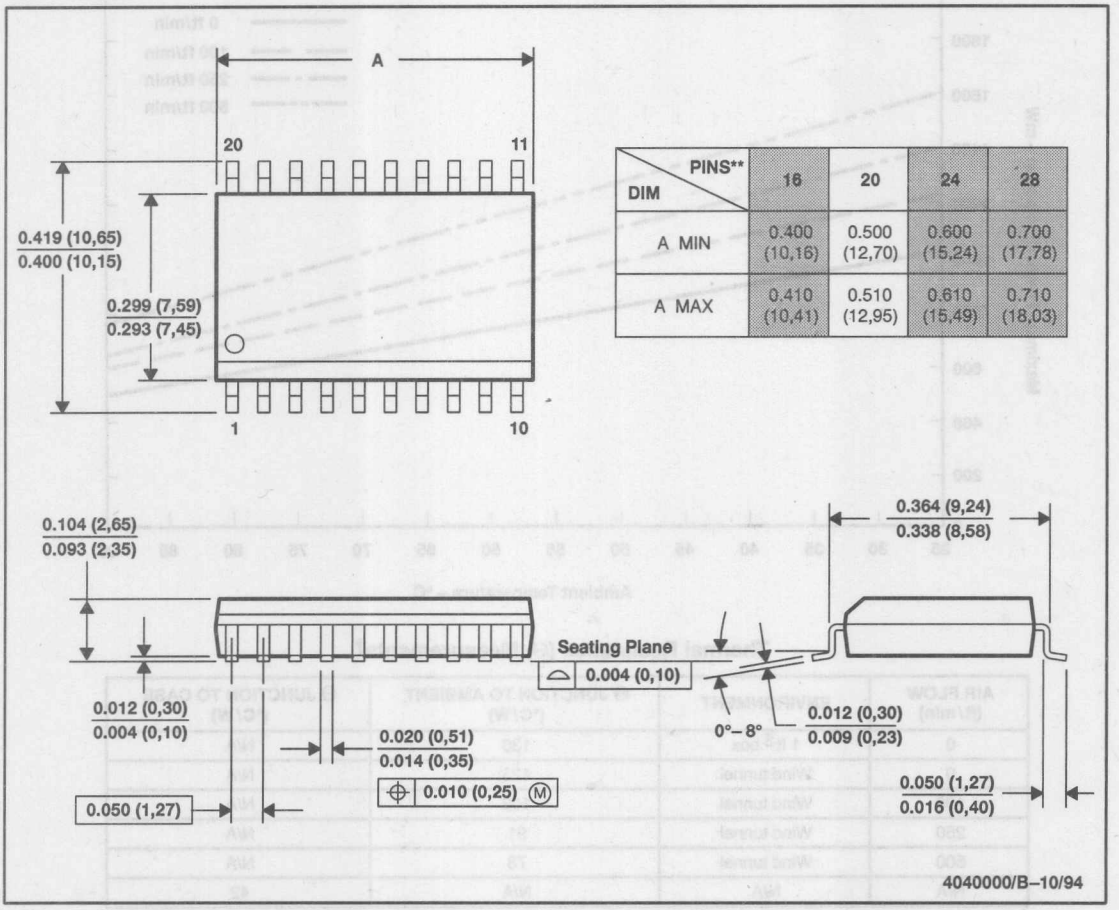
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	130	N/A
0	Wind tunnel	123	N/A
100	Wind tunnel	102	N/A
250	Wind tunnel	91	N/A
500	Wind tunnel	78	N/A
N/A	N/A	N/A	42

† Mounted on printed-circuit board

DW/R-PDSO-G** **PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE**

20 PIN SHOWN

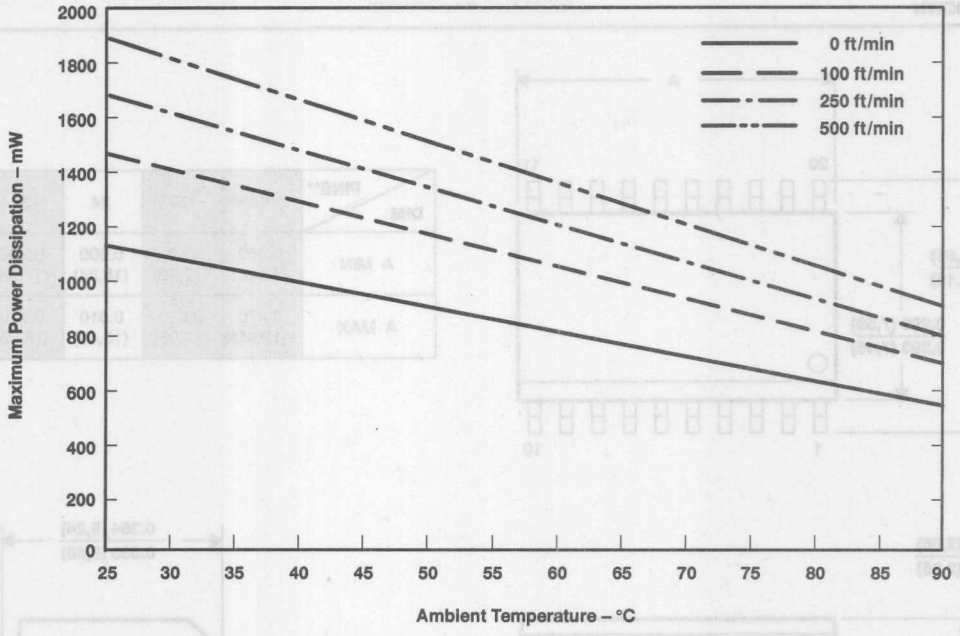


DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

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20-Pin SOIC (DW) Package Power Dissipation Derating at Varying Air Flows



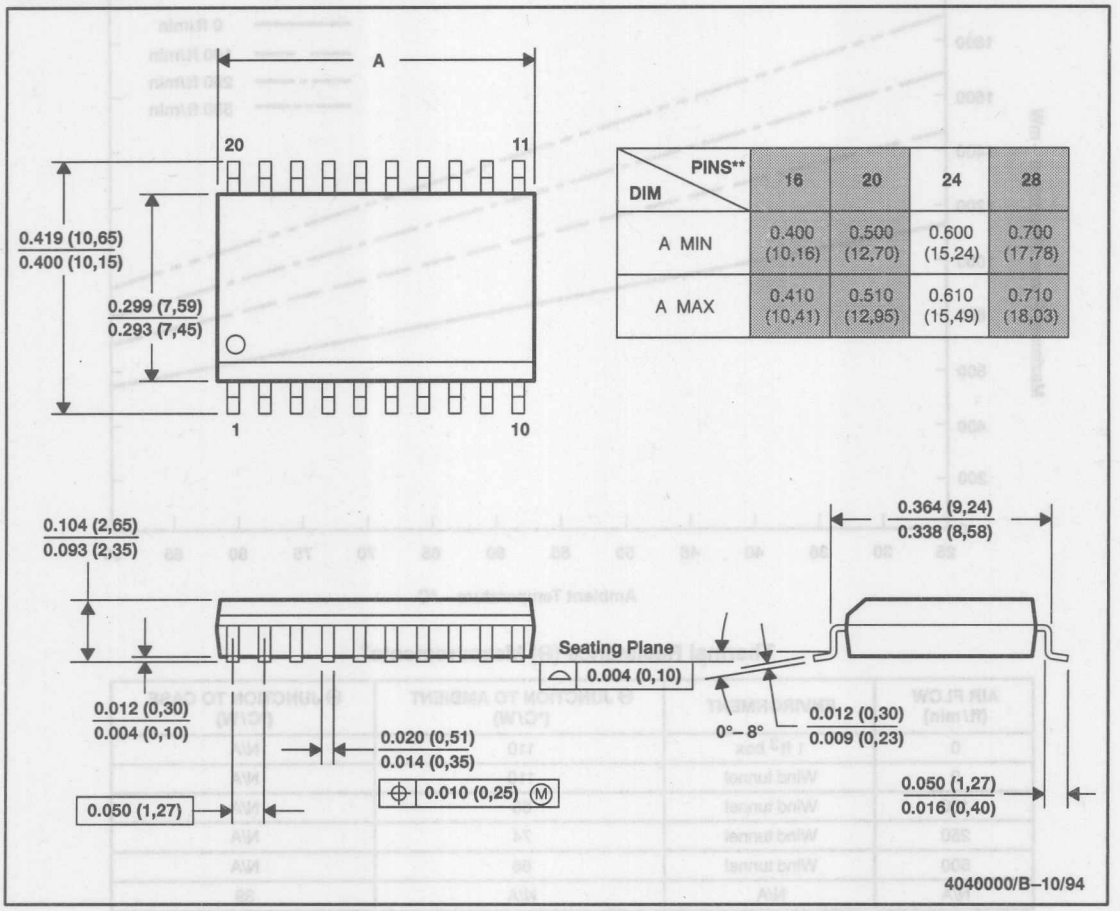
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	110	N/A
0	Wind tunnel	110	N/A
100	Wind tunnel	85	N/A
250	Wind tunnel	74	N/A
500	Wind tunnel	66	N/A
N/A	N/A	N/A	39

† Mounted on printed-circuit board

DW/R-PDSO-G** **PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE**

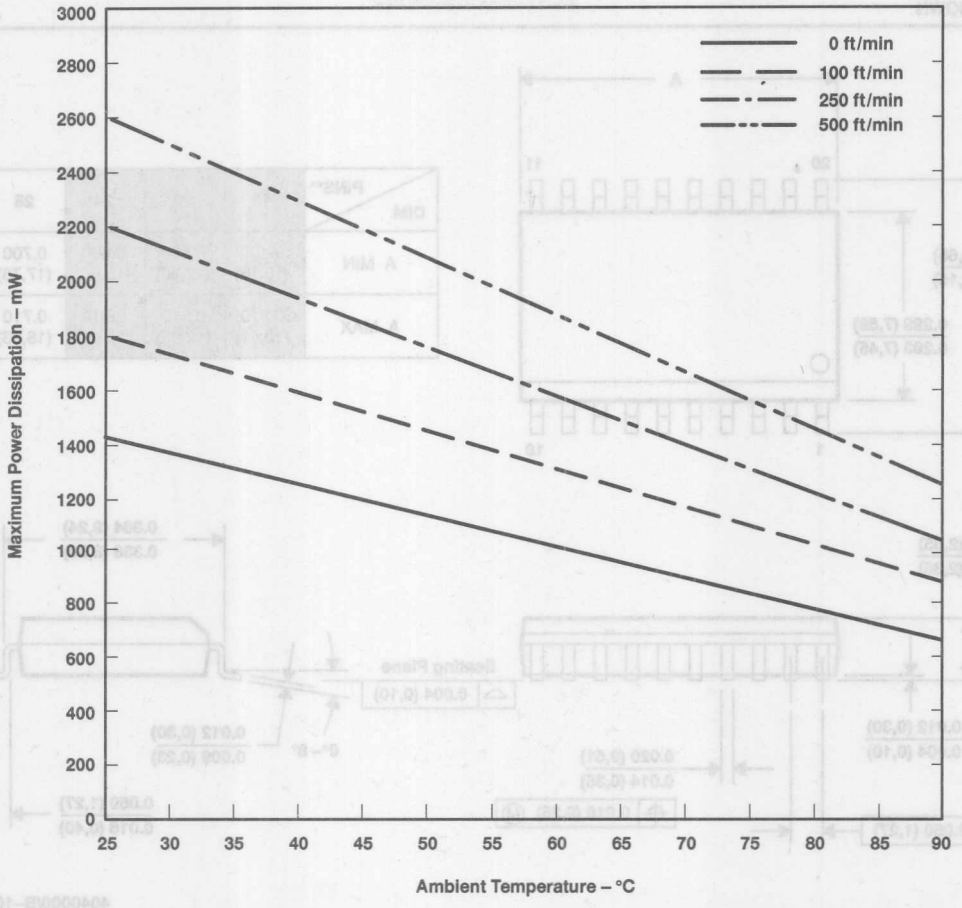
20 PIN SHOWN



DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

24-Pin SOIC (DW) Package Power Dissipation Derating at Varying Air Flows



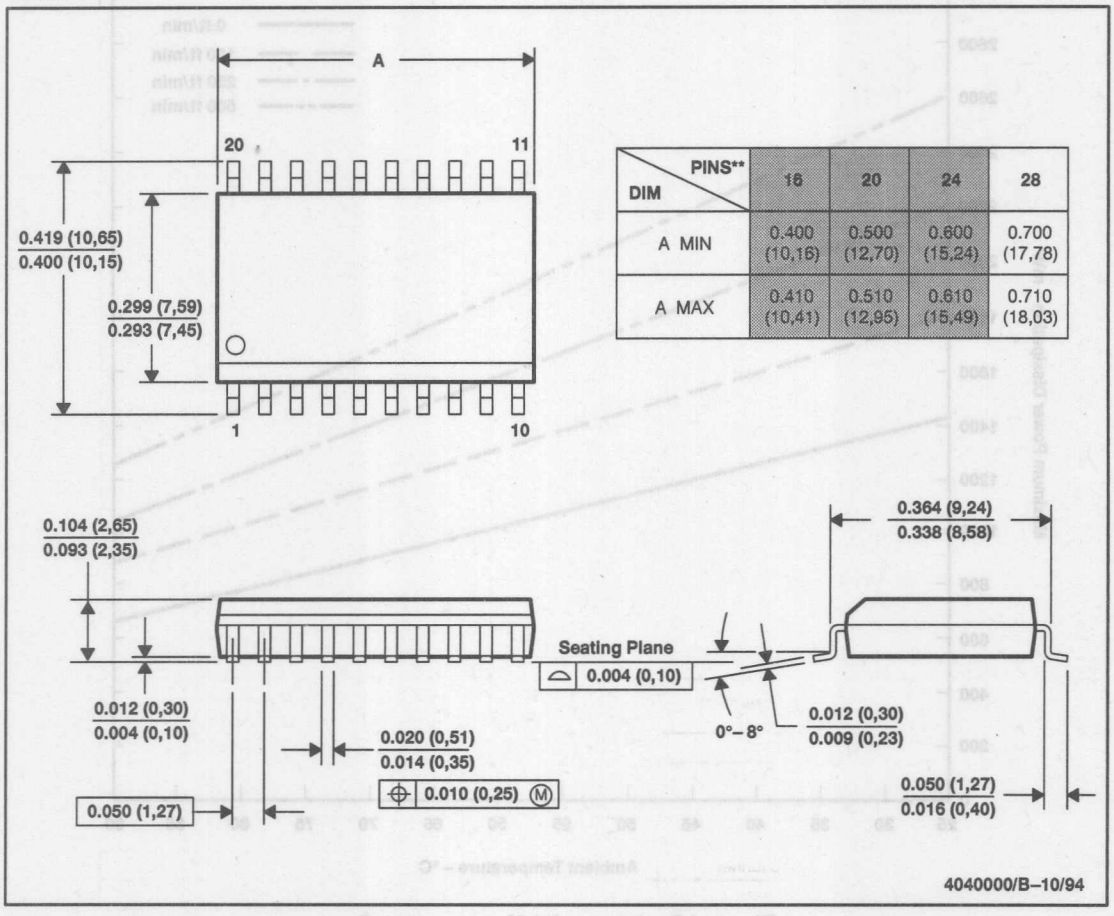
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	92	N/A
0	Wind tunnel	88	N/A
100	Wind tunnel	69	N/A
250	Wind tunnel	57	N/A
500	Wind tunnel	48	N/A
N/A	N/A	N/A	25

† Mounted on printed-circuit board

DW/R-PDSO-G** **PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE**

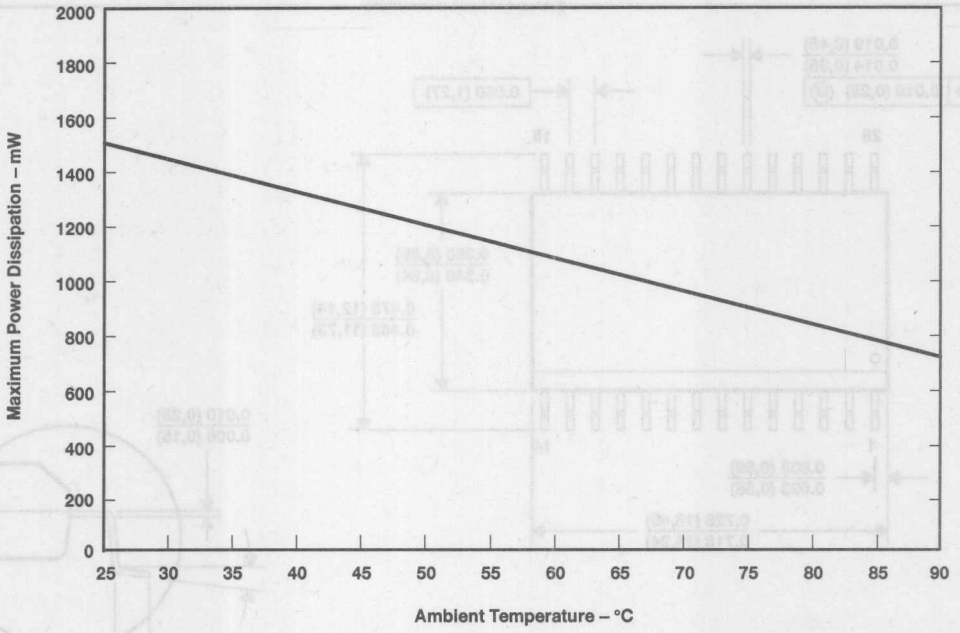
20 PIN SHOWN



DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

28-Pin SOIC (DW) Package Power Dissipation Derating in Still Air

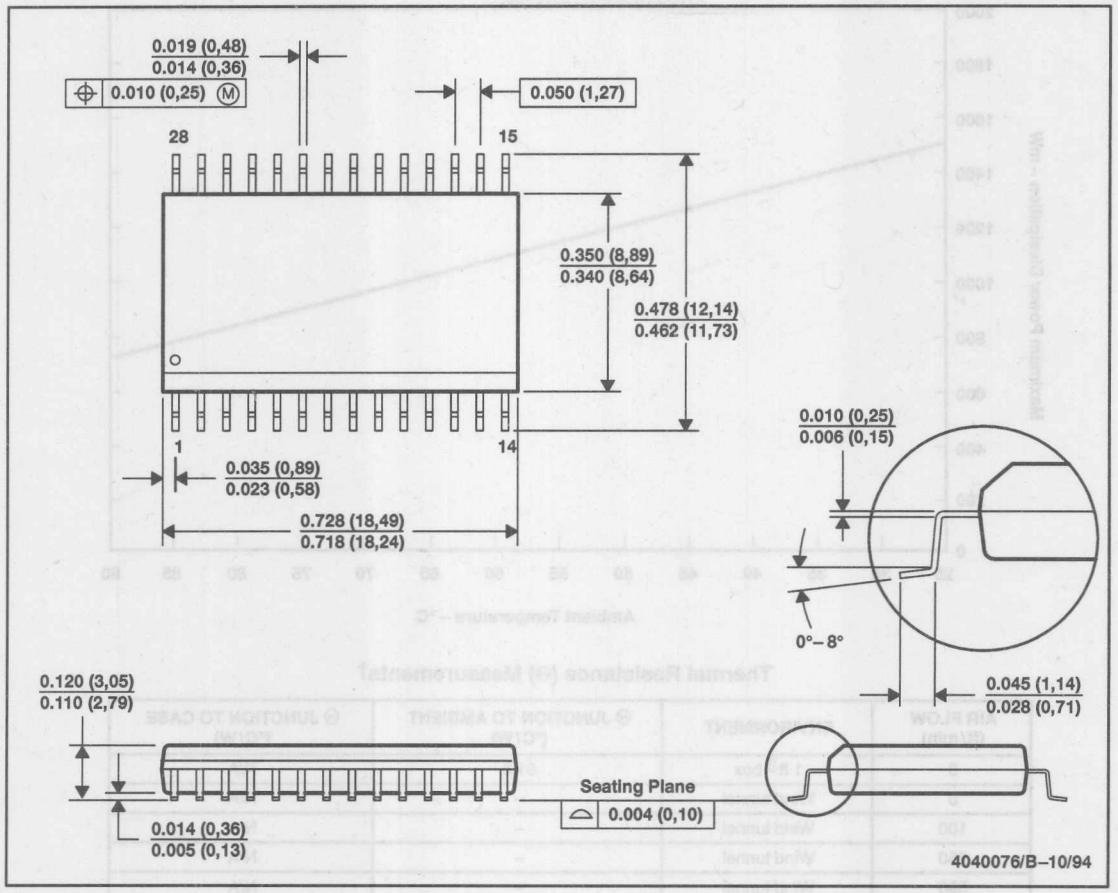


Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	81.8	N/A
0	Wind tunnel	–	N/A
100	Wind tunnel	–	N/A
250	Wind tunnel	–	N/A
500	Wind tunnel	–	N/A
N/A	N/A	N/A	15.4

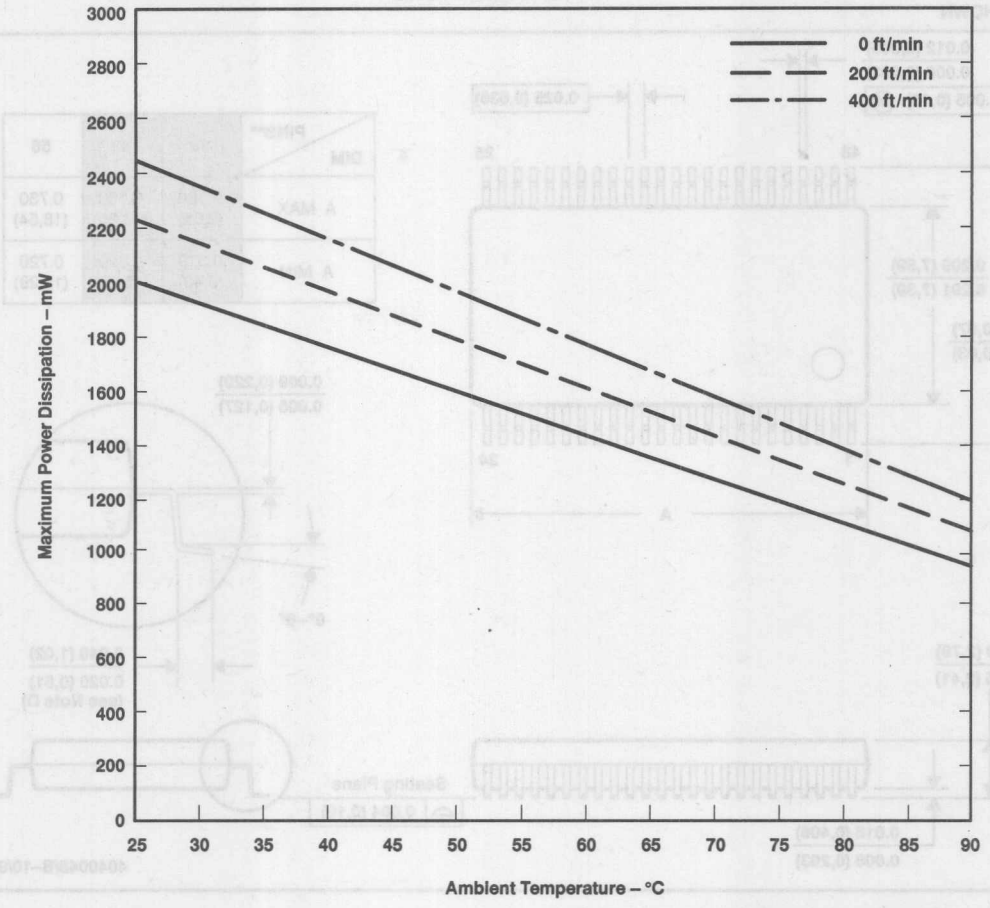
† Mounted on printed-circuit board

DV/R-PDSO-G28 **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

28-Pin SOIC (DV) Package Power Dissipation Derating at Varying Air Flows



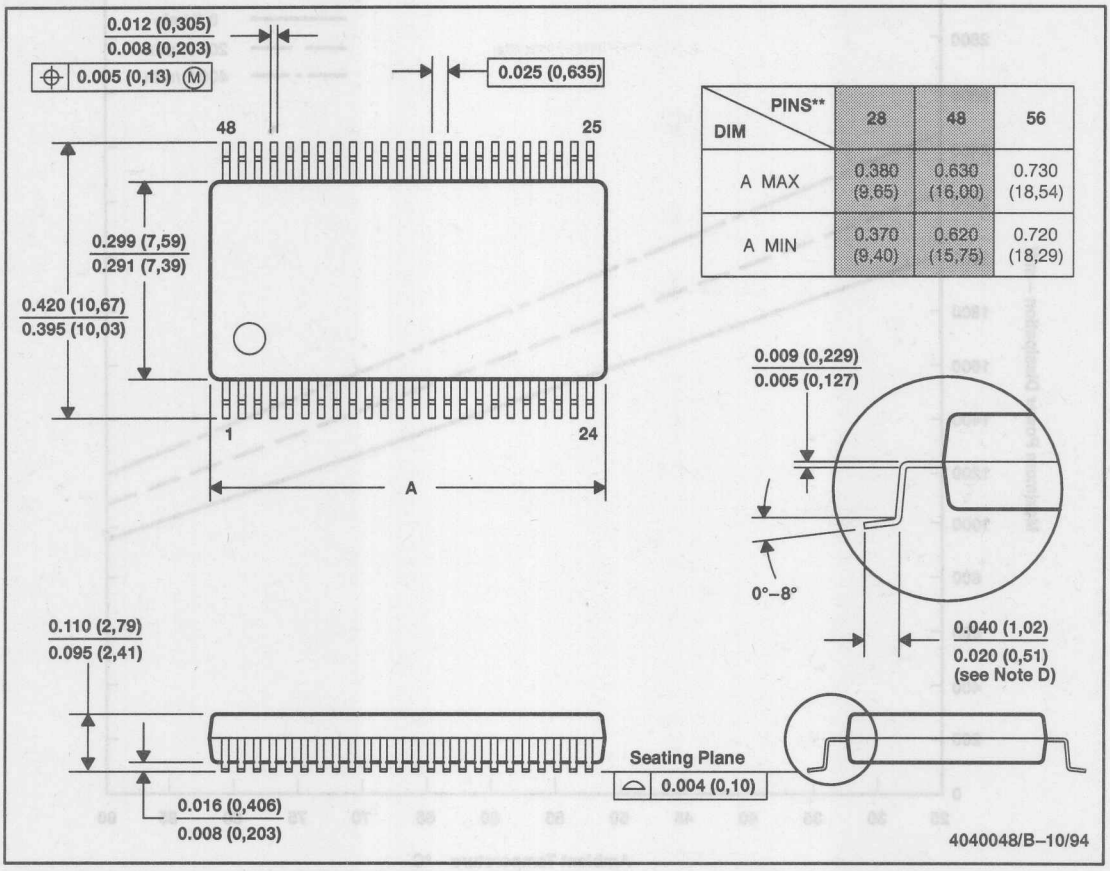
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	–	N/A
0	Wind tunnel	63	N/A
200	Wind tunnel	56	N/A
400	Wind tunnel	51	N/A
N/A	N/A	N/A	–

† Mounted on printed-circuit board

DL/R-PDSO-G** **PLASTIC SHRINK SMALL-OUTLINE PACKAGE**

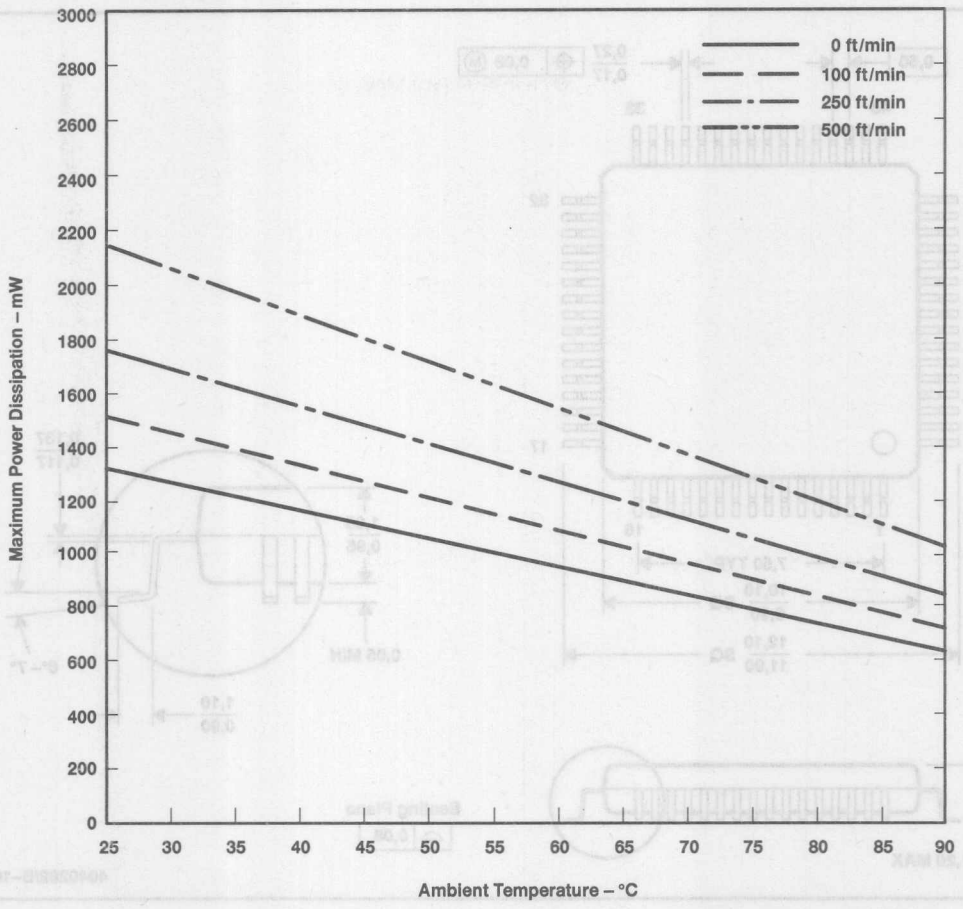
48 PIN SHOWN



DIM \ PINS**	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Foot length is measured from lead top to point 0.010 (0.254) above seating plane.

56-Pin SSOP (DL) Package Power Dissipation Derating at Varying Air Flows

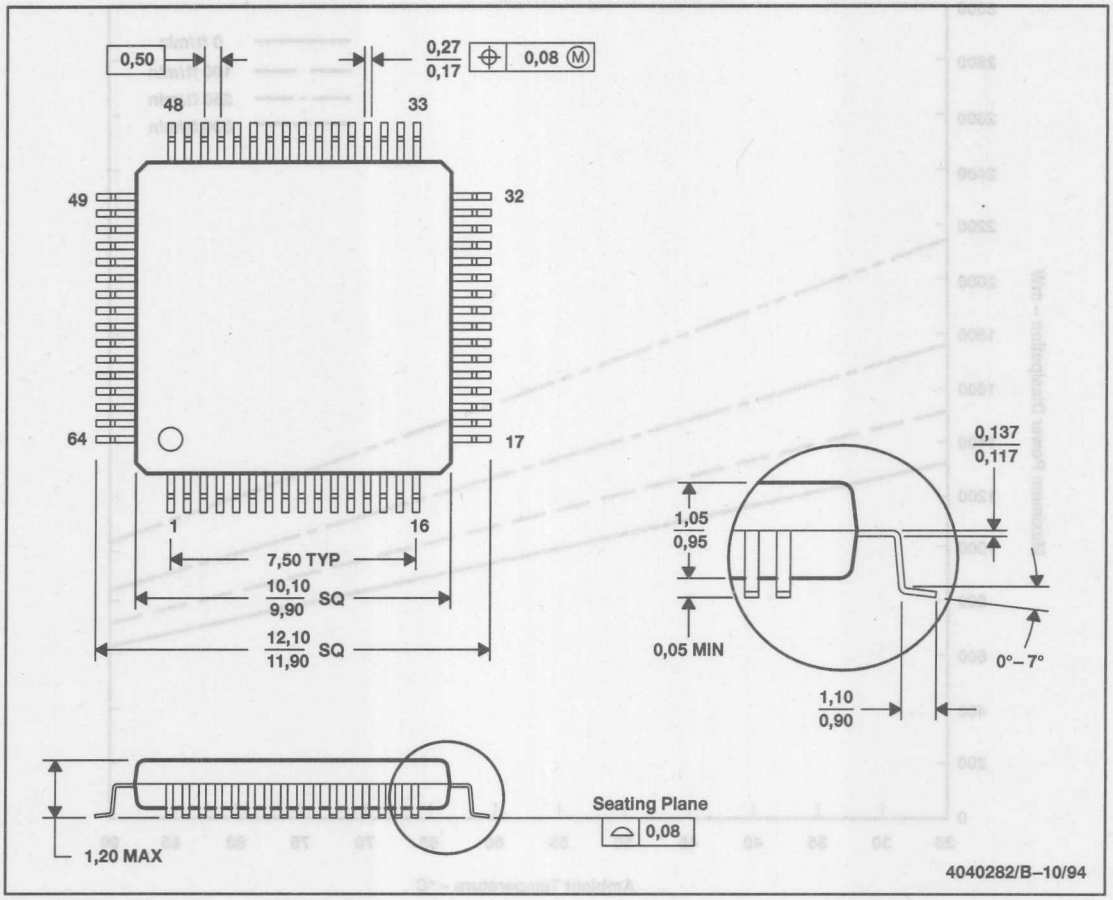


Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	94	N/A
0	Wind tunnel	94	N/A
100	Wind tunnel	82	N/A
250	Wind tunnel	70	N/A
500	Wind tunnel	58	N/A
N/A	N/A	N/A	22

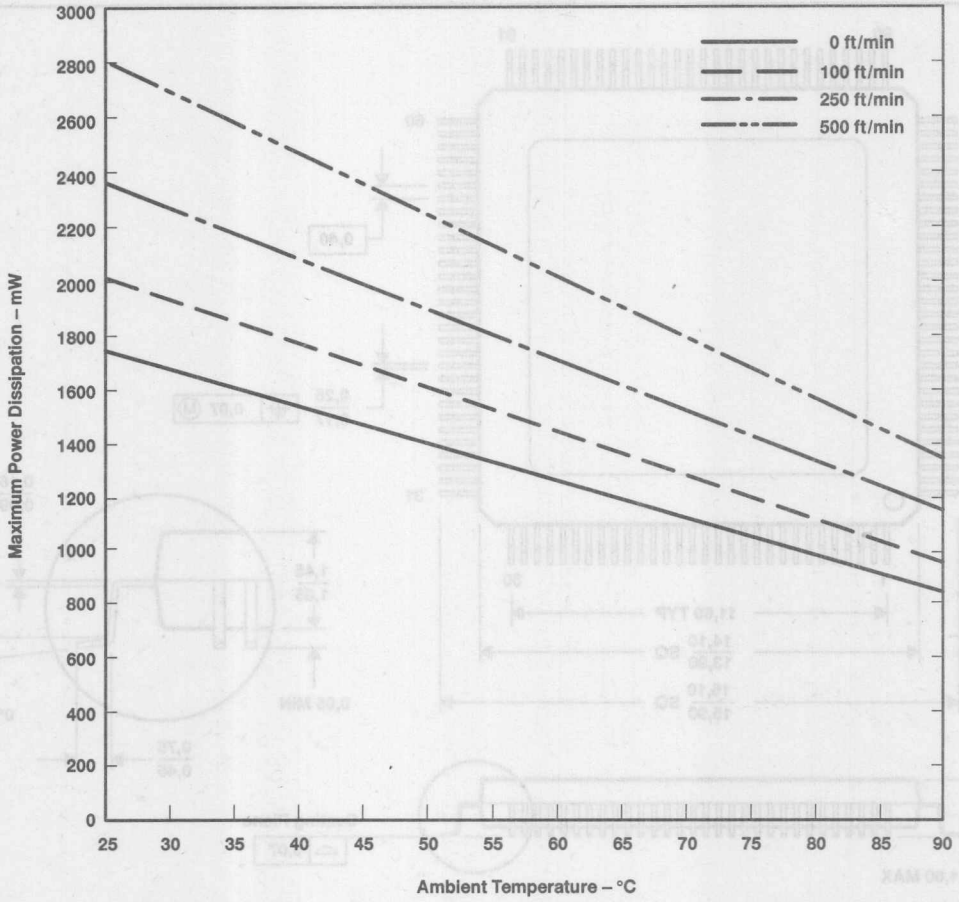
† Mounted on printed-circuit board

PAG/S-PQFP-G64 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

64-Pin TQFP (PAG) Package Power Dissipation Derating at Varying Air Flows

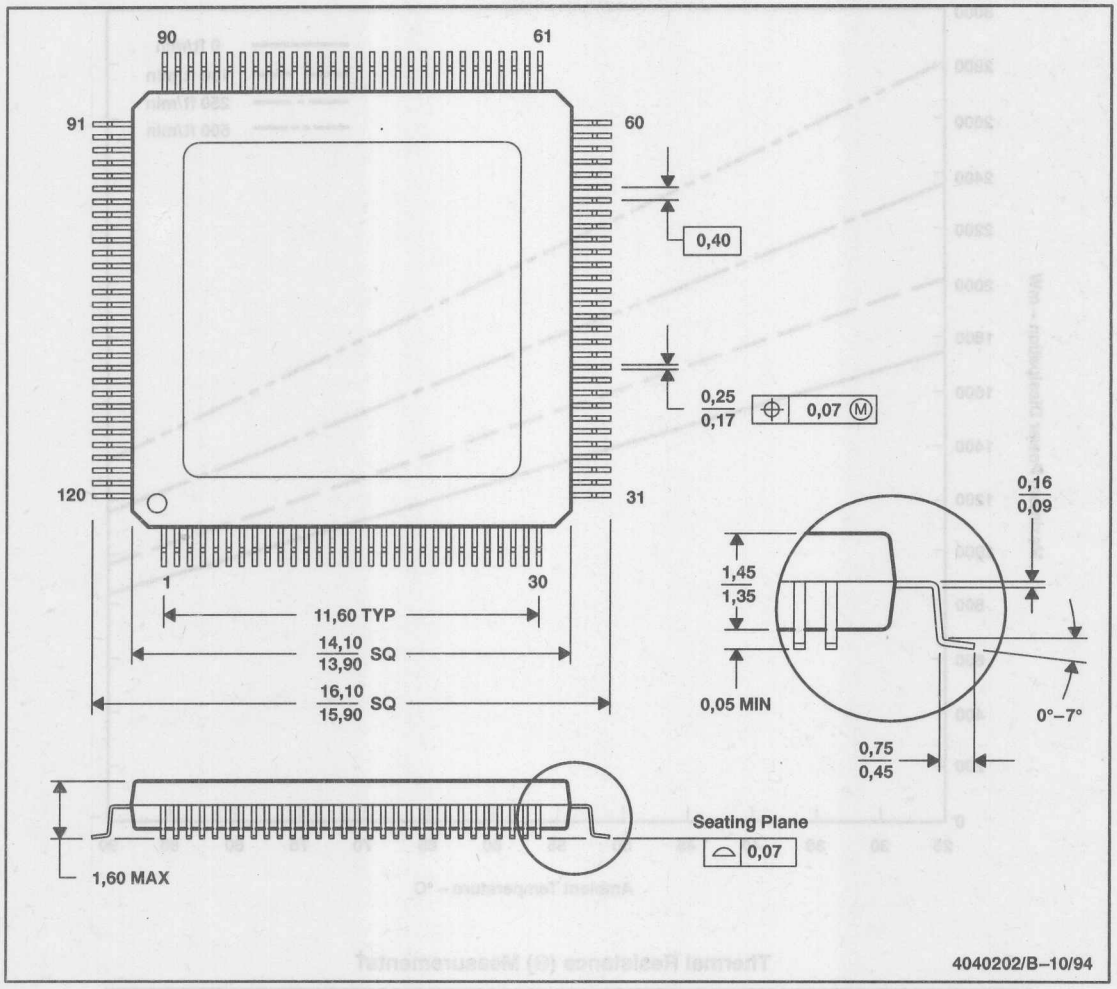


Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	75.7	N/A
0	Wind tunnel	71.3	N/A
100	Wind tunnel	61.9	N/A
250	Wind tunnel	52.6	N/A
500	Wind tunnel	44.6	N/A
N/A	N/A	N/A	15.1

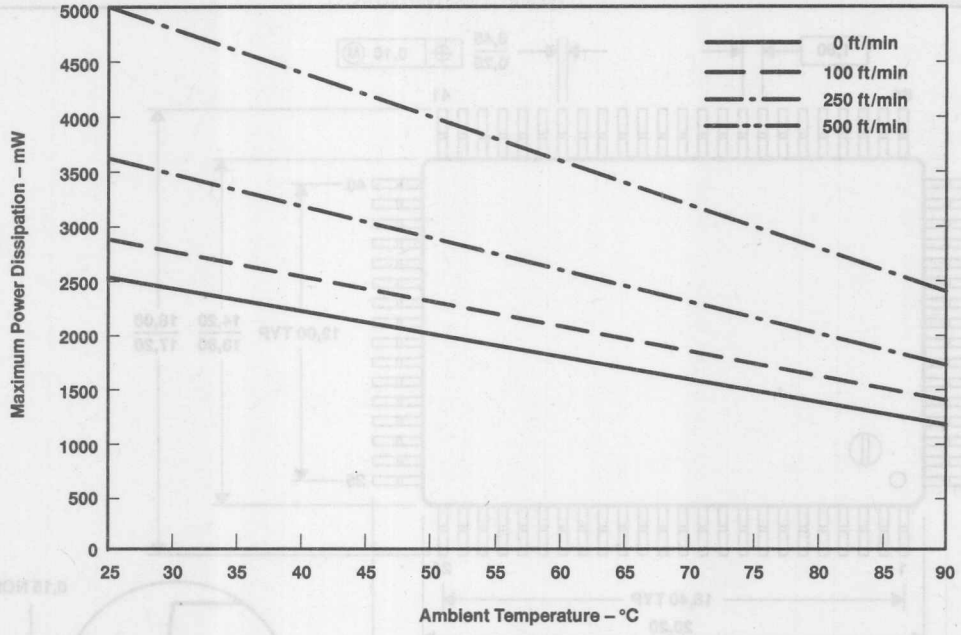
† Mounted on printed-circuit board

PCB/S-PQFP-G120 PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Allowable protrusion is 0,25mm maximum per side.
D. Thermally enhanced molded plastic package (HSP).

120-Pin TQFP (PCB)† Package Power Dissipation Derating at Varying Air Flows

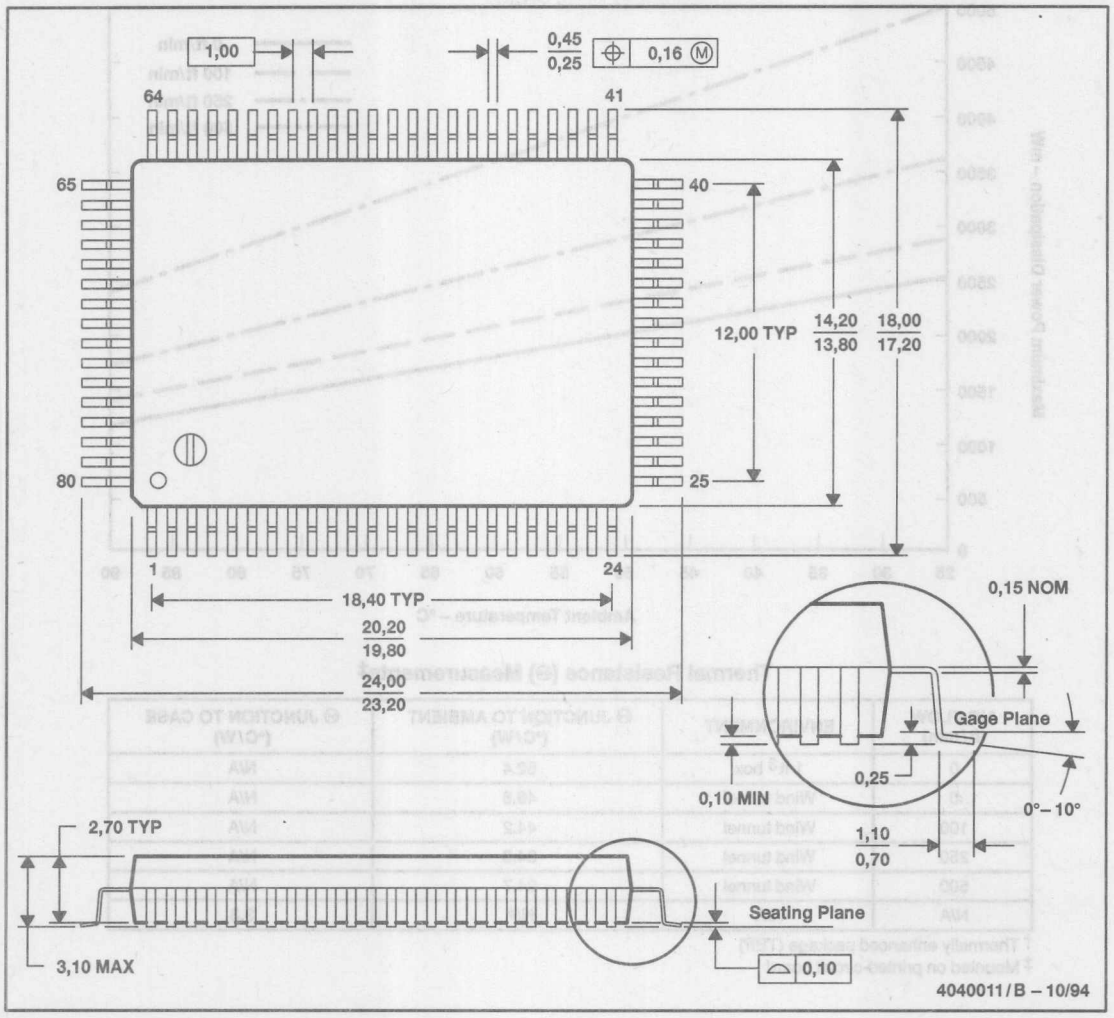


Thermal Resistance (Θ) Measurements‡

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	52.4	N/A
0	Wind tunnel	49.8	N/A
100	Wind tunnel	44.2	N/A
250	Wind tunnel	34.3	N/A
500	Wind tunnel	24.7	N/A
N/A	N/A	N/A	3.3

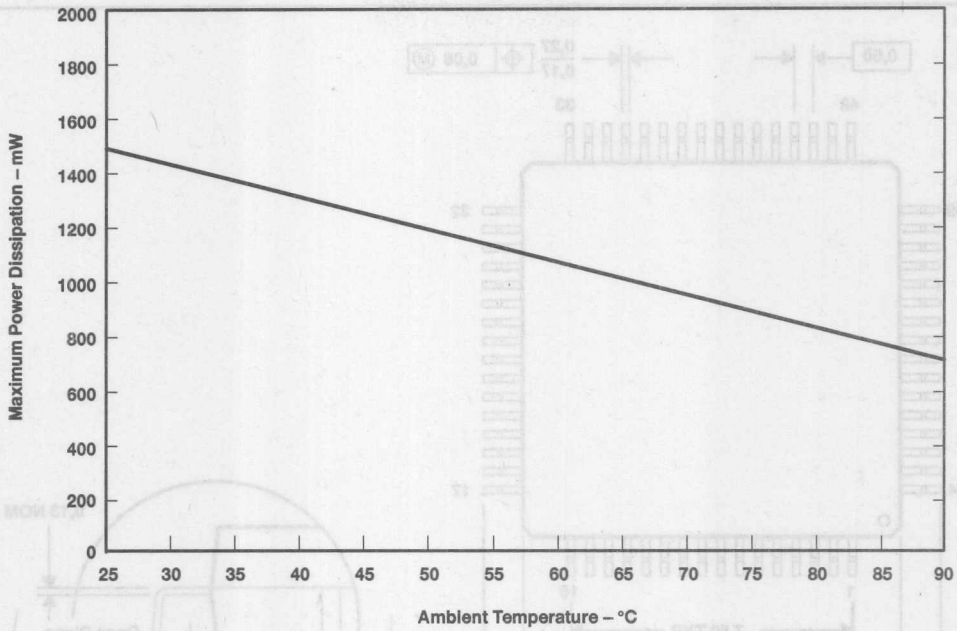
† Thermally enhanced package (TEP)
‡ Mounted on printed-circuit board

PH/R-PQFP-G80 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

80-Pin PQFP (PH) Package Power Dissipation Derating in Still Air

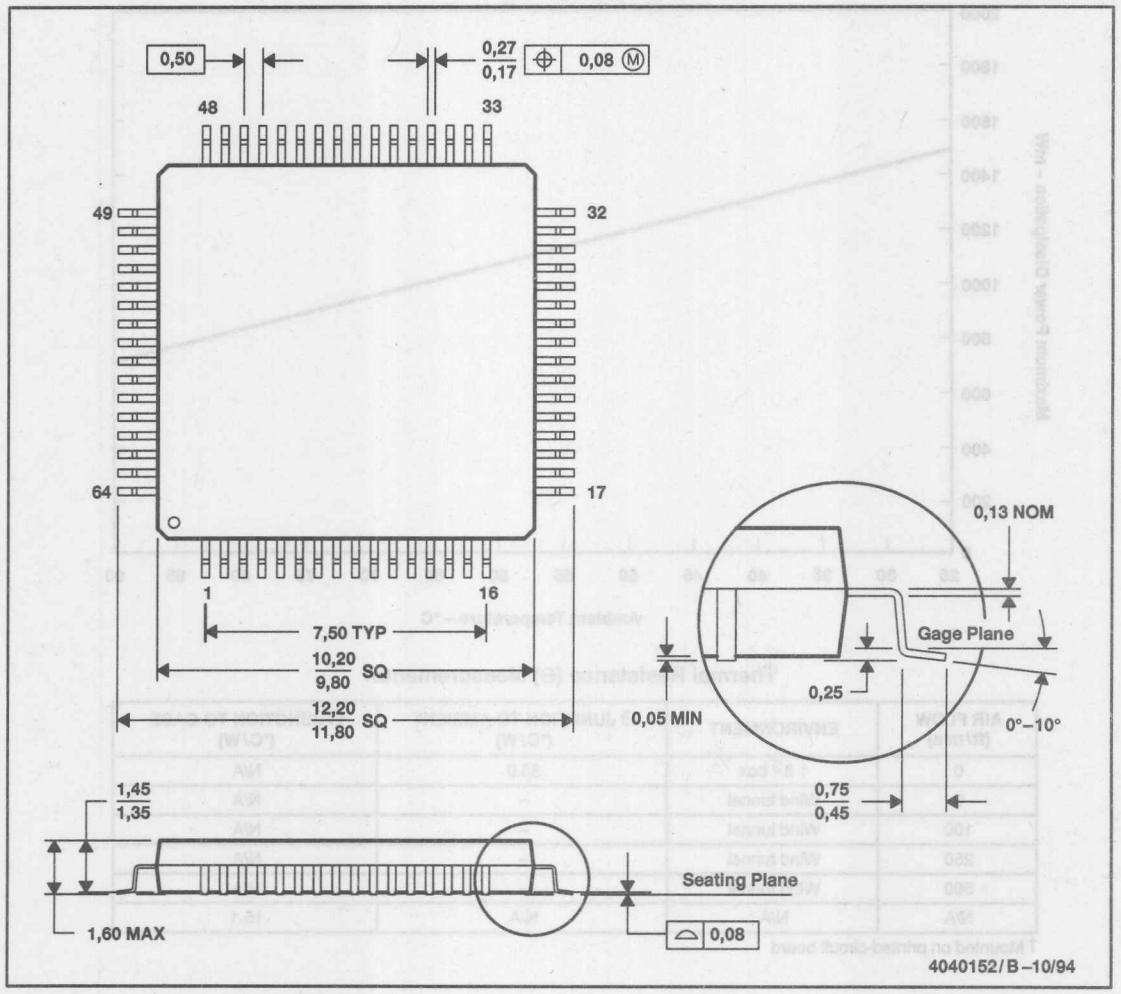


Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	83.9	N/A
0	Wind tunnel	–	N/A
100	Wind tunnel	–	N/A
250	Wind tunnel	–	N/A
500	Wind tunnel	–	N/A
N/A	N/A	N/A	15.1

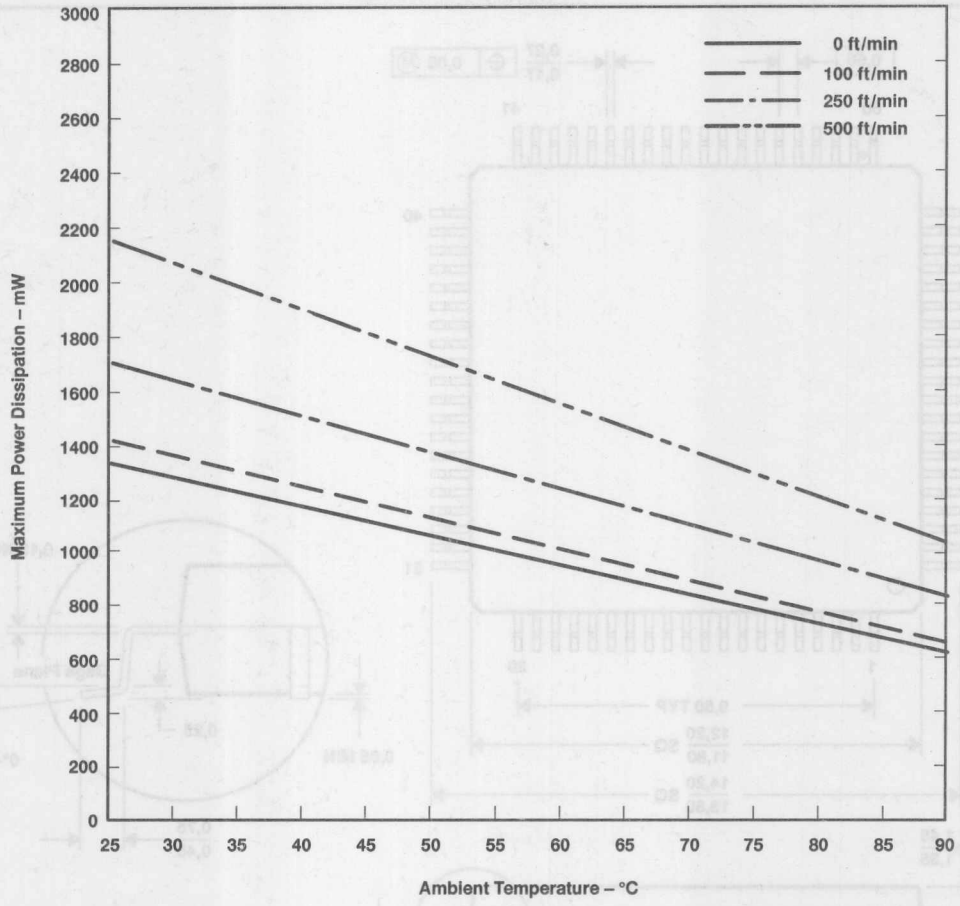
† Mounted on printed-circuit board

PM/S-PQFP-G64 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

64-Pin TQFP (PM)† Package Power Dissipation Derating at Varying Air Flows

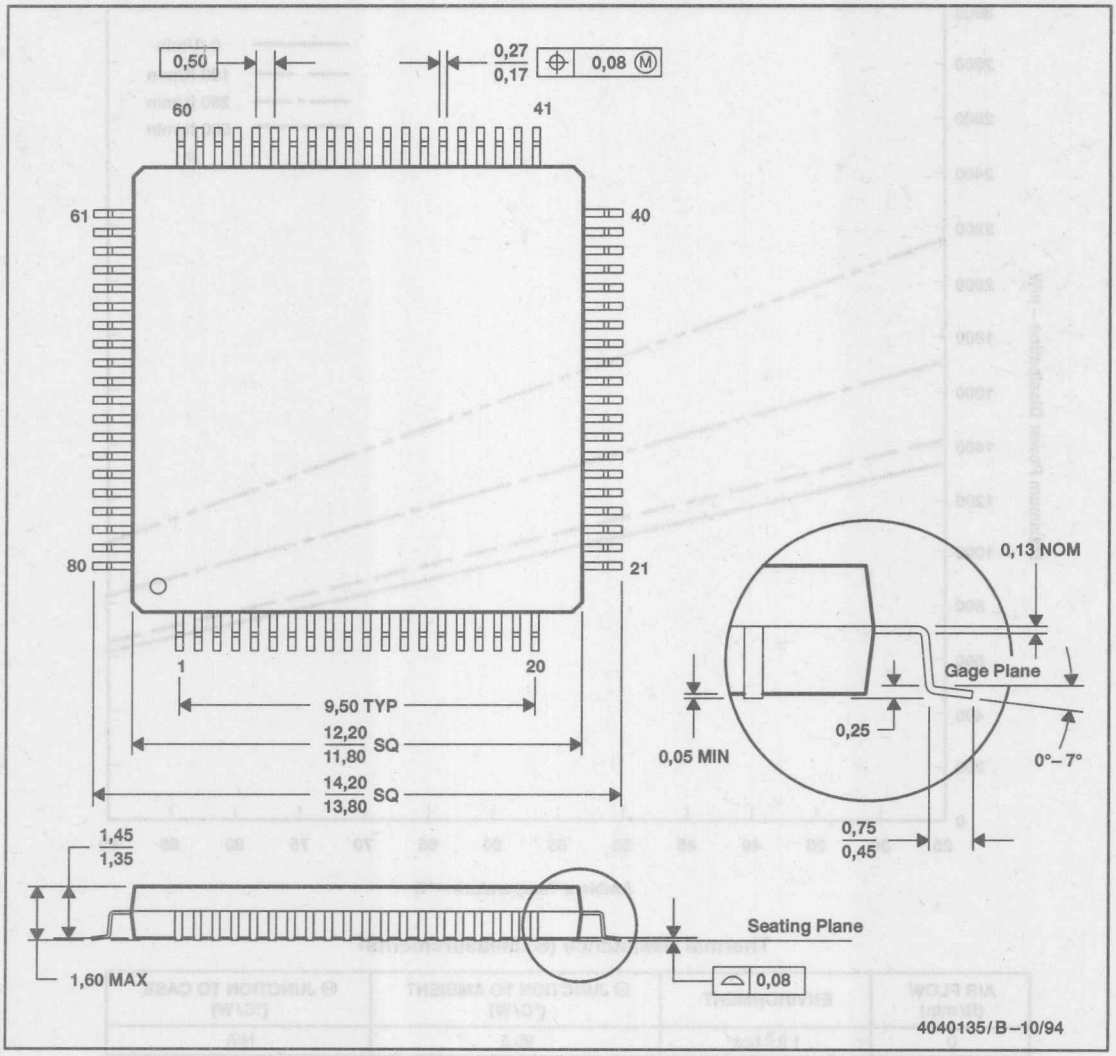


Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	95.5	N/A
0	Wind tunnel	92.5	N/A
100	Wind tunnel	87.8	N/A
250	Wind tunnel	72.9	N/A
500	Wind tunnel	57.8	N/A
N/A	N/A	N/A	10.4

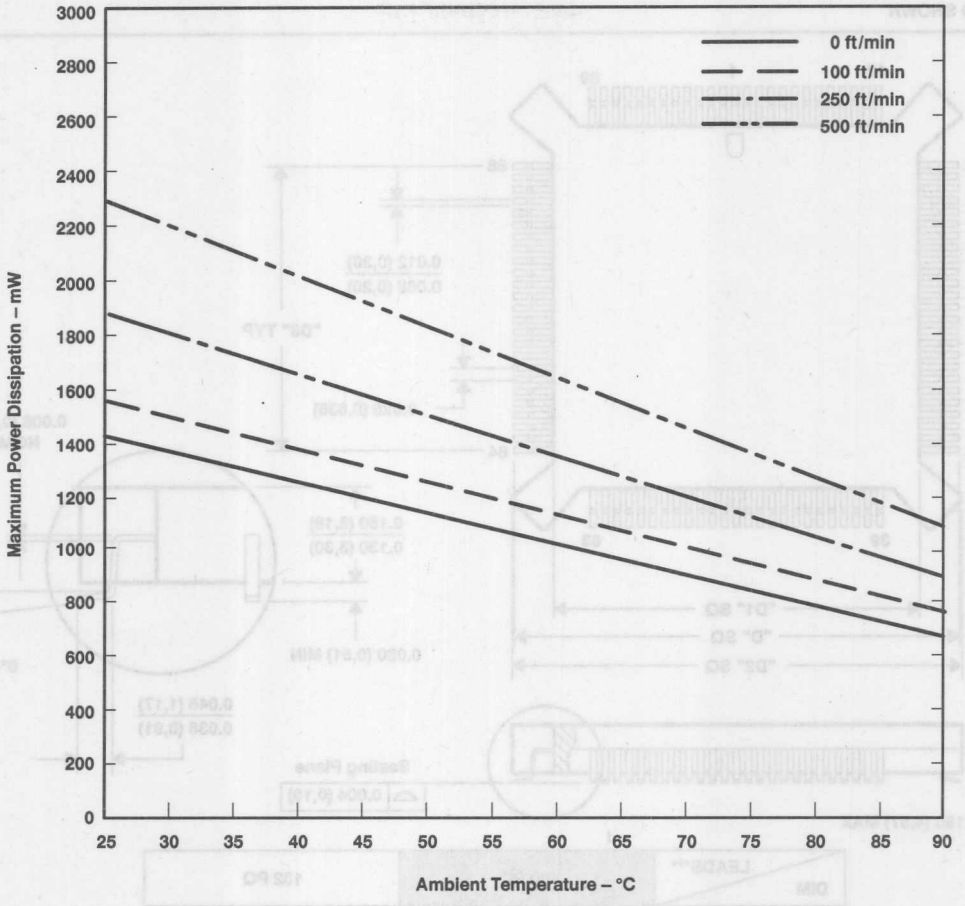
† Mounted on printed-circuit board

PN/S-PQFP-G80 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

80-Pin TQFP (PN) Package Power Dissipation Derating at Varying Air Flows



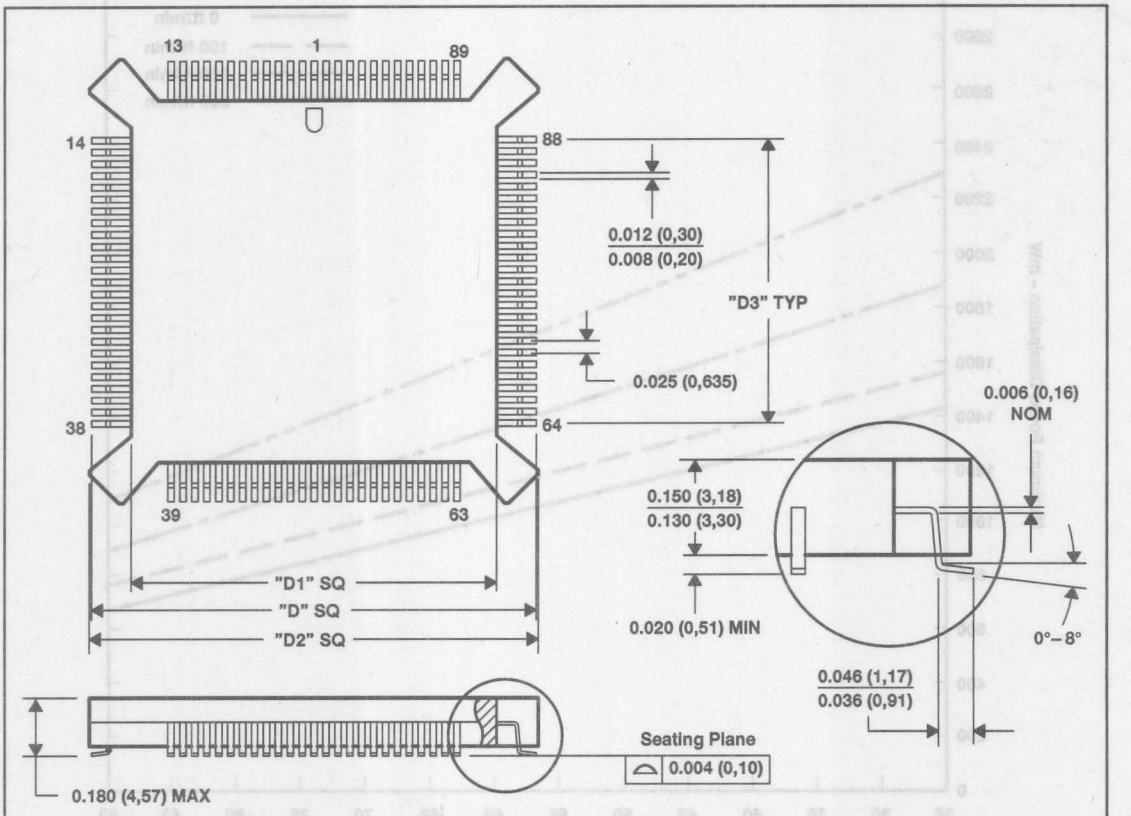
Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	89.2	N/A
0	Wind tunnel	87.8	N/A
100	Wind tunnel	79.1	N/A
250	Wind tunnel	67.3	N/A
500	Wind tunnel	54.2	N/A
N/A	N/A	N/A	10.6

† Mounted on printed-circuit board

PQ/S-PQFP-G* PLASTIC QUAD FLATPACK**

100 LEAD SHOWN

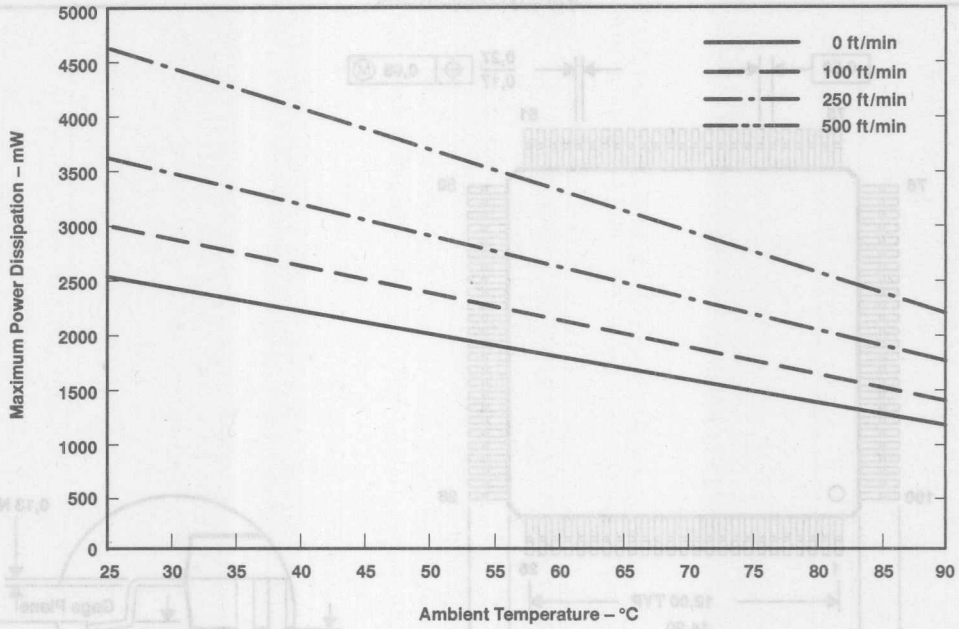


DIM \ LEADS***		100 PQ	132 PQ
"D"	MAX	0.890 (22,61)	1.090 (27,69)
	MIN	0.870 (22,10)	1.070 (27,18)
"D1"	MAX	0.766 (19,46)	0.966 (24,54)
	MIN	0.734 (18,64)	0.934 (24,72)
"D2"	MAX	0.912 (22,16)	1.112 (28,25)
	MIN	0.888 (22,56)	1.088 (27,64)
"D3"	TYP	0.600 (15,24)	0.800 (20,32)

4040045/B–10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-069

132-Pin PQFP (PQ) Package Power Dissipation Derating at Varying Air Flows

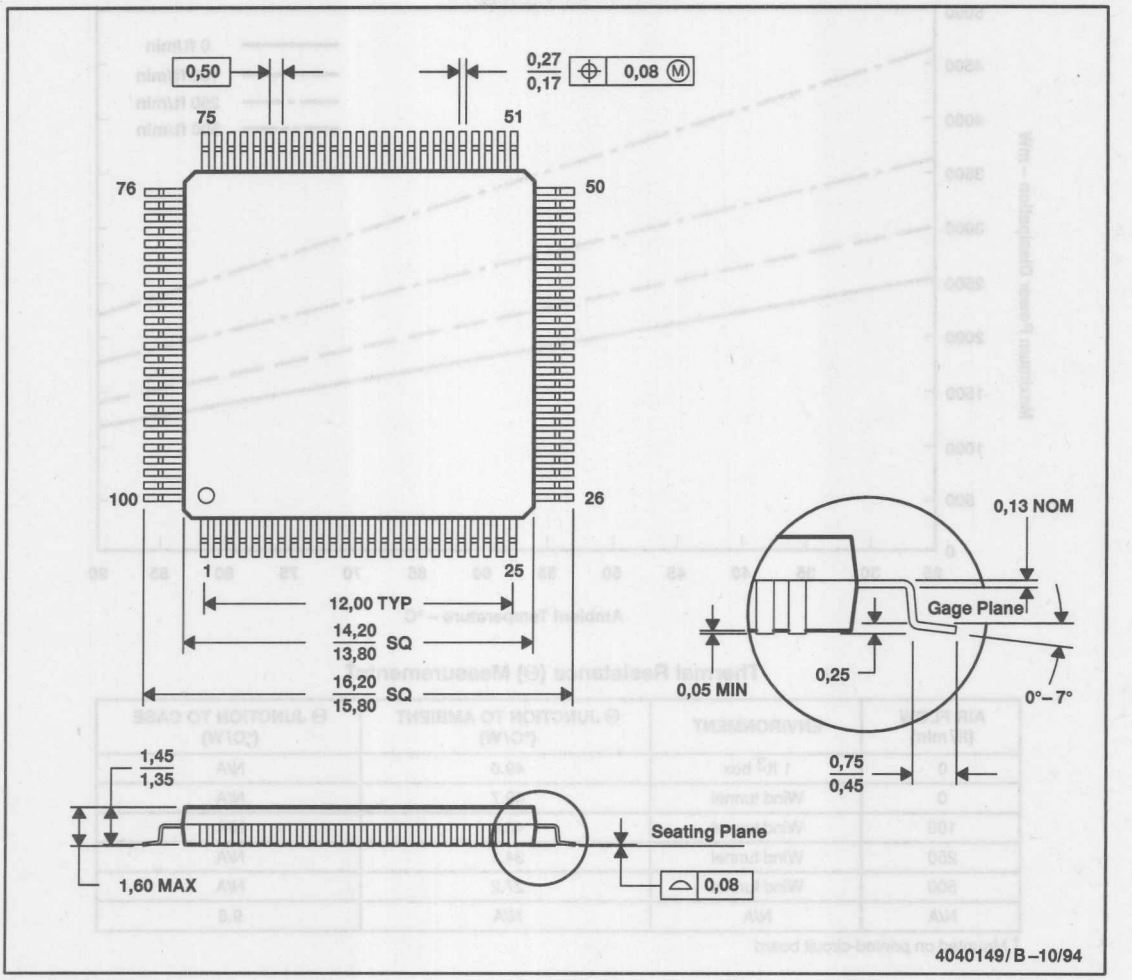


Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	49.6	N/A
0	Wind tunnel	49.7	N/A
100	Wind tunnel	42.6	N/A
250	Wind tunnel	34.1	N/A
500	Wind tunnel	27.2	N/A
N/A	N/A	N/A	9.8

† Mounted on printed-circuit board

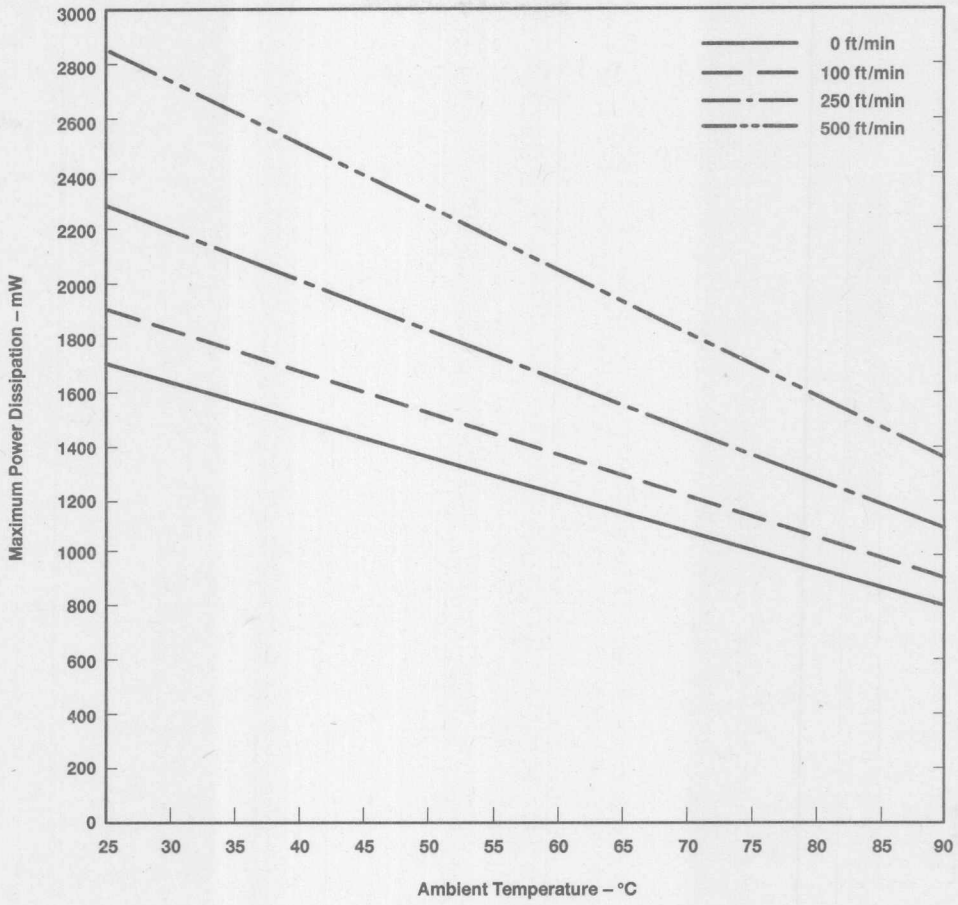
PZ/S-PQFP-G100 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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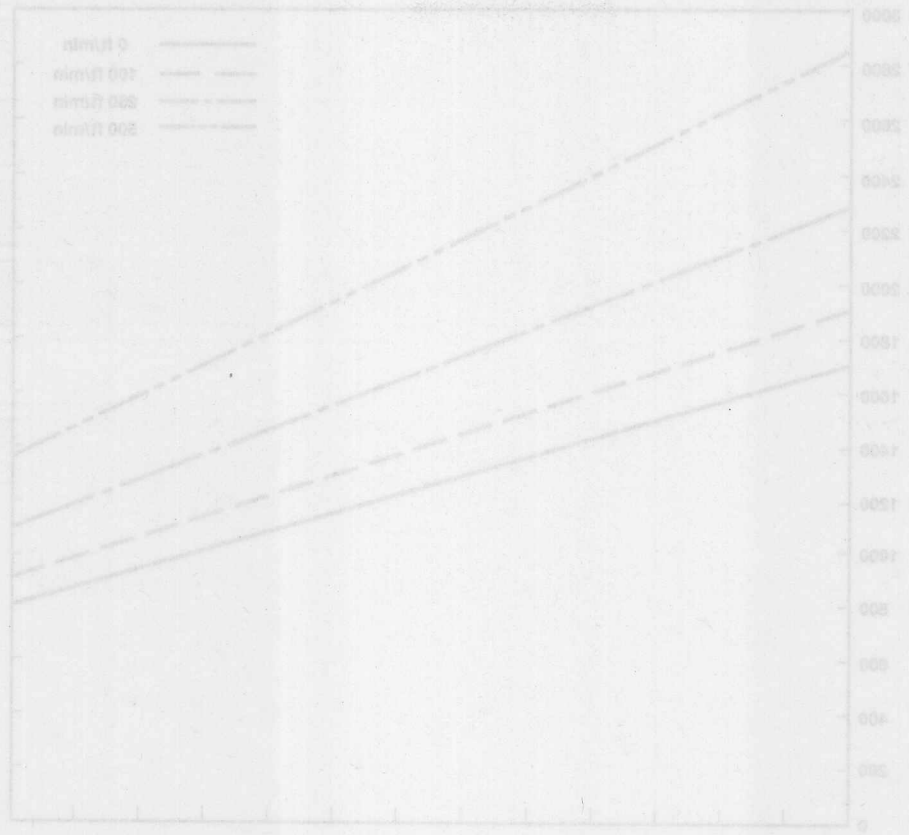
100-Pin TQFP (PZ) Package Power Dissipation Derating at Varying Air Flows



Thermal Resistance (Θ) Measurements†

AIR FLOW (ft/min)	ENVIRONMENT	Θ JUNCTION TO AMBIENT (°C/W)	Θ JUNCTION TO CASE (°C/W)
0	1 ft^3 box	79	N/A
0	Wind tunnel	72.7	N/A
100	Wind tunnel	65.2	N/A
250	Wind tunnel	54.5	N/A
500	Wind tunnel	43.6	N/A
N/A	N/A	N/A	11.6

† Mounted on printed-circuit board



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6 Device Models

VHDL Models

VHDL models for the FIFOs listed below are available through your local Texas Instruments sales office:

SN74ACT2226 (Dual 64 × 1, Dual 256 × 1 Clocked FIFO)
SN74ACT3632-15/20/30 (512 × 36 × 2 Clocked FIFO)
SN74ACT3651-15/20/30 (2048 × 36 Clocked FIFO)
SN74ACT7881-15/20/30 (1024 × 18 Clocked FIFO)
SN74ACT7804-20/25/40 (512 × 18 Strobed FIFO)
SN74ACT7813-15/20/25/40 (64 × 18 Clocked FIFO)
SN74ACT7814-20/25/40 (64 × 18 Strobed FIFO)

Logic-Modeling Behavioral Models

The Logic Modeling Group continually updates model libraries. If you do not see a TI FIFO model that you need, contact a local Logic Modeling Group representative or call 1-800-34MODEL (1-800-346-6335) for current availability. For international inquiries, call 503-690-6900.

Behavioral models of the following TI FIFOs are available from the Logic Modeling Group, 19500 N.W. Gibbs Drive, P.O. Box 310, Beaverton, OR 97075, 503-690-6900, fax: 503-690-6906, Technical Product Support: 1-800-445-1888.

DEVICE	ARCHITECTURE	ORGANIZATION	SPEED SORTS
SN74ACT2226	Clocked	64 × 1	
SN74ACT2228	Clocked	256 × 1	
SN74ACT2227	Clocked	64 × 1	
SN74ACT2229	Clocked	256 × 1	
SN74ABT3611	Clocked	64 × 36	−15, −20, −30
SN74ABT3612	Clocked	64 × 36 × 2	−15, −20, −30
SN74ABT3613	Clocked	64 × 36	−15, −20, −30
SN74ABT3614	Clocked	64 × 36 × 2	−15, −20, −30
SN74ACT3632	Clocked	512 × 36 × 2	−15, −20, −30
SN74ACT3641	Clocked	1K × 36	−15, −20, −30
SN74ACT7813	Clocked	64 × 18	−15, −20, −25, −40
SN74ACT7803	Clocked	512 × 18	−15, −20, −25, −40
SN74ABT7819	Clocked	512 × 18 × 2	−12, −15, −20, −30
SN74ACT7811	Clocked	1K × 18	−15, −18, −20, −25
SN74ACT7807	Clocked	2K × 9	−15, −20, −25, −40
SN74ACT7814	Strobed	64 × 18	−20, −25, −40
SN74ACT7806	Strobed	256 × 18	−20, −25, −40
SN74ACT7804	Strobed	512 × 18	−20, −25, −40
SN74ABT7820	Strobed	512 × 18 × 2	−15, −20, −25, −40
SN74ACT2235	Strobed	1K × 9 × 2	−20, −30, −40, −60
SN74ACT2236	Strobed	1K × 9 × 2	−20, −30, −40, −60
SN74ACT7808	Strobed	2K × 9	−20, −25, −30, −40
SN74ACT7201	Asynchronous	512 × 9	−15, −25, −35, −50
SN74ACT7202	Asynchronous	1K × 9	−15, −25, −35, −50
SN74ALS2233	Asynchronous	64 × 9	
SN74ALS2238	Asynchronous	32 × 9 × 2	
SN74ALS2232	Asynchronous	64 × 8	
SN74ALS236	Asynchronous	64 × 4	
SN74ALS232	Asynchronous	64 × 4	

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7 Quality and Reliability Assurance

Qualification of Products and Processes

Introduction

A significant change has recently occurred in the way our customers qualify products. At one point, virtually all customers were spending millions of dollars annually, duplicating supplier qualification tests. However, as years of improving quality and reliability have raised the level of customer confidence and satisfaction, much of this in-house customer testing was eliminated and customers began to rely on Texas Instruments (TI) test results.

This approach also became applicable to major process changes. If a major process change is made to a product, TI qualifies the new process through extensive testing and transmits the data to customers for approval.

Both of these qualification approaches form the basis of the quality and reliability assurance practices for TI's FIFO products.

Quality and Reliability Assurance in Integrated-Circuit Design

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Quality and Reliability Assurance in Integrated-Circuit Design

Quality and reliability of the products are important elements in achieving customer satisfaction. These elements must be designed in during the design phase of the products and built in during fabrication. To ensure that this occurs, all integrated-circuit designs at Texas Instruments (TI) follow a three-tier design-rule structure as follows:

- General company-wide quality and reliability rules
- Process-specific design rules
- Methodology-oriented design rules

General Quality and Reliability Rules

The process-independent company-wide quality and reliability rules are defined and, as necessary, adapted to new requirements by a committee that is organized worldwide. These rules include directives for:

- ESD protection
- Latch-up protection
- Electromigration constraints on current density
- Maximum junction temperature
- Hot-electron injection

Strict application of these rules results in high process yields and high quality and reliability. These rules are company standards at TI, the result of many years of experience in semiconductor production.

Process-Specific Design Rules

These rules are created by a design council that is composed of members from different areas including process development, product development, wafer fabrication, test development, and quality and reliability engineering. The design council meets on a regular basis to generate and periodically update the design notebook, which contains all the process-specific design rules. The design council acts as a forum for worldwide sharing of experience, knowledge, and problems related to a specific process. The design notebook is maintained on a central computer, which can be accessed by any authorized user at any worldwide TI facility; therefore, the latest version is instantly available for worldwide access. Major chapters of the notebook are:

- General guidelines for circuit design
- Process parameters
- Simulation models for processes
- Simulation instructions and guidelines
- Design methodology
- Design documentation
- Process-layout rules
- Reliability rules
- Electrical models for circuit packages
- Requirements for photomask generation in wafer fabrication

Methodology-Oriented Design Rules

The guidelines for design methodology are basically the same for all types of semiconductors at TI and are rigidly adhered to. This gives the designer a high confidence level that the target specifications are maintained, the functions of a device are correctly implemented, and a high standard of reliability is achieved. Designing integrated circuits is now a classic application for computer-aided design. Each designer has a network at their disposal for circuit entry, circuit simulation, mask layout, and circuit verification.

Change Control

Continuous improvement at TI is recognized as a key method of offering greater value to our long-term customers. A major responsibility is to ensure that improvements in the materials and processes do not adversely affect our customers. One of TI's missions is to assure our customers of a source of qualified supply and to provide a stable market to our suppliers.

Through joint development efforts with strategic suppliers, TI has provided our customers with a steady stream of improvements to the materials that are used in volume production. In addition, to remain competitive, new equipment

and process methods are constantly being evaluated. It is TI's goal to keep our customers informed of all changes identified as requiring notification.

The change-control system is contained in TI's quality system and covers all operations worldwide. The list of changes requiring notification (see Table 1) is based upon a dynamic composite of documented customer requirements and experience. The required qualification testing and process-capability studies also are defined in the quality system. The change notification contains a description of the change, reason for change, anticipated impact on customers, if any, supporting reliability and applicable electrical-characterization data, and effective timing.

Table 1. Examples of Major Changes That Can Require User Notification

PROCESS	MAJOR DESIGN CHANGE	
Wafer Fab	Wafer-fab site Process flow Gate-oxide materials Dielectric material Metallization material Passivation material Die-coating material	Wafer diameter Diffusion dopant Gate-oxide thickness Polysilicon-dopant type Metallization thickness Passivation thickness Die-coating thickness
Assembly	Assembly site Plating material Wire-bond material Sealing material Marking method	Leadframe-base material Plating method Mold-compound material Die-attach material Marking appearance
Test	Elimination of test steps	
Electrical Specification	Relaxation of AC specification Relaxation of DC specification	
Mechanical Specification	Case outline Loosening tolerance(s)	
Packing/Shipping/Labeling/Environment	Carrier (reel, tray) dimensions Maximum storage temperature Drypack requirements	

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Environmental Laboratory

The environmental-test laboratories provide environmental-test services, both climatic and mechanical, for device qualification, engineering evaluation, and acceptance purposes to operating entities within Texas Instruments (TI). TI acquires and maintains suitable calibrated equipment with which the test and inspections required by external customers and internal specifications can be performed. A properly trained and certified staff is maintained to perform the required tests and inspections in a timely, cost-effective manner. The TI laboratories worldwide are maintained in a certified/approved status for those customers and agencies requiring this condition. TI conforms to national and international standards and is certified as an approved self-qualification lab for several major customers.

Lab personnel interface closely with equipment manufacturers and standards bodies for maintenance of test capabilities. Environmental-test methods and specifications are developed and controlled for TI worldwide. For continuous improvement in maintaining world-class status, the environmental lab uses self-measurement indices by tracking cycle time and customer satisfaction, both internal and external.

Methods of Measuring Component Reliability

Product-reliability tests are performed at high-stress conditions so that performance levels can be established during a relatively short test duration. Specific stress conditions are chosen because they represent accelerated versions of various device-application environments and allow meaningful extrapolations to lower stress levels. These reliability-test conditions are held constant so that product improvements or deficiencies can be readily discerned by comparing current test data with the historical database on identical tests. However, extreme care is exercised to avoid any overstress condition that could cause a device failure not related to the final device application.

The reliability stresses used most widely at TI are:

- Life stress
- Biased temperature and humidity
- Biased highly accelerated stress test (HAST)
- Nonbiased autoclave
- Temperature cycling (air-to-air)

Failure-Rate Calculations for FIFO Products

The failure-rate performance for FIFO products has been calculated to be 15 FITs (failures per 10^6 device hours). This calculation is based upon the following assumptions:

- Applied supply voltage: 5 V
- Junction temperature; 125°C or 150°C
- Activation energy; 0.7 eV
- Derating temperature; 55°C
- Chi^2 upper confidence level: 60%

Qualification Data for FIFO Products

Qualification data has been gathered for each of the key design sets in TI's FIFO product line. This data represents the results from life test and ESD characterization (see Table 1).

Table 1. Life-Test and ESD-Characterization Data

DESIGN SERIES	QUALIFICATION VEHICLE	PACKAGE TYPE	LIFE TEST			ESD LEVEL	
			125°C, 68 HRS DYNAMIC	125°C, 1000 HRS DYNAMIC	150°C, 300 HRS STATIC	HUMAN-BODY MODEL	MACHINE MODEL
SN74ABT3612	SN74ABT3614	PCB			0/116	II	I
SN74ABT3613	SN74ABT3614	PCB/PQ				II	I
SN74ABT3614	SN74ABT3614	PCB				II	I
SN74ABT7819	SN74ABT7819	PH/PN			0/116	II	II
SN74ABT7820	SN74ABT7819	PH/PN				II	II
SN74ACT2235	SN74ACT2235	FN		0/116		I	I
SN74ACT2236	SN74ACT2235	FN				I	I
SN74ACT7808	SN74ACT7808	PAG		0/116		I	I
SN74ACT2226	SN74ACT2229	DW		0/116		II	I
SN74ACT2227	SN74ACT2229	DW				II	I
SN74ACT2228	SN74ACT2229	DW				II	I
SN74ACT2229	SN74ACT2229	DW				II	I
SN74ACT3632	SN74ACT3632	PCB/PQ			0/116	I	I
SN74ACT3641	SN74ACT3632	PCB/PQ				I	I
SN74ACT7803	SN74ACT7803	DL	0/116			I	I
SN74ACT7804	SN74ACT7803	DL				I	I
SN74ACT7805	SN74ACT7803	DL				I	I
SN74ACT7806	SN74ACT7803	DL				I	I
SN74ACT7807	SN74ACT7807	FN	0/116			I	I
SN74ACT7811	SN74ACT7801	FN/PN	0/116			I	I
SN74ACT7813	SN74ACT7803	DL	0/116			I	I
SN74ACT7814	SN74ACT7803	DL				I	I

	HUMAN-BODY MODEL (V)	MACHINE MODEL (V)
Level I	0–1999	0–199
Level II	2000–3999	200–399
Level III	4000 or greater	400 or greater